
Logic Analyzer Capture of DDRII Signals Above 400MT/s

Is DDRII just too fast to probe with a logic analyzer?

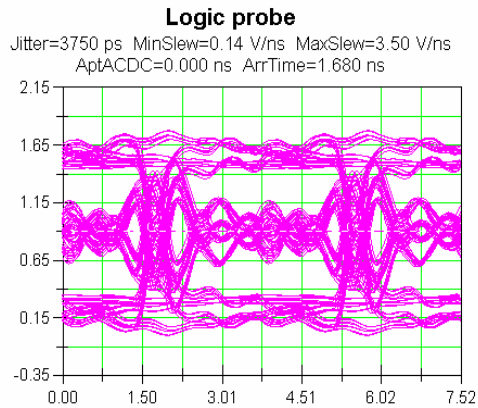


Figure 2

The valid eye is gone in this simulation of control lines on the interposer at 533MT/s.

What Causes This Deterioration of the Eye Pattern?

Transmission Line Effects on Address and Control Lines: Address and control lines on DDRII are parallel terminated to V_{tt} on the motherboard. As address and control signals pass along the transition line, they are “stubbed” out to the memory components at each DIMM location (see Figure 3). This is one reason why most unbuffered DDRII systems are limited to two DIMMs per channel. Loading affects from one DIMM slot will impact the available signal to the other. Reflections off the open termination on each DIMM’s 16 memory chips will also cause signaling issues on the memories in the other slot.

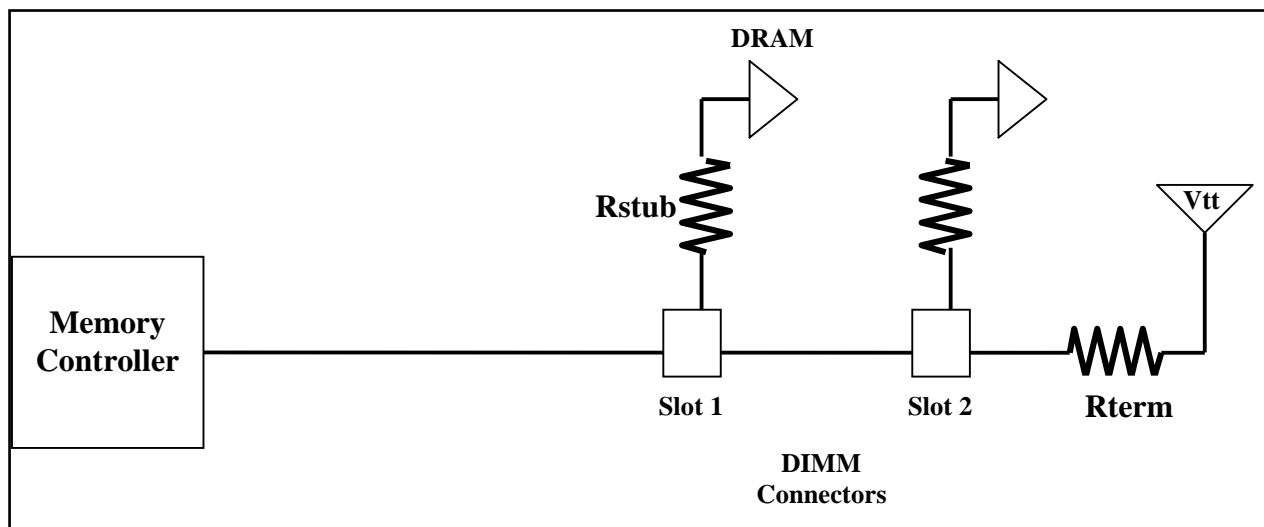


Figure 3

Inserting an extender card into the DIMM slot will change the magnitude and timing relationship of that reflection and may adversely affect the signal presented to the second DIMM. Since each stub is essentially an open termination, as address and control signals pass along the transmission line, they are half-height (using a 50-Ohm driver and a 50-Ohm impedance transmission line). See Figure 4.

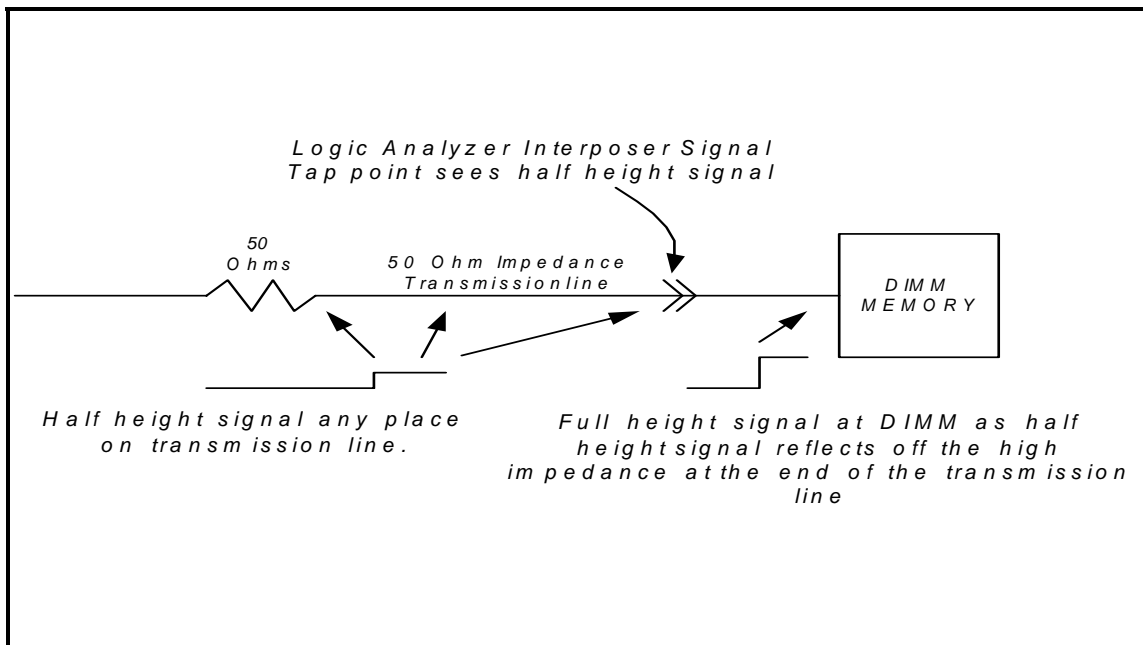


Figure 4

When the half-height signal reflects off the high impedance at the end of the transmission line (input to memory chip) it becomes full-height (half being driven is added with the half that is reflected) as it moves back to its source.

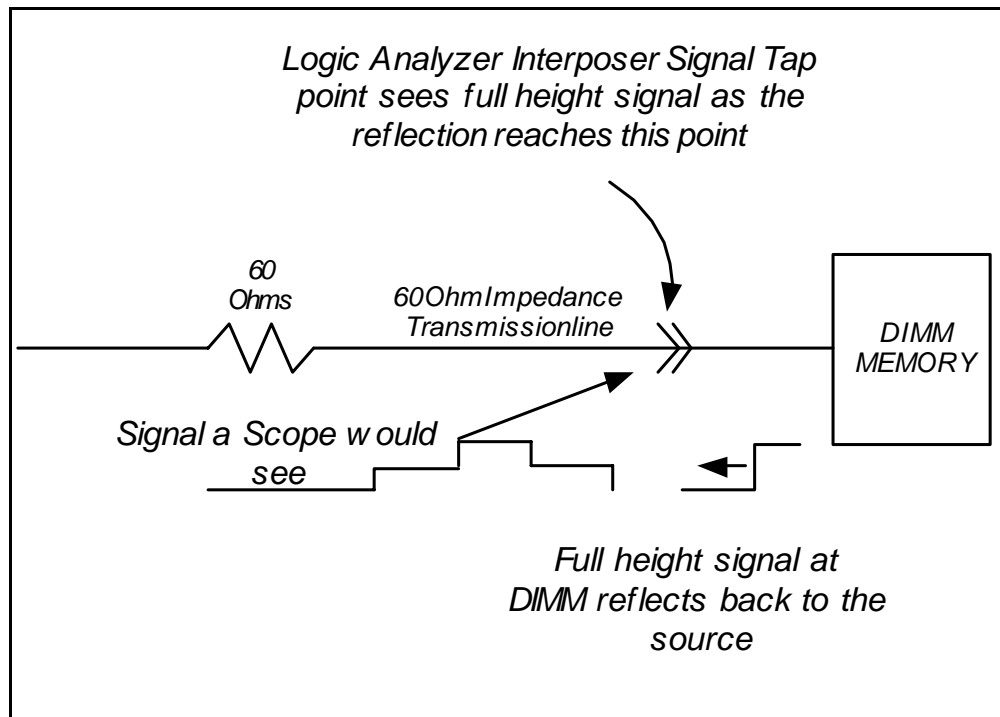


Figure 5

The full-height time is the high-time of the original signal; minus the time it took for the signal to travel to the end of the transmission line; minus the time for the full-height signal to travel back to the logic analyzer probe point. The signal will go to half-height level again as soon as the signal from the source goes low and reaches the tap-point. This leaves, again, only a half-height signal until the low from the source reaches the end and reflects a low back. At that point the signal seen at the logic analyzer probe point drops to a low.

The duration of the high signal is affected by two items:

1. Due to travel time from the tap-point to the memory chip and back, the greater the distance from the logic analyzer connection to the end of the transmission line, the less time the signal will be full-height at the tap-point. The ideal probe point is on the memory chip.
2. As signals increase in speed, their time at full-height gets less. With less time high, the logic analyzer sample point valid eye will also diminish.

Couple the two above forces that are closing the valid eye-pattern and add high-speed noise. The addition of any interposer will also add the problems of another connector and increased trace lengths. All this put together gives a marginal eye for the address and control lines at speeds over 400MT/s as seen at the DIMM edge connector. However, the eye remains very good at the memory chip. This brings the conclusion that interposer probes of any kind should not be considered as a valid alternative above 400MT/s. Simulations and actual testing of this assertion are in Appendix A & B.

An Innovative Solution: NEXVu

Nexus Technology's family of NEXVu DDRII DIMMs provides a new probing method to allow DDRII Logic Analyzer captures at 533MT/s and faster. This new interface to the Tektronix Logic Analyzer takes the form of a modified DIMM that is designed to JEDEC standards, but with Logic Analyzer connections attached to the memory chips. See Figure 6.

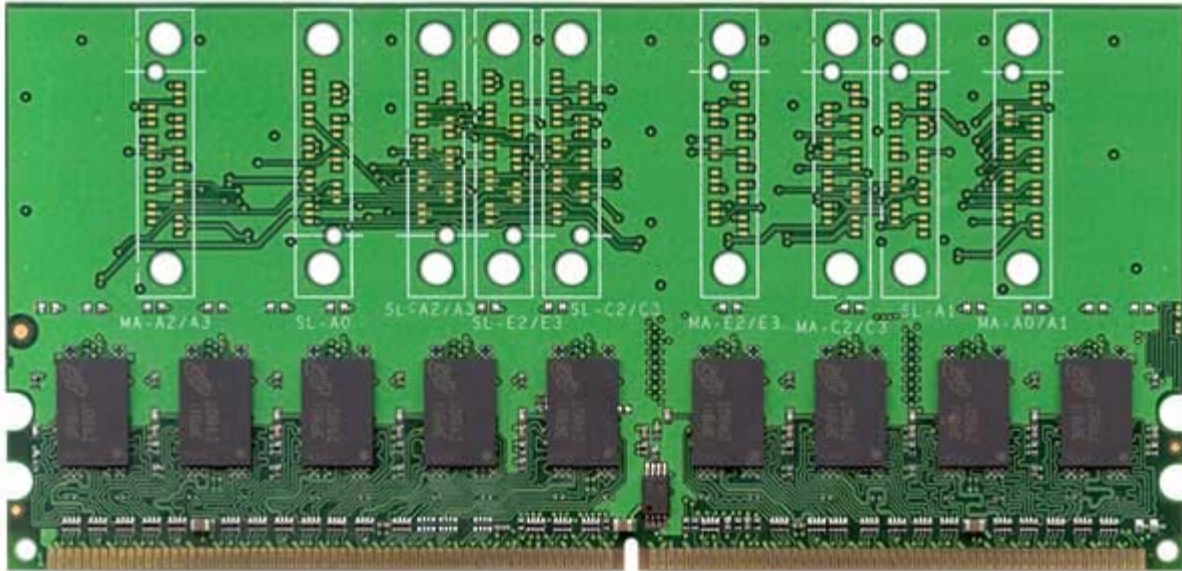


Figure 6 – NEXVu DDRII DIMM with Tektronix Compression Pads

This new design approach solves the problem of trying to acquire signals at the edge connector of the target DIMM by putting the logic analyzer probe points on a DIMM designed to JEDEC standards. Since the signals are only valid at the memory devices, this is where the probing is done. This approach provides excellent visibility of the DDRII bus. Note the signal quality of the simulations in Figures 7 & 8. Also refer to the scope capture in Figure 9.

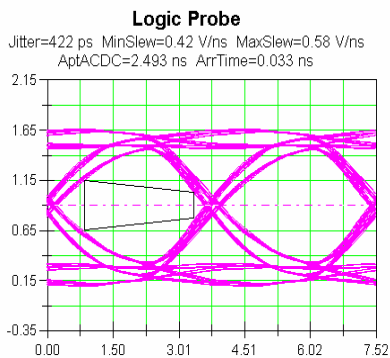


Figure 7

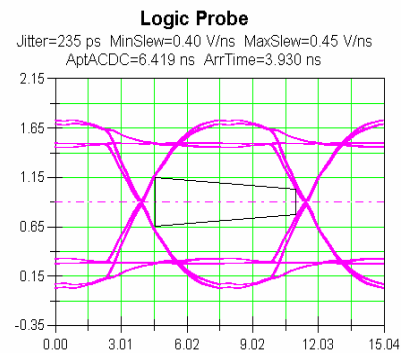


Figure 8

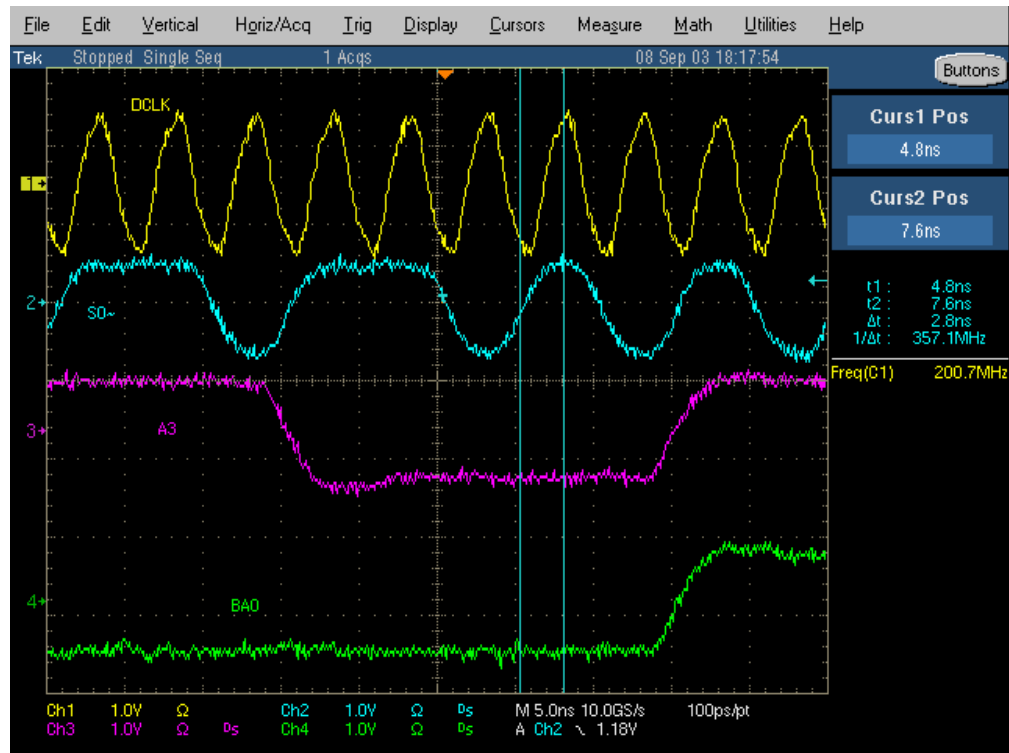


Figure 9 - From the Top: Clock, S0~, A3, BA0

Standard features of the new NEXVu DDRII solutions include:

- DDRII DIMM designed to JEDEC standards with designed-in TLA connections
- Innovative approach provides visibility of actual eye-patterns, as seen by the memory chips
 - Size of a valid eye-pattern will be greater at the memory chips than at the edge connector, where the eye may not be large enough to be acquired by a logic analyzer. As bus speeds increase, this larger eye is imperative for logic analyzer capture.
- Memory Chips included on each DIMM
- DIMMs without memory chips for use with alternate vendor memories are also available
- Support for a variety of DIMM configurations
- Acquisition of DDRII Address / Command, Read and Write data
- Quick and easy connection between the DIMM bus and a Tektronix Logic Analyzer
- Currently supports DDRII400 and DDRII533. Faster support planned for future release. See Contact Information on last page for more information.
- DIMM design does not require a dedicated slot
- No impedance matching concerns as no interposer card is used

Simulation Results

Simulations were run at:

- The logic analyzer interposer sample point
- The DIMM edge connector (no interposer installed)
- A memory chip (on the other side of a stub resistor with no interposer installed)

Interposer Probe Sample Point Simulations

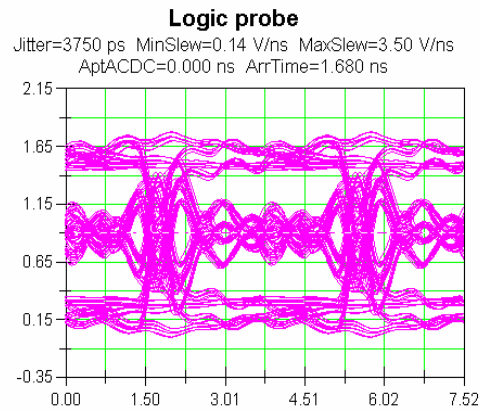


Figure 10

Control line S0# has no valid eye at the logic analyzer interposer probe sample point.

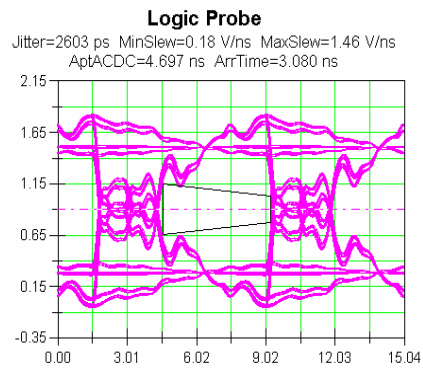


Figure 11

A definite degradation of the voltage swings is shown

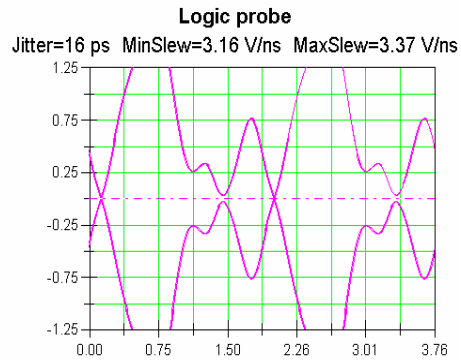


Figure 12

Clock sampled at the logic analyzer interposer. Due to the malformed clock, the logic analyzer may miss-clock acquisitions.

The conclusion is that at 533MT/s the interposer approach will not work.

DIMM Edge Connector Simulations - No logic analyzer interposer used

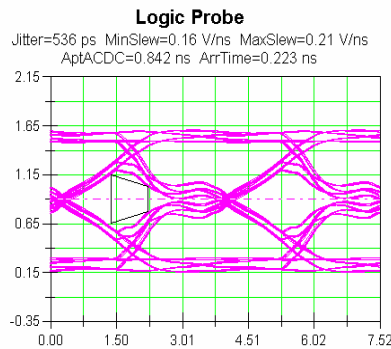


Figure 13

Control line S0# at the DIMM edge connector. Note that even when the interposer is not installed, the distance from the edge connector to the memory is too far and the eye-pattern is being reduced.

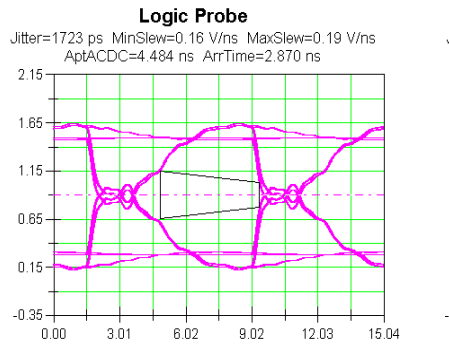


Figure 14

Address looks better but remember that there is no logic analyzer interposer in the system.

Conclusion – Even at the DIMM card edge with no interposer, the signals are of marginal quality for logic analyzer capture.

DIMM Memory Chip Simulation - taken at a memory chip on the DIMM (on the other side of an isolation resistor). No interposer used.

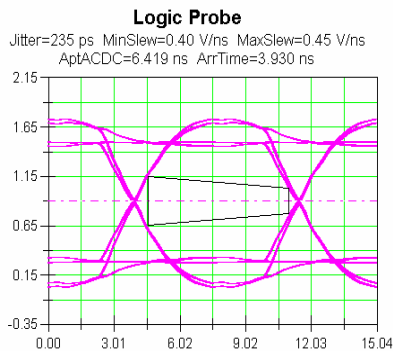


Figure 15

Note the high quality of the address capture compared to other simulations.

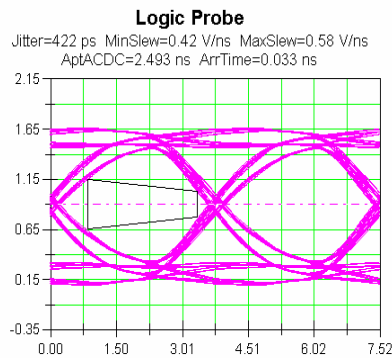


Figure 16

The same quality signal for control line S0#.

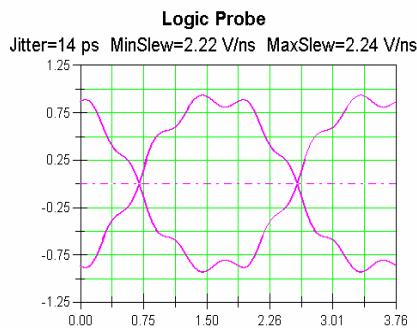


Figure 17

High quality Clock signal.

Conclusion – Probing on the legs of the memory chips allows for reliable logic analyzer acquisition without reducing system performance.

Real Measurements

Everyone can tell stories of the simulation that was faulty, often showing signals worse than found in real life. To insure the accuracy of the simulations, verification was done on a DDR Motherboard running in excess of 400MT/s.

Signal quality measurements were taken on an existing interposer card, and on a new DDRII NEXVu DIMM.

Real Measurements - Interposer Probe Sample Point

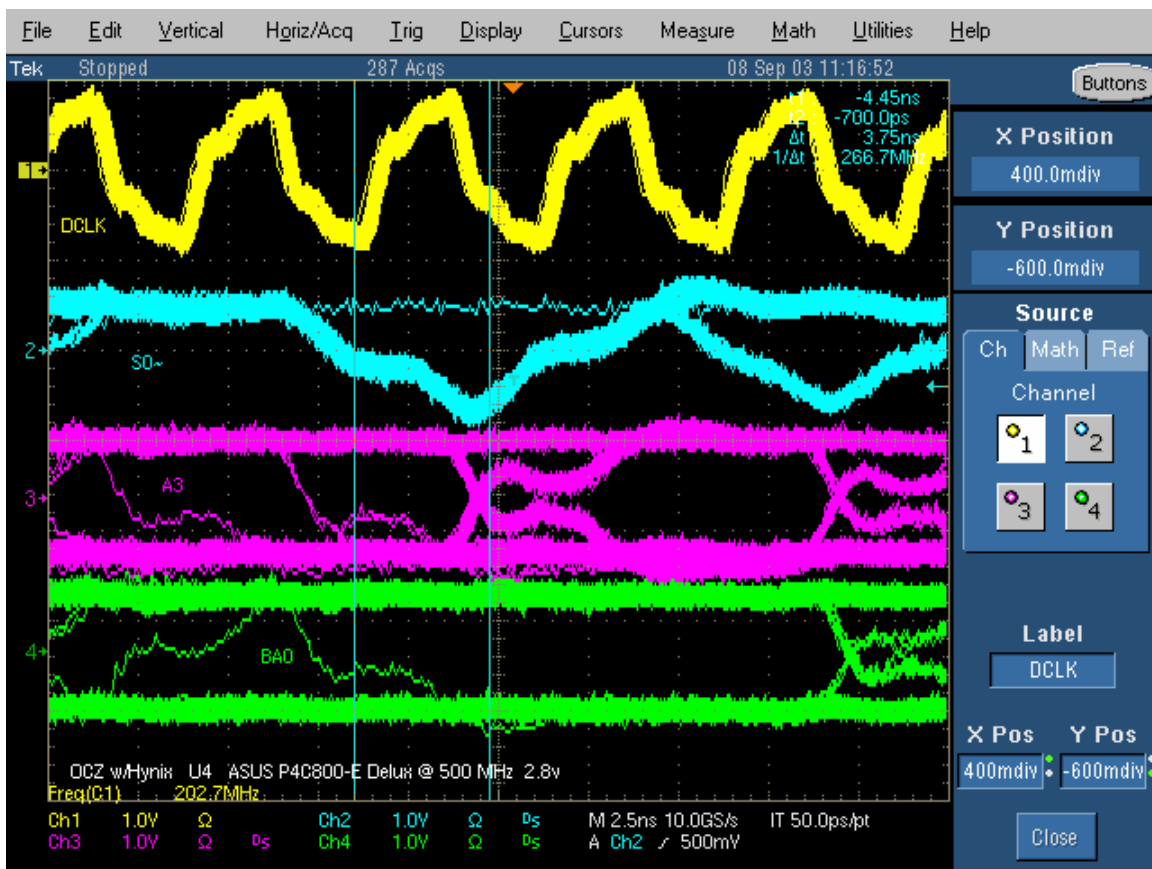


Figure 18

Note the eye-pattern reduction in size compared with the next capture with no interposer installed. At only 400MT/s, the eye is reduced by 30%.

Real Measurements - NEXVu DDRII DIMM Probe Sample Point

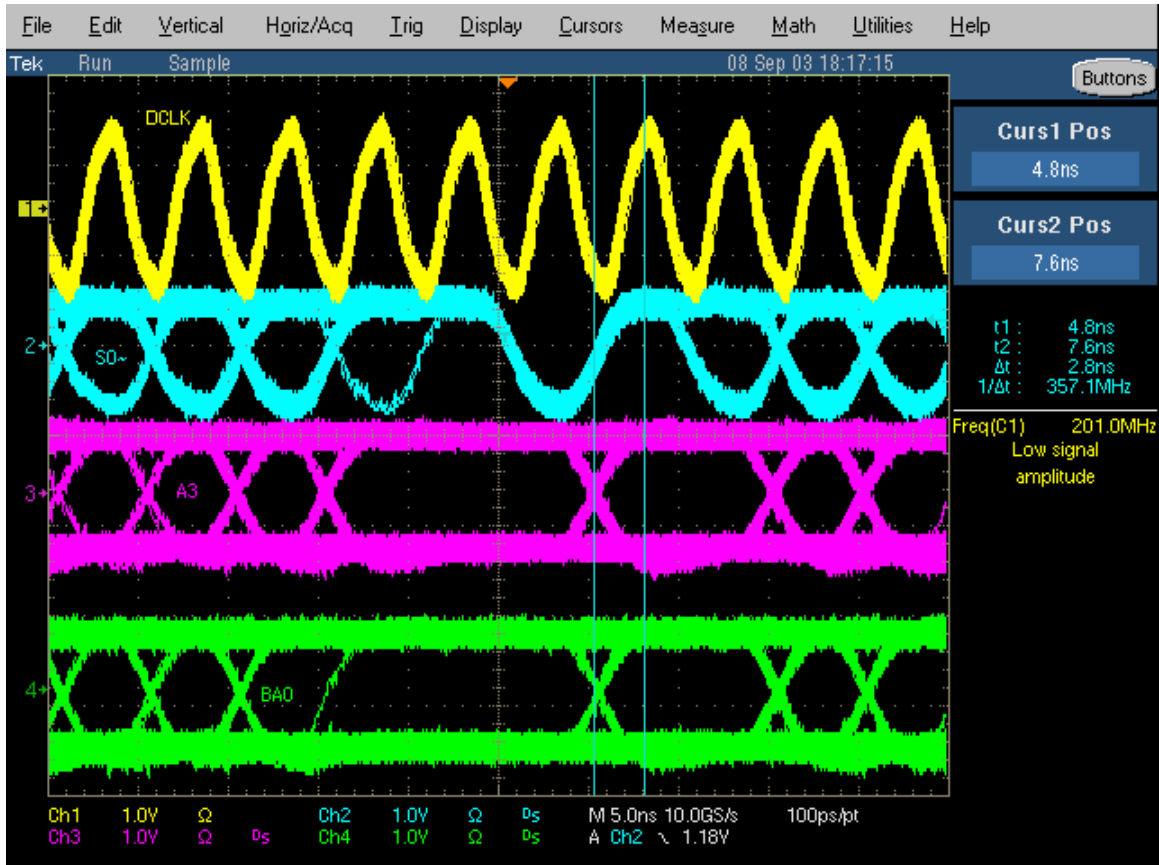
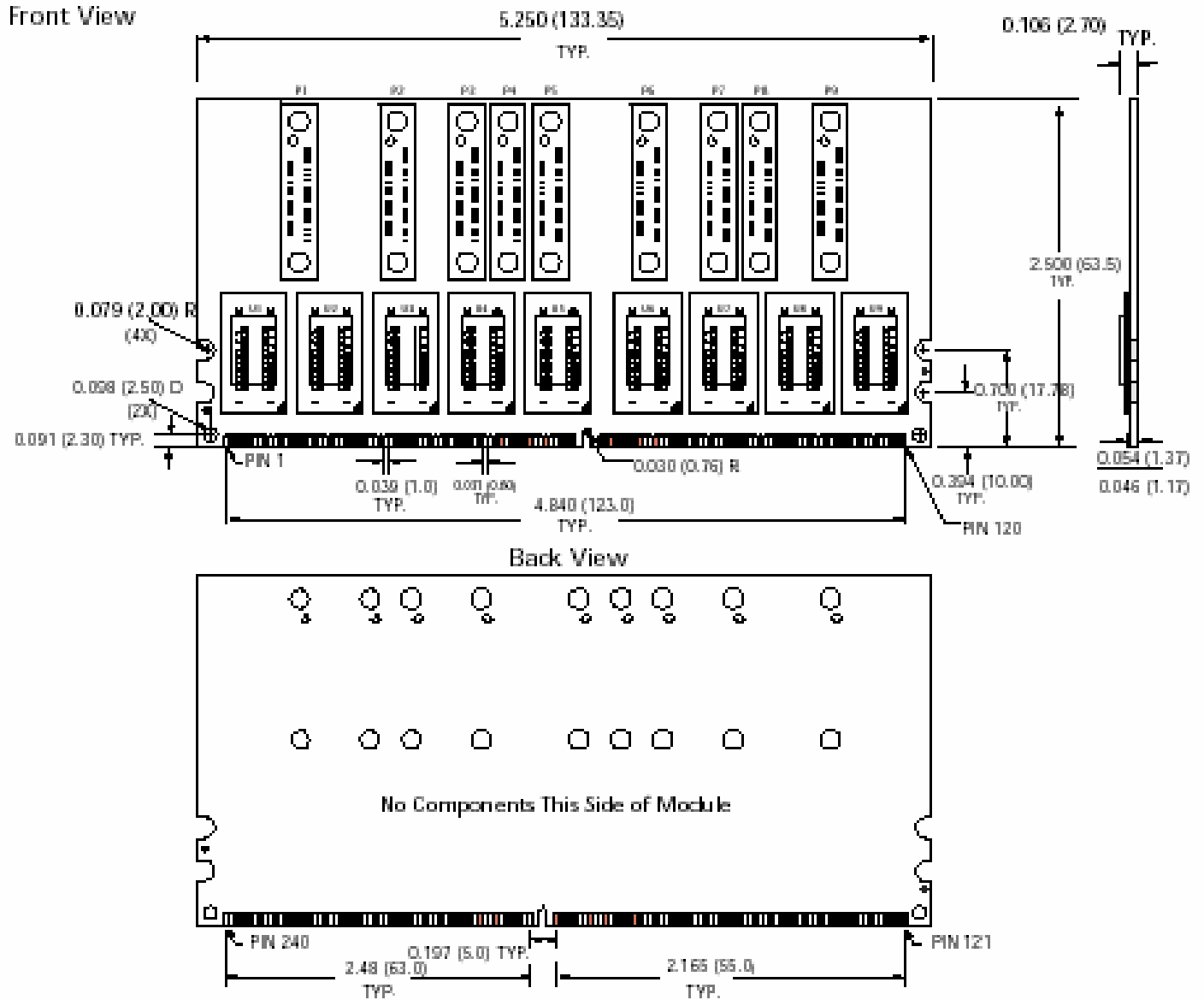


Figure 19

Note the nice clean signals. This verifies that the new NEXVu DDRII DIMMs are an innovative solution that will allow logic analyzer probing of DDRII 533MT/s buses and greater.

Mechanical Information for NEXVu DDRII DIMM

While each Logic Analyzer interface DIMM varies slightly, the only variation from a Standard DIMM is the height. Approximately 1 3/8" has been added to the height.



NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Approximately 1.5" of horizontal keep-out area is required for the Tektronix probes. A drawing with dimensions of the probe is shown in Figure 20.

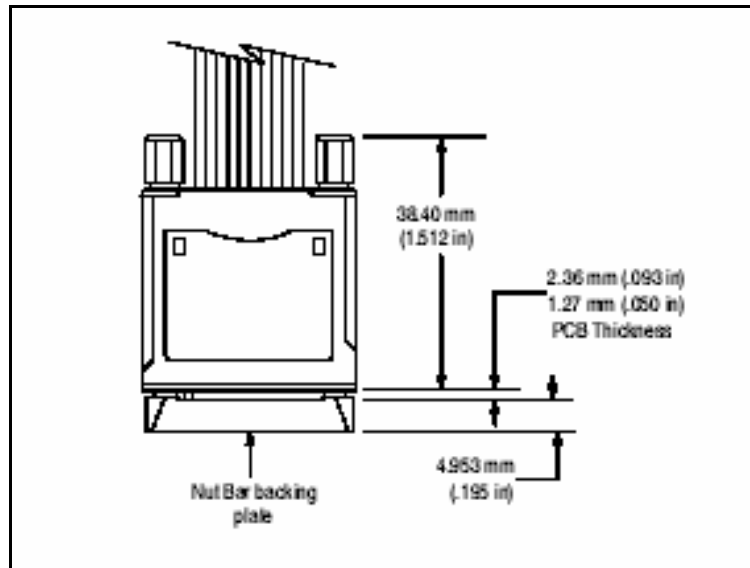


Figure 20

Tektronix Logic Analyzer Support / Configuration

A TLA700 equipped with three, merged, 136-channel, 450MHz state speed acquisition modules (TLA7AA4 or TLA7AB4 cards) are required for 533MT/s support (two modules for 400MT/s support). In addition, four P6860 and four P6864 Tektronix probes are required for 533MT/s support (eight P6860 for 400MT/s). Inquire about your specific application or see the Nexus website at <http://www.busboards.com>

8 GHz MagniVu timing and Enhanced iView Analog Mux capability available with either configuration.

Ordering / Contact Information

Please visit our website or contact us for information.

Postal

Nexus Technology, Inc.
PO Box 6575
Nashua, NH 03063

Sales and Technical Support

support@busboards.com

Website

<http://www.busboards.com>

Telephone

TEL: 877-595-8116

Product Website

<http://www.busboards.com/products/memory/ddrii>

Fax

FAX: 877-595-8118

To place an order:

- (1) Credit card orders can be placed directly at (877) 595-8116.
- Or, (2) FAX your purchase order to (877) 595-8118.

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