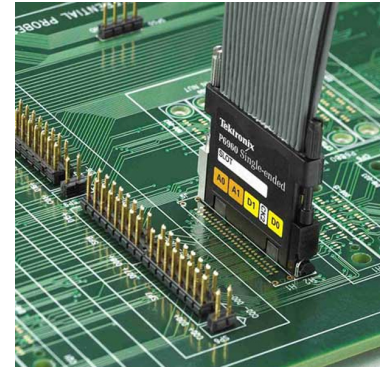


DDR3 Embedded Logic Analyzer Software

Embedded DDR3 Digital & Analog Validation



- Available For All Speeds of DDR3 up to DDR3-1867
- High Speed DDR3 Digital & Analog Validation
- No Hardware to Purchase
- Uses Industry Standard Probes
- Passive 50% Module Reduction w/MR Technology™
- Use When Standard Connector Not Available
- Or, When Direct Probing of Target Board Is Desired
- Automated Logic Analyzer Setup
- DDR3 Protocol Violation Analysis



Direct Target Probing

DDR3 embedded logic analyzer software solutions require direct target probing (sometimes referred to as midbus probing). This requires the customer to route the DDR3 bus signals on their target PCB to Tektronix logic analyzer probe footprints. Nexus Technology can provide recommended probe footprint designs and routing constraints. These routing constraints are critical to ensure proper operation of the DDR3 bus and to ensure the probed data can be acquired and stored by the logic analyzer.

Layout Support

We are available to assist in your design and layout process. We can provide probe footprint recommendations, required probe pin outs and general layout assistance. This information and support is provided at no additional cost.

Supported Tektronix Logic Analyzers

DDR3 embedded logic analyzer software solutions are available for the Tektronix [TLA7000](#), [TLA5000](#) and [TLA700](#) series of logic analyzers. This includes complete support for the [TLA7Axx](#) and [TLA7Bxx](#) series of logic analyzer modules. The following is a partial list of supported TLA modules: [TLA7AB2](#), [TLA7AB3](#), [TLA7AB4](#), [TLA7AC2](#), [TLA7AC3](#), [TLA7AC4](#), [TLA7BC4](#), [TLA7BB2](#), [TLA7BB3](#), and [TLA7BB4](#).

Module Reduction (MR) Technology™

Nexus Technology's Module Reduction Technology™ is available for embedded solutions using Tektronix [TLA7Bxx](#) module(s). Products implementing MR Technology™ allow for full acquisition, including read and write data, while cutting the hardware requirements in half.

Module Reduction Technology™ is a software solution. No qualifier sideband signals are required and no active circuitry is implemented in MR Technology™ which would otherwise force double-probing and increase the load on the DDR3 target.

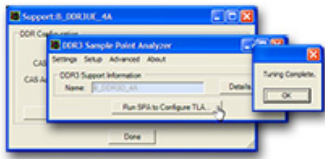
Embedded Logic Analyzer Software

All Nexus Technology DDR3 embedded logic analyzer software supports come with the required logic analyzer setup software, DDR3 protocol decode software, DDR3 data eye sample point analysis software, and a limited version of the protocol violation software. Optional full protocol analysis is available separately.

Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions for easy display and logic analyzer triggering/filtering.

Data Sample Point Analysis Software



In order for the logic analyzer to capture data, the DDR3 signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDR3 data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes are purposely skewed - as per the DDR3

specification - on a byte basis relative to the DDR clock. The valid eyes also contain skew (again relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

These, among other factors, make reliable and accurate DDR3 read and write data bus acquisition extremely difficult - if done manually. [NEX-DDR3-SPA](#), provided free, automates this process enabling quick and reliable DDR3 read and write data bus acquisition in only minutes. For more information, please see the [NEX-DDR3-SPA](#) product page on our website.

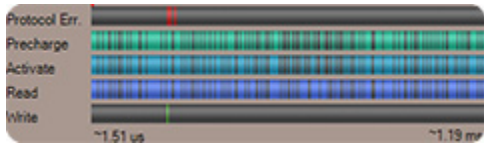
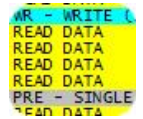
Protocol Violation Software



There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Please see the [NEX-DDR-PROTOCOL](#) product for more information.

Digital Validation

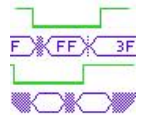
Logic analyzer setup software (TLA support package) is included with these products. This setup software acquires/reconstructs the command/address bus and acquires/reconstructs the read/write data from the data bus. The software also decodes and displays the bus protocol, shows the valid read/write data and provides easy DDR protocol triggering to quickly capture relevant data.



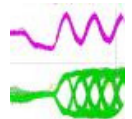
These products also come with the NEX-DDR-PROTOCOL software tool. This software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs basic protocol violation checking. Advanced protocol violation checking is available for purchase separately. Please see the [NEX-DDR-PROTOCOL](#) product for more information on this powerful tool.

Analog Validation

The most readily available tool is the Tektronix Logic Analyzer's 20ps (50GHz) MagniVu timing. This 2.5us deep acquisition space, separate from state acquisition memory is simultaneously acquired with state data, and is typically filled with bus activity that occurred around the state trigger. A wealth of analog information can be found in this data, including: positive/negative pulse widths, signal skew, and data glitches. Activity that appears too short, too long, unreasonably skewed relative to another signal, or that contains glitches are indications that there is an analog characteristic of that signal that deserves further attention.



Another powerful analog validation feature is the Tektronix Logic Analyzer's Analog Mux capability. When paired with an oscilloscope, this feature enables analog visibility of every DDR3 signal probed. Any of the ten or so command bits, sixteen-plus address bits and any of the data bits can be viewed on an oscilloscope in seconds and - literally - with a touch of a button. This feature comes with two significant limitations. First, there is no calibration specification for the channel-to-channel skew through the Analog Mux. Second, the signals are bandwidth limited to 3GHz. This limitation acts as a high speed filter, limiting the visibility of the signal's harmonics that are over 3GHz. For DDR3-1600, this filtering will cause artificial increases in the slew rates which appear as rising/falling edges that take longer to transition. The effect on the data eyes will be similar, showing a rounding effect. Although these limitations force the user to find alternate methods (see our DDR3 Component Interposers) for accurate DDR3-1600 analog validation, the importance of this tool for preliminary analog validation can not be understated. The ability of a digital validation engineer to quickly and easily assess the general analog health of a target can save an enormous amount of time and resources.



Tektronix discusses some of these topics in more detail in the application note, [Debugging Timing Problems with a Logic Analyzer](#) available for download from tek.com. Nexus Technology recommends these products for the debugging methods and practices described in this application note.

Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST.

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