

DDR3/DDR2 Threshold & Sample Point Analyzer

Automated Threshold & Sample Point Setting Software

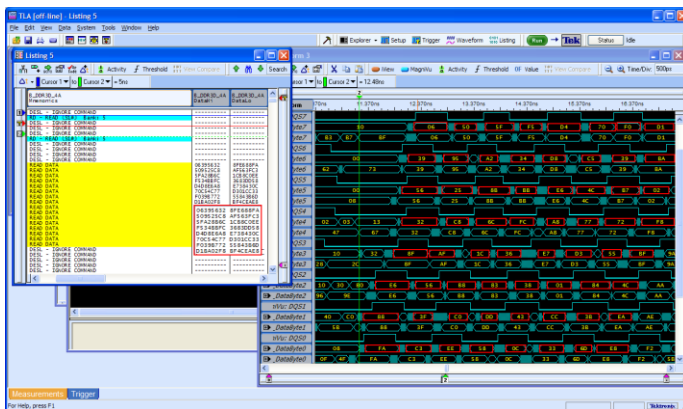


In order for the logic analyzer to capture data, the DDR3 signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDR3 data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes are purposely skewed - as per the DDR3 specification - on a byte basis relative to the DDR clock. The valid eyes also contain skew (again relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

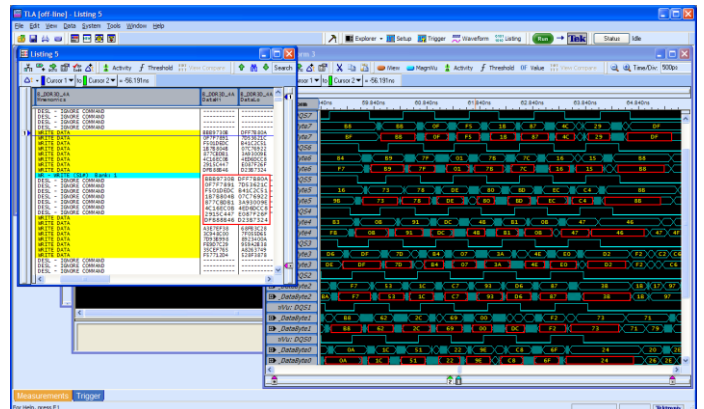
These, among other factors, make reliable and accurate DDR3/DDR2 read and write data bus acquisition extremely difficult - if done manually.

DDR3/DDR2 Sample Point Analyzer software, provided free with every Nexus Technology DDR3/DDR2 TLA7Bxx product, automates this process enabling quick and reliable DDR3/DDR2 read and write data bus acquisition in only minutes.

Performance You Can Trust



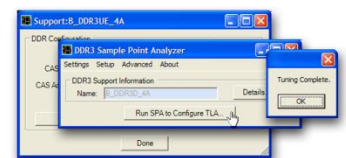
Fully Tuned Acquisition – Read Data



Fully Tuned Acquisition – Write Data

Simple, Automated Interface

This software uses a simple and easy to understand interface to facilitate the setup of the logic analyzer for DDR3 acquisition. After entering the setup parameters needed for analysis, the user is literally two button presses away from a fully setup logic analyzer that is ready for reliable and accurate DDR3 data acquisition.



Under the Hood – Threshold Setting

The fastest speeds of DDR3 and the push to reduce the operating voltages of DDR3 make automated tuning of the logic analyzer digitizing threshold critical for reliable and accurate DDR3 acquisition. Automated tuning also greatly reduces the engineering training time and the logic analyzer setup time for all speeds of DDR3. For a typical DDR3-1600 system, the thresholds are **automatically tuned for**

153 logic analyzer channels (72 read data channels, 72 write data channels, and 9 data strobe channels).

Under the Hood – Sample Position Setting

DDR read and write preambles, postambles, burst lengths, and (most target's) lack of control of the burst data patterns makes automated tuning of the logic analyzer sample positions (setup/hold values) critical for reliable and accurate DDR acquisition. Automated tuning also greatly reduces the engineering training time, the logic analyzer setup time, and the number of acquisitions that must be acquired to perform the tuning. For a typical DDR3-1600 system, the sample positions are **automatically determined for 576 data alignment locations** (72 read data channels, 72 write data channels, each having four sampling locations).

Under the Hood – Channel Tuning

The individual channel tuner provides adjustment of threshold or sample points on a per-channel basis. Current settings are displayed and sample point locations are shown in an intuitive graphical display, along with strobe and clock data to assist in determining where to set values. Multiple channels may be adjusted and re-evaluated by reacquiring data with the TLA and verifying the result.

Tektronix Hardware Requirements

TLA Application software V5.6 and TLA7Bxx modules are required.

Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST/EDT.

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