

## NEX-IBM440GP

Listing 4

C1: 9 C2: 13 Delta Time: 2.01012us Lock Delta Time

Sample	Ibm440GP Address	Ibm440GP DRAMAddr	Ibm440GP RDDatHi	Ibm440GP RDDatLo	Ibm440GP WRDatHi	Ibm440GP WRDatLo	Ibm440GP Mnemonics	Ibm440GP Strobes	Ibm44C WrtMas
12	-----	-----	-----	-----	-----	-----	NOP - NO OPERATION (SO~)	FF	FF
13	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
14	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	FF
15	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	FF
16	00000000	-----	23331323	33313331	-----	-----	READ DATA	FF	FF
	00000000	-----	23331323	-----	-----	-----	subfic r25,r19,0x1323	FF	FF
	00000004	-----	-----	33313331	-----	-----	addic r25,r17,0x3331	FF	FF
17	00000008	-----	33331112	33313331	-----	-----	READ DATA	00	FF
	00000008	-----	33331112	-----	-----	-----	addic r25,r19,0x1112	00	FF
	0000000C	-----	-----	33313331	-----	-----	addic r25,r17,0x3331	00	FF
18	00000010	-----	33013333	3B303111	-----	-----	READ DATA	FF	FF
	00000010	-----	33013333	-----	-----	-----	addic r24,r1,0x3333	FF	FF
	00000014	-----	-----	3B303111	-----	-----	addi r25,r16,0x3111	FF	FF
19	00000018	-----	33333133	33311331	-----	-----	READ DATA	00	FF
	00000018	-----	33333133	-----	-----	-----	addic r25,r19,0x3133	00	FF
	0000001C	-----	-----	33311331	-----	-----	addic r25,r17,0x1331	00	FF
20	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	EB	FF
21	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
22	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
23	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
24	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
25	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
26	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
27	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
28	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
29	-----	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (SO~)	FF	FF
30	-----	00400	-----	-----	-----	-----	WRITE - COL ADDR WRITE (SO~)	FF	FF
31	-----	-----	-----	-----	-----	-----	NOP - NO OPERATION (SO~)	91	FF
32	00000000	-----	-----	-----	23331323	00000000	WRITE DATA	FE	00
33	00000008	-----	-----	-----	-----	-----	WRITE DATA	FF	FF
34	00000010	-----	-----	-----	-----	-----	WRITE DATA	EE	FF
35	00000018	-----	-----	-----	-----	-----	WRITE DATA	FF	FF
36	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	FF
37	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
38	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF

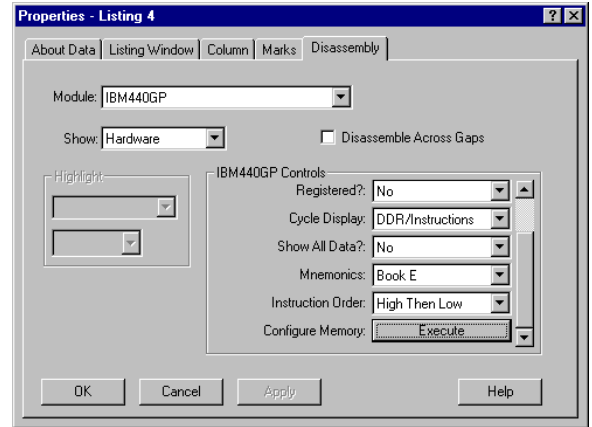
- Quick setup of the Tektronix Logic Analyzer
- Disassembly of IBM440GP data acquired from the DDR bus
- Custom clocking or clock on every edge
- 8GHz timing acquisition on every channel
- Simultaneous state and timing on every channel of the TLA
- Correlation with data from other acquisition modules

The NEX-IBM440GP support is software only.

## General Description

The NEX-IBM440GP support software acquires and decodes IBM440GP bus activity and displays the information in assembly language mnemonics (machine code). This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types to only display data of interest to the software engineers. The user can choose to display the acquired data in Hardware, Software, Control Flow or Subroutine modes.

A major feature of the NEX-IBM440GP software is its ability to intelligently acquire bus cycle information. By taking advantage of the data clocking power built into the Tektronix Logic Analyzer, the support software is able to acquire only the valid IBM440GP bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more microprocessor bus cycles per acquisition. For debug purposes the user also has the ability to override this function and acquire data on every rising clock edge to permit the user to see all of the bus traffic, including the Idle and Wait state.



Every stored cycle (bus or clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 125ps in the TLA7Axx series acquisition modules, permits precise measurements of microprocessor bus activity. Because of the design of the Tektronix Logic Analyzer, there is no need to worry about trading off acquisition memory depth when making these measurements (the timestamp memory is separate from the acquisition memory).

Sample	IBM440GP Address	IBM440GP DRAMAddr	IBM440GP RDAstHi	IBM440GP RDAstLo	IBM440GP WRDAstHi	IBM440GP WRDAstLo	IBM440GP Mnemonics	IBM440GP Strokes	IBM44C Wr/Wa
12	-----	-----	-----	-----	-----	-----	NOP - NO OPERATION (SD-)	FF	FF
13	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
14	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	FF
15	00000000	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	FF
16	00000000	23313323	33313331	-----	-----	-----	READ DATA	FF	FF
00000000	-----	23313323	-----	-----	-----	-----	add1c r25,r19,0x3323	FF	FF
00000004	-----	-----	33313331	-----	-----	-----	add1c r25,r17,0x3331	FF	FF
17	00000008	-----	33311112	33313331	-----	-----	READ DATA	00	FF
00000008	-----	-----	33311112	-----	-----	-----	add1c r25,r19,0x1112	00	FF
0000000C	-----	-----	-----	33313331	-----	-----	add1c r25,r17,0x3331	00	FF
18	00000010	-----	33013333	38303111	-----	-----	READ DATA	FF	FF
00000010	-----	-----	33013333	-----	-----	-----	add1c r24,r1,0x3333	FF	FF
00000014	-----	-----	-----	38303111	-----	-----	add1 r25,r16,0x3111	FF	FF
19	00000018	-----	33331333	33311331	-----	-----	READ DATA	00	FF
00000018	-----	-----	33331333	-----	-----	-----	add1c r25,r19,0x3133	00	FF
0000001C	-----	-----	-----	33311331	-----	-----	DESL - IGNORE COMMAND	00	FF
20	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
21	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
22	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
23	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
24	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
25	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
26	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
27	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
28	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
29	-----	000000	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
30	-----	004000	-----	-----	-----	-----	WRITE - COL ADDR WRITE (SD-)	FF	FF
31	-----	-----	-----	-----	-----	-----	NOP - NO OPERATION (SD-)	91	FF
32	00000000	-----	-----	23313323	00000000	-----	WRITE DATA	00	FF
33	00000008	-----	-----	-----	-----	-----	WRITE DATA	FF	FF
34	00000010	-----	-----	-----	-----	-----	WRITE DATA	FF	FF
35	00000018	-----	-----	-----	-----	-----	WRITE DATA	FF	FF
36	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	FF
37	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF
38	-----	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF

## Connecting the TLA700 to an IBM440GP Target

When installed on a TLA700 the NEX-IBM440GP software provides quick and easy setup of the TLA and disassembly of the acquired IBM440GP data.

The logic analyzer can be connected to the DDR interface on a target by using an adapter available from Nexus Technology or by designing the interface directly into the target.

If a DDR DIMM adapter is used as the interface then the NEX-DDRHS or NEX-DDRHSM product from Nexus Technology may be used to acquire data.

If the interface will be designed directly onto the target then a required pinout must be followed. Please contact us for this information.

**Important:** Specific wiring must be followed when routing the IBM440GP DDR signals to mictor or compression pads if this support is to be used.

## LA Support / Configuration

The required Tektronix Logic Analyzer configuration depends on the DDR memory interface of the target. For all configurations, the TLA application software must be V4.2 or later.

To support a **200MT/s** SDRAM memory interface to the microprocessor – two merged TLA7AA4 or TLA7AB4, 136-channel, 235MHz (minimum) state speed acquisition modules are required. Probing options can vary.

To support a **266MT/s or faster** SDRAM memory interface to the microprocessor – two merged TLA7AA4 or TLA7AB4, 136-channel, 450MHz state speed acquisition modules are required. Eight P6860 compression probes are also required.

If compression pad connections have not been designed into the target and DDR DIMM memory is being used, then an NEX-DDRHS or NEX-DDRHSM adapter is recommended to enable acquisition of the necessary signals for disassembly.

## Ordering / Contact Information

**Part Number** NEX-IBM440GP

Includes:     Software  
              Manual

**Options** include  
              NEX-DDRHS or NEX-DDRHSM

**Postal:**     Nexus Technology, Inc.  
              78 Northeastern Blvd. #2  
              Nashua, NH 03062

**Telephone:** 877-595-8116

**Fax:**        877-595-8118

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              quotes@nexustechnology.com  
              techsupport@nexustechnology.com

**Website:**   www.nexustechnology.com

### Placing an Order

Credit Card orders can be placed directly at 877-595-8116.  
Purchase orders can be faxed to 877-595-8118.

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