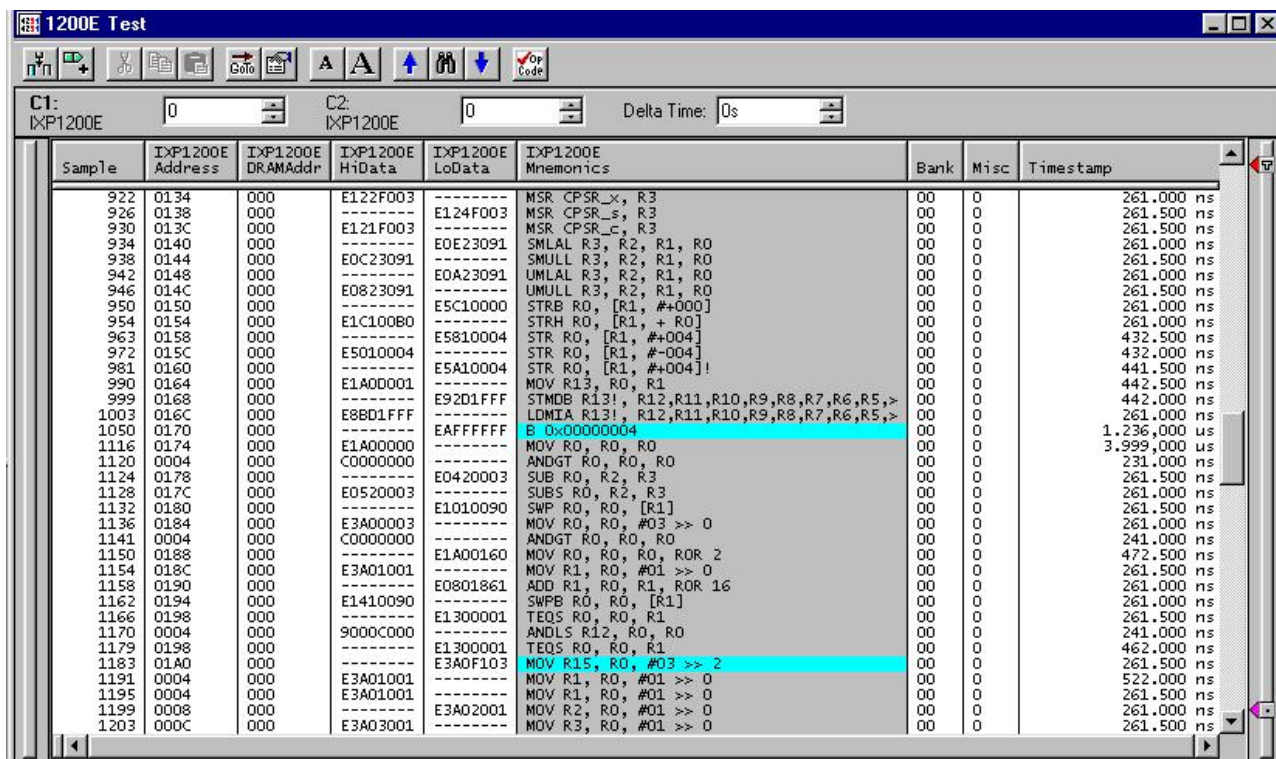


## NEX-IXP1200



Sample	IXP1200E Address	IXP1200E DRAMAddr	IXP1200E HiData	IXP1200E LoData	IXP1200E Mnemonics	Bank	Misc	Timestamp
922	0134	000	E122F003	-----	MSR CPSR_x, R3	00	0	261.000 ns
926	0138	000	-----	E124F003	MSR CPSR_s, R3	00	0	261.500 ns
930	013C	000	E121F003	-----	MSR CPSR_c, R3	00	0	261.500 ns
934	0140	000	-----	E0E23091	SMLAL R3, R2, R1, RO	00	0	261.000 ns
938	0144	000	E0C23091	-----	SMULL R3, R2, R1, RO	00	0	261.500 ns
942	0148	000	-----	E0A23091	UMLAL R3, R2, R1, RO	00	0	261.000 ns
946	014C	000	E0823091	-----	UMULL R3, R2, R1, RO	00	0	261.500 ns
950	0150	000	-----	E5C10000	STRB RO, [R1, #+000]	00	0	261.000 ns
954	0154	000	E1C100B0	-----	STRH RO, [R1, + RO]	00	0	261.000 ns
963	0158	000	-----	E5810004	STR RO, [R1, #+004]	00	0	432.500 ns
972	015C	000	E5010004	-----	STR RO, [R1, #-004]	00	0	432.000 ns
981	0160	000	-----	E5A10004	STR RO, [R1, #-004]!	00	0	441.500 ns
990	0164	000	E1A00001	-----	MOV R13, RO, R1	00	0	442.500 ns
999	0168	000	-----	E92D1FFF	STMDB R13!, R12,R11,R10,R9,R8,R7,R6,R5,>	00	0	442.000 ns
1003	016C	000	E8BD1FFF	-----	LDMIA R13!, R12,R11,R10,R9,R8,R7,R6,R5,>	00	0	261.000 ns
1050	0170	000	-----	EFFFFFFF	B 0x00000004	00	0	1.236.000 us
1116	0174	000	E1A00000	-----	MOV RO, RO, RO	00	0	3.999.000 us
1120	0004	000	C0000000	-----	ANDGT RO, RO, RO	00	0	231.000 ns
1124	0178	000	-----	E0420003	SUB RO, R2, R3	00	0	261.500 ns
1128	017C	000	E0520003	-----	SUBS RO, R2, R3	00	0	261.000 ns
1132	0180	000	-----	E1010090	SWP RO, RO, [R1]	00	0	261.500 ns
1136	0184	000	E3A00003	-----	MOV RO, RO, #03 >> 0	00	0	261.000 ns
1141	0004	000	C0000000	-----	ANDGT RO, RO, RO	00	0	241.000 ns
1150	0188	000	E1A00160	-----	MOV RO, RO, RO, ROR 2	00	0	472.500 ns
1154	018C	000	E3A01001	-----	MOV R1, RO, #01 >> 0	00	0	261.500 ns
1158	0190	000	-----	E0801861	ADD R1, RO, R1, ROR 16	00	0	261.000 ns
1162	0194	000	E1410090	-----	SWPB RO, RO, [R1]	00	0	261.000 ns
1166	0198	000	-----	E1300001	TEQS RO, RO, R1	00	0	261.500 ns
1170	0004	000	9000C000	-----	ANDLS R12, RO, RO	00	0	241.000 ns
1179	0198	000	-----	E1300001	TEQS RO, RO, R1	00	0	462.000 ns
1183	01A0	000	-----	E3A0F103	MOV R15, RO, #03 >> 2	00	0	261.500 ns
1191	0004	000	E3A01001	-----	MOV R1, RO, #01 >> 0	00	0	522.000 ns
1195	0004	000	E3A01001	-----	MOV R1, RO, #01 >> 0	00	0	261.500 ns
1199	0008	000	-----	E3A02001	MOV R2, RO, #01 >> 0	00	0	261.000 ns
1203	000C	000	E3A03001	-----	MOV R3, RO, #01 >> 0	00	0	261.500 ns

- Quick setup of the Logic Analyzer
- Disassembly of the acquired IXP1200 data
- Custom clocking or Clock on every edge
- 8GHz Timing acquisition on every channel

When installed on the TLA600 or TLA700 the NEX-IXP1200 software provides quick and easy setup of the TLA and disassembly of the acquired IXP1200 data.

## General Description

The NEX-IXP1200 support is software only. Please see below for information on probing.

### Connecting the TLA600/700 to a IXP1200 target

When possible it is recommended that the user add Mictor connectors to their target for the interface to the TLA600/700 using Tektronix P6434/P6860 high-density probes.

**IMPORTANT:** Specific wiring must be followed when routing the IXP1200 signals to Mictor connectors if the NEX-IXP1200 support is going to be used. Table 2 shows this pinout.

### Disassembly Features

Identification / Support of the following:

- RAS/CAS Address Reconstruction
- Architecture v4 Level Instructions and Addressing modes
- Load data read cycle detection
- LDM and LDC multiple load read cycle detection
- Branch Prefetch Instruction flush detection

**Support for the following IXP1200 modes:** Number of Row Bits, Number of Column Bits, High/Low Instruction and Suppress SDRAM cycles

### Number of Row Bits and Number of Column Bits

The IXP1200 microprocessor supports the use of DRAM for code execution memory. However, because DRAM is accessed by Row and Column address cycles it becomes necessary to translate those two cycles into a physical address equivalent which is necessary for tracking the flow of program code. The Address group is used by the IXP1200 support to reconstruct the physical address from Row and Column information contained in the DRAMAddr group. The DRAMAddr group in the IXP1200 support is configured by default for 13 Row and 10 Column address bits. The number of bits used in this group may need to be adjusted to reflect a given target. The disassembler supports 13, 12 or 11 RAS bits and 10, 9 or 8 CAS bits. These settings determine how the Physical address is reconstructed into the Address display group. A DOS executable named Readdress.exe is present on the installation diskette (although it is not automatically installed). This executable will encode and decode between RAS/CAS bits and a Physical address and is included for convenience.

### High/Low Instruction

Because the IXP1200 microprocessor acquires two instructions in each fetch, the IXP1200 support contains a mode for controlling how these values are displayed. If the choice "Both" is selected, then high and low instructions are displayed. If the choice "Low then High" is selected, then the Low instruction is displayed during the first fetch at a given 64 bit location. The High instruction is displayed during the next fetch to the same location.

### Suppress SDRAM cycles

Because the IXP1200 microprocessor support acquires all cycle types, RAS, CAS and PRECHARGE cycles will be interspersed with instruction reads, data reads and data writes. When "Suppress SDRAM cycles" mode is set to "Display", all cycles are visible. Setting "Suppress SDRAM cycles" to "Suppress" will display only instruction, data read and data write cycles

## All five addressing modes are supported:

### Addressing Mode 1

- Shifter operands
- Immediate
- Register
- Logical shift left by immediate
- Logical shift left by register
- Logical shift right by immediate
- Logical shift right by register
- Arithmetic shift right by immediate
- Arithmetic shift right by register
- Rotate right by immediate
- Rotate right by register
- Rotate right with extend

### Addressing Mode 2

- Immediate offset
- Register offset
- Scaled register offset
- Immediate pre-indexed
- Register pre-indexed
- Scaled register pre-indexed
- Immediate post-indexed
- Register post-indexed
- Scaled register post-indexed

### Addressing Mode 3

- Immediate offset
- Register offset
- Immediate pre-indexed
- Register pre-indexed
- Immediate post-indexed
- Register post-indexed

### Addressing Mode 4

- Increment after
- Increment before
- Decrement after
- Decrement before

### Addressing Mode 5

- Immediate offset
- Immediate pre-indexed
- Immediate post-indexed

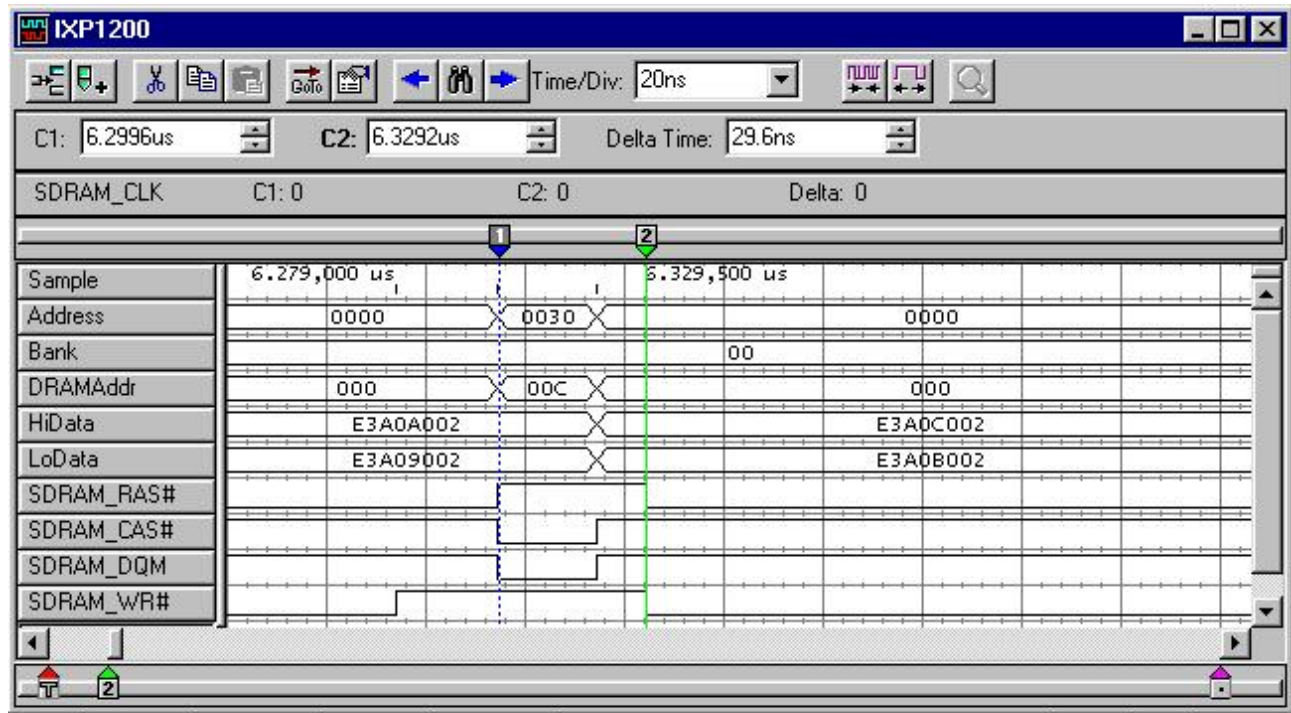
## IXP1200 Instructions Supported

- ADC                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- ADD                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- AND                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- B{L}                    {<cond>} <target address>
- BIC                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- BX                     {<cond>} Rm
- CDP                    {<cond>} p<cp#>, <opcode\_1>, CRd, CRn, CRm, <opcode\_2>
- CMN                    {<cond>} Rn, <shifter\_operand>
- CMP                    {<cond>} Rn, <shifter\_operand>
- EOR                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- LDC                    {<cond>} p<cp\_num>, CRd, <addressing\_mode>
- LDM                    {<cond>} <addressing\_mode> Rn{!}, <registers>                    LDM(1)
- LDM                    {<cond>} <addressing\_mode> Rn, <registers>^                    LDM(2)
- LDM                    {<cond>} <addressing\_mode> Rn{!}, <registers\_and\_pc>^            LDM(3)
- LDR                    {<cond>} Rd, <addressing\_mode>
- LDR                    {<cond>}B Rd, <addressing\_mode>
- LDR                    {<cond>}BT Rd, <post\_indexed\_addressing\_mode>
- LDR                    {<cond>}H Rd, <addressing\_mode>
- LDR                    {<cond>}SB Rd, <addressing\_mode>
- LDR                    {<cond>}SH Rd, <addressing\_mode>
- LDR                    {<cond>}T Rd, <post\_indexed\_addressing\_mode>
- MCR                    {<cond>} p<cp#>, <opcode\_1>, Rd, CRn, CRm, <opcode\_2>
- MLA                    {<cond>}{<S>} Rd, Rm, Rs, Rn
- MOV                    {<cond>}{S} Rd, <shifter\_operand>
- MRC                    {<cond>} p<cp#>, <opcode\_1>, Rd, CRn, CRm, <opcode\_2>
- MRS                    {<cond>} Rd, CPSR
- MRS                    {<cond>} Rd, SPSR
- MSR                    {<cond>} Rd, CPSR\_f, #32bit immediate
- MSR                    {<cond>} Rd, CPSR\_<fields>, Rm
- MSR                    {<cond>} Rd, SPSR\_f, #32bit immediate
- MSR                    {<cond>} Rd, SPSR\_<fields>, Rm
- MUL                    {<cond>}{<S>}Rd, Rm, Rs
- MVN                    {<cond>}{<S>} Rd, <shifter\_operand>
- ORR                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- RSB                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- RSC                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- SBC                    {<cond>}{S} Rd, Rn, <shifter\_operand>
- SMLAL    {<cond>}{<S>} RdLo, RdHi, Rm, Rs
- SMULL    {<cond>}{<S>} RdLo, RdHi, Rm, Rs
- STC                    {<cond>} p<cp\_num>, CRd, <addressing\_mode>
- STM                    {<cond>} <addressing\_mode> Rn{!}, <registers>                    STM(1)
- STM                    {<cond>} <addressing\_mode> Rn{!}, <registers>^                STM(2)

## IXP1200 Instructions Supported (cont'd)

- STR            {<cond>} Rd, <addressing\_mode>
- STR            {<cond>}B Rd, <addressing\_mode>
- STR            {<cond>}BT Rd, <post\_indexed\_addressing\_mode>
- STR            {<cond>}H Rd, <addressing\_mode>
- STR            {<cond>}T Rd, <post\_indexed\_addressing\_mode>
- SUB            {<cond>}{<S>} Rd, Rn, <shifter\_operand>
- SWI            {<cond>} <24\_bit\_immediate>
- SWP            {<cond>} Rd, Rm, [Rn]
- SWP            {<cond>}B Rd, Rm, [Rn]
- TEQ            {<cond>} Rn, <shifter\_operand>
- TST            {<cond>} Rn, <shifter\_operand>
- UMLAL        {<cond>}{<S>} RdLo, RdHi, Rm, Rs
- UMULL        {<cond>}{<S>} RdLo, RdHi, Rm, Rs

## Timing Display



## IXP1200 TLA600/700 Wiring

Group Name	Signal Name	IXP1200 Pin #	TLA700 input	Group Name	Signal Name	IXP1200 Pin #	TLA700 input
HiData (Hex)	MDATA63		A3:7	LoData (Hex)	MDATA31		D3:7
	MDATA62		A3:6		MDATA30		D3:6
	MDATA61		A3:5		MDATA29		D3:5
	MDATA60		A3:4		MDATA28		D3:4
	MDATA59		A3:3		MDATA27		D3:3
	MDATA58		A3:2		MDATA26		D3:2
	MDATA57		A3:1		MDATA25		D3:1
	MDATA56		A3:0		MDATA24		D3:0
	MDATA55		A2:7		MDATA23		D2:7
	MDATA54		A2:6		MDATA22		D2:6
	MDATA53		A2:5		MDATA21		D2:5
	MDATA52		A2:4		MDATA20		D2:4
	MDATA51		A2:3		MDATA19		D2:3
	MDATA50		A2:2		MDATA18		D2:2
	MDATA49		A2:1		MDATA17		D2:1
	MDATA48		A2:0		MDATA16		D2:0
	MDATA47		A1:7		MDATA15		D1:7
	MDATA46		A1:6		MDATA14		D1:6
	MDATA45		A1:5		MDATA13		D1:5
	MDATA44		A1:4		MDATA12		D1:4
	MDATA43		A1:3		MDATA11		D1:3
	MDATA42		A1:2		MDATA10		D1:2
	MDATA41		A1:1		MDATA9		D1:1
	MDATA40		A1:0		MDATA8		D1:0
	MDATA39		A0:7		MDATA7		D0:7
	MDATA38		A0:6		MDATA6		D0:6
	MDATA37		A0:5		MDATA5		D0:5
	MDATA36		A0:4		MDATA4		D0:4
	MDATA35		A0:3		MDATA3		D0:3
	MDATA34		A0:2		MDATA2		D0:2
	MDATA33		A0:1		MDATA1		D0:1
	MDATA32		A0:0		MDATA0		D0:0
	Address (Hex) Synthesized	---	---		---	DRAMAddr	MADR[13]
---		---	---	MADR[12]			C1:6
---		---	---	MADR[11]			C3:7
Control (Sym)	RAS#		C2:0	MADR[10]			C3:6
	CAS#		C2:1	MADR[9]			C3:5
	DQM		C2:3	MADR[8]			C3:4
	WE#		C2:2	MADR[7]			C3:3
Misc (Bin)	SDCLK		Clock:3	MADR[6]			C3:2
	PARITY		C0:0	MADR[5]			C3:1
				MADR[4]			C3:0
				MADR[3]			C2:7
				MADR[2]			C2:6
				MADR[1]			C2:5
				MADR[0]		C2:4	
			DRAM_A1	ground	C0:3		
			DRAM_A0	ground	C0:2		

## NEX-IXP1200 Mictor Pinout

Tek Mictor Pin #	AMP Mictor Pin #	TLA600 / TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #
3	5	CLK:0			36	6	CLK:1		
4	7	A3:7	MDATA[63]	AH6	35	8	A1:7	MDATA[47]	AE2
5	9	A3:6	MDATA[62]	AJ5	34	10	A1:6	MDATA[46]	AE1
6	11	A3:5	MDATA[61]	AL4	33	12	A1:5	MDATA[45]	U4
7	13	A3:4	MDATA[60]	AK4	32	14	A1:4	MDATA[44]	V2
8	15	A3:3	MDATA[59]	AH5	31	16	A1:3	MDATA[43]	U3
9	17	A3:2	MDATA[58]	AH2	30	18	A1:2	MDATA[42]	U2
10	19	A3:1	MDATA[57]	AH1	29	20	A1:1	MDATA[41]	U1
11	21	A3:0	MDATA[56]	AG3	28	22	A1:0	MDATA[40]	T4
12	23	A2:7	MDATA[55]	AF4	27	24	A0:7	MDATA[39]	T3
13	25	A2:6	MDATA[54]	AG2	26	26	A0:6	MDATA[38]	T2
14	27	A2:5	MDATA[53]	AG1	25	28	A0:5	MDATA[37]	T1
15	29	A2:4	MDATA[52]	AF3	24	30	A0:4	MDATA[36]	R3
16	31	A2:3	MDATA[51]	AF2	23	32	A0:3	MDATA[35]	R4
17	33	A2:2	MDATA[50]	AF1	22	34	A0:2	MDATA[34]	P2
18	35	A2:1	MDATA[49]	AE3	21	36	A0:1	MDATA[33]	P3
19	37	A2:0	MDATA[48]	AD4	20	38	A0:0	MDATA[32]	N1

### Mictor Group A

Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #
3	5	CLK:3	SDCLK	AD2	36	6	QUAL:1	do not use	---
4	7	C3:7	MADR[11]	AC2	35	8	C1:7	MADR[13]	AD1
5	9	C3:6	MADR[10]	AC1	34	10	C1:6	MADR[12]	AC3
6	11	C3:5	MADR[9]	AB3	33	12	C1:5	do not use	---
7	13	C3:4	MADR[8]	AA4	32	14	C1:4	do not use	---
8	15	C3:3	MADR[7]	AB2	31	16	C1:3	do not use	---
9	17	C3:2	MADR[6]	AB1	30	18	C1:2	do not use	---
10	19	C3:1	MADR[5]	AA3	29	20	C1:1	do not use	---
11	21	C3:0	MADR[4]	AA1	28	22	C1:0	do not use	---
12	23	C2:7	MADR[3]	Y3	27	24	C0:7	do not use	---
13	25	C2:6	MADR[2]	W4	26	26	C0:6	do not use	---
14	27	C2:5	MADR[1]	Y2	25	28	C0:5	do not use	---
15	29	C2:4	MADR[0]	Y1	24	30	C0:4	do not use	---
16	31	C2:3	DQM	V3	23	32	C0:3		
17	33	C2:2	WE#	W1	22	34	C0:2		
18	35	C2:1	CAS#	W3	21	36	C0:1		
19	37	C2:0	RAS#	W2	20	38	C0:0	PARITY	AK5

### Mictor Group C

## NEX-IXP1200 Mictor Pinout (cont'd)

Tek Mictor Pin #	AMP Mictor Pin #	TLA600 / TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #
3	5	QUAL:0	do not use	---	36	6	CLK:2		
4	7	D3:7	MDATA[31]	N2	35	8	D1:7	MDATA[15]	H2
5	9	D3:6	MDATA[30]	N3	34	10	D1:6	MDATA[14]	J4
6	11	D3:5	MDATA[29]	M1	33	12	D1:5	MDATA[13]	H3
7	13	D3:4	MDATA[28]	M2	32	14	D1:4	MDATA[12]	G1
8	15	D3:3	MDATA[27]	N4	31	16	D1:3	MDATA[11]	G2
9	17	D3:2	MDATA[26]	M3	30	18	D1:2	MDATA[10]	H4
10	19	D3:1	MDATA[25]	L1	29	20	D1:1	MDATA[9]	G3
11	21	D3:0	MDATA[24]	L2	28	22	D1:0	MDATA[8]	F1
12	23	D2:7	MDATA[23]	M4	27	24	D0:7	MDATA[7]	F2
13	25	D2:6	MDATA[22]	L3	26	26	D0:6	MDATA[6]	F3
14	27	D2:5	MDATA[21]	K1	25	28	D0:5	MDATA[5]	E1
15	29	D2:4	MDATA[20]	K3	24	30	D0:4	MDATA[4]	E2
16	31	D2:3	MDATA[19]	J1	23	32	D0:3	MDATA[3]	F4
17	33	D2:2	MDATA[18]	J2	22	34	D0:2	MDATA[2]	E3
18	35	D2:1	MDATA[17]	J3	21	36	D0:1	MDATA[1]	D1
19	37	D2:0	MDATA[16]	H1	20	38	D0:0	MDATA[0]	D2

### Mictor Group D

## NEX-IXP1200 Compression Pinout

Pad P3-PH2	Input	IXP1200 Signal Name	IXP1200 Pin #
A15	CK0-		
A13	CK0+		
B12	A3:7	MDATA[63]	AH6
B10	A3:6	MDATA[62]	AJ5
A12	A3:5	MDATA[61]	AL4
A10	A3:4	MDATA[60]	AK4
B9	A3:3	MDATA[59]	AH5
B7	A3:2	MDATA[58]	AH2
A9	A3:1	MDATA[57]	AH1
A7	A3:0	MDATA[56]	AG3
B6	A2:7	MDATA[55]	AF4
B4	A2:6	MDATA[54]	AG2
A6	A2:5	MDATA[53]	AG1
A4	A2:4	MDATA[52]	AF3
B3	A2:3	MDATA[51]	AF2
B1	A2:2	MDATA[50]	AF1
A3	A2:1	MDATA[49]	AE3
A1	A2:0	MDATA[48]	AD4

Pad P3-PH1	Input	IXP1200 Signal Name	IXP1200 Pin #
A15	Q0-		
A13	Q0+	do not use	---
B12	D3:7	MDATA[31]	N2
B10	D3:6	MDATA[30]	N3
A12	D3:5	MDATA[29]	M1
A10	D3:4	MDATA[28]	M2
B9	D3:3	MDATA[27]	N4
B7	D3:2	MDATA[26]	M3
A9	D3:1	MDATA[25]	L1
A7	D3:0	MDATA[24]	L2
B6	D2:7	MDATA[23]	M4
B4	D2:6	MDATA[22]	L3
A6	D2:5	MDATA[21]	K1
A4	D2:4	MDATA[20]	K3
B3	D2:3	MDATA[19]	J1
B1	D2:2	MDATA[18]	J2
A3	D2:1	MDATA[17]	J3
A1	D2:0	MDATA[16]	H1

## NEX-IXP1200 Compression Pinout (Cont'd)

Pad P2-PH2	Input	IXP1200 Signal Name	IXP1200 Pin #
A15	CK1-		
A13	CK1+		
B12	A1:7	MDATA[47]	AE2
B10	A1:6	MDATA[46]	AE1
A12	A1:5	MDATA[45]	U4
A10	A1:4	MDATA[44]	V2
B9	A1:3	MDATA[43]	U3
B7	A1:2	MDATA[42]	U2
A9	A1:1	MDATA[41]	U1
A7	A1:0	MDATA[40]	T4
B6	A0:7	MDATA[39]	T3
B4	A0:6	MDATA[38]	T2
A6	A0:5	MDATA[37]	T1
A4	A0:4	MDATA[36]	R3
B3	A0:3	MDATA[35]	R4
B1	A0:2	MDATA[34]	P2
A3	A0:1	MDATA[33]	P3
A1	A0:0	MDATA[32]	N1

Pad P2-PH1	Input	IXP1200 Signal Name	IXP1200 Pin #
A15	CK2-		
A13	CK2+		
B12	D1:7	MDATA[15]	H2
B10	D1:6	MDATA[14]	J4
A12	D1:5	MDATA[13]	H3
A10	D1:4	MDATA[12]	G1
B9	D1:3	MDATA[11]	G2
B7	D1:2	MDATA[10]	H4
A9	D1:1	MDATA[9]	G3
A7	D1:0	MDATA[8]	F1
B6	D0:7	MDATA[7]	F2
B4	D0:6	MDATA[6]	F3
A6	D0:5	MDATA[5]	E1
A4	D0:4	MDATA[4]	E2
B3	D0:3	MDATA[3]	F4
B1	D0:2	MDATA[2]	E3
A3	D0:1	MDATA[1]	D1
A1	D0:0	MDATA[0]	D2

Pad P1-PH2	Input	IXP1200 Signal Name	IXP1200 Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	SDCLK	AD2
B12	C3:7	MADR[11]	AC2
B10	C3:6	MADR[10]	AC1
A12	C3:5	MADR[9]	AB3
A10	C3:4	MADR[8]	AA4
B9	C3:3	MADR[7]	AB2
B7	C3:2	MADR[6]	AB1
A9	C3:1	MADR[5]	AA3
A7	C3:0	MADR[4]	AA1
B6	C2:7	MADR[3]	Y3
B4	C2:6	MADR[2]	W4
A6	C2:5	MADR[1]	Y2
A4	C2:4	MADR[0]	Y1
B3	C2:3	DQM	V3
B1	C2:2	WE#	W1
A3	C2:1	CAS#	W3
A1	C2:0	RAS#	W2

Pad P1-PH1	Input	IXP1200 Signal Name	IXP1200 Pin #
A15	Q1-		
A13	Q1+	do not use	---
B12	C1:7	MADR[13]	AD1
B10	C1:6	MADR[12]	AC3
A12	C1:5	do not use	---
A10	C1:4	do not use	---
B9	C1:3	do not use	---
B7	C1:2	do not use	---
A9	C1:1	do not use	---
A7	C1:0	do not use	---
B6	C0:7	do not use	---
B4	C0:6	do not use	---
A6	C0:5	do not use	---
A4	C0:4	do not use	---
B3	C0:3		
B1	C0:2		
A3	C0:1		
A1	C0:0	PARITY	AK5

## TLA700 system requirements

TLA600 or TLA700 with a TLA7x3 or TLA7x4 (102 channel card min.). Because of the setup/hold specifications of the IXP1200, support is not available for the DAS9200 or TLA5x0.

## Ordering / Contact Information

**Part Number** NEX-IXP1200

**Includes:** Software to setup/configure the TLA700  
IXP1200 disassembly software for the TLA700 on 3 ½" Diskette  
Manual

**Postal:** Nexus Technology, Inc.  
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Nashua, NH 03062

**Telephone:** 877-595-8116

**Fax:** 877-595-8118

**Email:** support@nexustechnology.com  
quotes@nexustechnology.com  
techsupport@nexustechnology.com

**Website:** [www.nexustechnology.com](http://www.nexustechnology.com)

## Placing an Order

Credit Card orders can be placed directly at 877-595-8116.  
Purchase orders can be faxed to 877-595-8118.

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