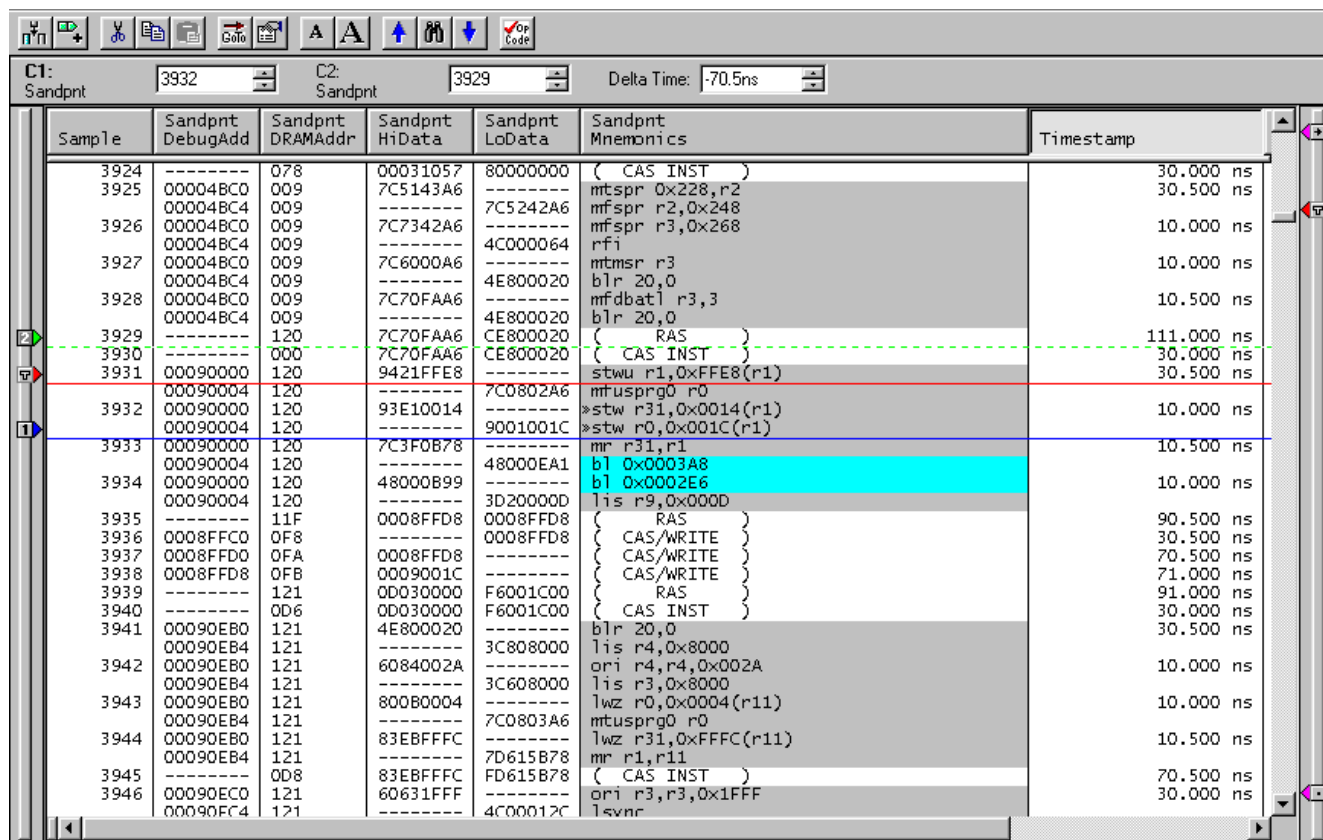


NEX-MPC824X



Sample	Sandpnt DebugAddr	Sandpnt DRAMAddr	Sandpnt HiData	Sandpnt LoData	Sandpnt Mnemonics	Timestamp
3924	-----	078	00031057	80000000	{ CAS INST }	30.000 ns
3925	00004BC0	009	7C5143A6	-----	mtspr 0x228,r2	30.500 ns
3926	00004BC0	009	7C7342A6	-----	mfspir r2,0x248	10.000 ns
3927	00004BC0	009	7C6000A6	-----	mfspir r3,0x268	10.000 ns
3928	00004BC0	009	7C70FAA6	-----	rfi	10.000 ns
3929	00004BC0	009	7C70FAA6	-----	mtmsr r3	10.000 ns
3930	00004BC4	009	7C70FAA6	-----	blr 20,0	10.500 ns
3931	00090000	120	9421FFE8	-----	mfdbat1 r3,3	10.500 ns
3932	00090004	120	93E10014	-----	blr 20,0	111.000 ns
3933	00090000	120	7C3F0B78	-----	{ CAS INST }	30.000 ns
3934	00090004	120	48000B99	-----	stwu r1,0xFFE8(r1)	30.500 ns
3935	00090004	120	0008FFD8	-----	mfusprg0 r0	10.000 ns
3936	0008FFC0	0F8	0008FFD8	-----	>stw r31,0x0014(r1)	10.000 ns
3937	0008FFD0	0FA	0008FFD8	-----	>stw r0,0x001C(r1)	10.500 ns
3938	0008FFD8	0FB	0008FFD8	-----	mr r31,r1	10.000 ns
3939	-----	121	0D030000	F6001C00	b1 0x0003A8	10.000 ns
3940	-----	0D6	0D030000	F6001C00	b1 0x0002E6	10.000 ns
3941	00090E80	121	4E800020	-----	lis r9,0x000D	90.500 ns
3942	00090E84	121	3C808000	-----	{ CAS/WRITE }	30.500 ns
3943	00090E80	121	6084002A	-----	{ CAS/WRITE }	70.500 ns
3944	00090E84	121	800B0004	-----	{ CAS/WRITE }	71.000 ns
3945	00090E80	121	83EBFFFC	-----	{ CAS/WRITE }	91.000 ns
3946	00090E84	121	7D615B78	-----	{ CAS INST }	30.000 ns
3947	00090E80	121	83EBFFFC	-----	{ CAS INST }	30.000 ns
3948	00090E84	121	FD615B78	-----	blr 20,0	30.500 ns
3949	00090EC0	121	60631FFF	-----	lis r4,0x8000	10.000 ns
3950	00090FC4	121	4C00012C	-----	ori r4,r4,0x002A	10.000 ns
3951	-----	-----	-----	-----	lis r3,0x8000	10.000 ns
3952	-----	-----	-----	-----	lwz r0,0x0004(r11)	10.000 ns
3953	-----	-----	-----	-----	mtusprg0 r0	10.500 ns
3954	-----	-----	-----	-----	lwz r31,0xFFFF(r11)	10.500 ns
3955	-----	-----	-----	-----	mr r1,r11	70.500 ns
3956	-----	-----	-----	-----	{ CAS INST }	30.000 ns
3957	-----	-----	-----	-----	ori r3,r3,0x1FFF	30.000 ns
3958	-----	-----	-----	-----	lsync	-----

- Quick setup of the Logic Analyzer
- Disassembly of the acquired MPC824X data when running from SDRAM*
- Includes software support for embedded MPC824X designs and the Motorola Sandpoint evaluation board
- Physical Address Reconstruction
- 8GHz Timing acquisition on every channel

*824X refers to the 8240, 8241 and 8245. Please call for information on supporting DRAM, SRAM (if used for 64-bit code fetches), Debug address and 8-bit boot code.

General Description

When installed on the TLA600 or TLA700, the NEX-MPC824X software provides quick and easy setup of the TLA600/700 and disassembly of the acquired MPC824X data.

The NEX-MPC824X support is software only. Please see below for information on connecting to a target.

Connecting the TLA600/700 to a MPC824X target

When possible it is recommended that the user add Mictor connectors to their target for the interface to the TLA600/700 using Tektronix P6434/P6860 high-density probes.

IMPORTANT: Specific wiring must be followed when routing the MPC824X signals to Mictor connectors if the NEX-MPC824X support is going to be used. Please refer to the Mictor Pinout for this.

Sandpoint Evaluation Board Support

The Motorola Sandpoint evaluation board has mictor connectors for connecting to a logic analyzer. However, in order for our Sandpoint support package to function properly several signals must be moved using two New Wave NEX-HDSWIZ adapters. One HDSWIZ is used with the TLA's 'E' Mictor cable; the second is used with the 'C' Mictor probe.

Hardware Adapter for connecting to the MPC8240

If a hardware adapter is needed to connect the TLA600/700 logic analyzer to the MPC8240 micro please contact NEW WAVE for a recommended adapter vendor.

Disassembly Features

General

The NEX-824X support software acquires and decodes Motorola MPC824X bus activity* and displays the information as assembly language mnemonics (machine code). This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types of interest to the software engineer. The user can choose to display the acquired data in Hardware, Software, Control Flow, or Subroutine modes.

A major feature of the NEX-824X software is its ability to intelligently acquire bus cycle information. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the support software is able to acquire only the valid MPC8240 bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more microprocessor bus cycles. For debug purposes the user also has the ability to override this function and acquire data on every Rising CLK Edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Every stored cycle (bus or clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 125ps in the TLA600/700 series, permits precise measurements of microprocessor bus activity. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

* Mnemonic decode according to: "Book E: PowerPC Architecture Enhanced for Embedded Applications" Copyright Motorola, Inc. 03 May 99

Disassembly Features (Cont'd)

Features

- Physical address reconstruction (Instruction and Data cycles).
- SDRam cycle suppression.
- High-Low Instruction or Low-High Instruction execution order.
- Support for: Ras Bits: 13, 12, 11, 10 and Cas Bits: 10, 9, 8, 7

Configuring the MPC-824X Disassembler

Because of the complexity and flexibility of the MPC824X micro it is necessary to properly configure the support so the disassembler can process the data and display it accurately. When using the NEX-MPC824X support there is a control box (named either “Sandpnt Controls” or “MPC824X Controls”) that contains 5 select fields labeled Suppress SDRAM cycles, Instruction Order, Number of Row Bits, Number of Column Bits, and Mnemonics. Each select field is described in detail as follows:

Suppress SDRAM Cycles

This field permits Displaying (the default) or Suppressing the display of the Row and Column address cycles. If Suppress is selected then any Row or Column address cycle that does not have valid data associated with it will be hidden from view.

Instruction Order

By default the instructions will be processed with the HiData information disassembled first followed by the LoData. A select option is available to swap these resulting in LoData being disassembled first followed by the HiData.

Number of Row Bits

This field allows setting of the number of Row bits used by the memory interface. Default is 13, with selections for 12, 11, and 10 bits. This field must be properly set for the physical address reconstruction to be accurate.

Number of Column Bits

This field allows setting of the number of Column bits used by the memory interface. Default is 10, with selections for 9, 8, and 7 bits. This field must be properly set for the physical address reconstruction to be accurate.

Mnemonics

This field allows the user to choose to view the disassembled instructions as Book E mnemonics or Simplified mnemonics. See Appendix C for further information.

Support for Simplified Mnemonics

The MPC824X has a set of instruction codes defined in Appendix A of the MPC8240 Integrated Processor User's Manual, and these opcodes are the ones that are displayed by default in the disassembly listing. The MPC-824X disassembler also supports the Simplified Mnemonics for the PowerPC family based on the following document:

"PowerPC Microprocessor Family: The Programming Environments"
Document G522-0290-00
Copyright Motorola, Inc. 1997.

The actual opcode binary between the two mnemonics is unchanged, simply the opcode text that is used to represent the opcode. Because there is no way for the MPC-824X software to know which opcodes the user prefers to view a select field has been added to allow switching from one to the other.

The following Simplified Mnemonics are supported:

Double-Word Comparisons

When a compare value involves a 64-bit value ($L = 1$), a 'd' is inserted into the mnemonic before the immediate indicator; an 'i' indicates a double-word compare.

Word Comparisons

When a compare value involves a 32-bit value ($L = 0$), a 'w' is inserted into the mnemonic before the immediate indicator; an 'i' indicates a word compare.

Branch Mnemonics Incorporating Conditions

For the 'bc' instruction variations, the BO and BI field values are used to produce appropriately modified mnemonics.

NOTES: so(un) and ns(u) are used where summary overflow and unordered overlap.

'Not less than' (nl) is shown as 'greater than or equal to' (ge).

'Not greater than' (ng) is shown as 'less than or equal to' (le).

Simplified Mnemonics for Condition Register Logical Instructions

The mnemonics are translated into set, clear, move and invert mnemonics.

Simplified Mnemonics for Trap Instructions

The TO values are used to produce a modified mnemonic.

Support provided for:

- lt
- le
- eq
- ge
- gt
- ne
- llt
- lle
- lge
- lgt
- Unconditional

Remaining Mnemonics are represented as follows:

- nl -> ge
- lnl -> lge
- ng -> le
- lng -> lle

Simplified Mnemonics for Special-Purpose Registers

The SPR numeric value is used to produce a modified mnemonic containing the SPR identifier.

NOTES: There is an error in the table for Simplified Mnemonic for Move to SPRG0-SPRG3. The form shown under Simplified Mnemonic for Move from SPRG0-SPRG3 was followed. There is also an error for Simplified Mnemonic for Move from Time base lower. The form shown under Simplified Mnemonic for Move to Time base lower was followed.

No-Op

The 'nop' mnemonic replaces the 'ori 0,0,0' instruction.

Load Immediate

As appropriate, the 'addi' and 'addis' are replaced by 'li' and 'lis', respectively, when no addition is being performed.

Move Register

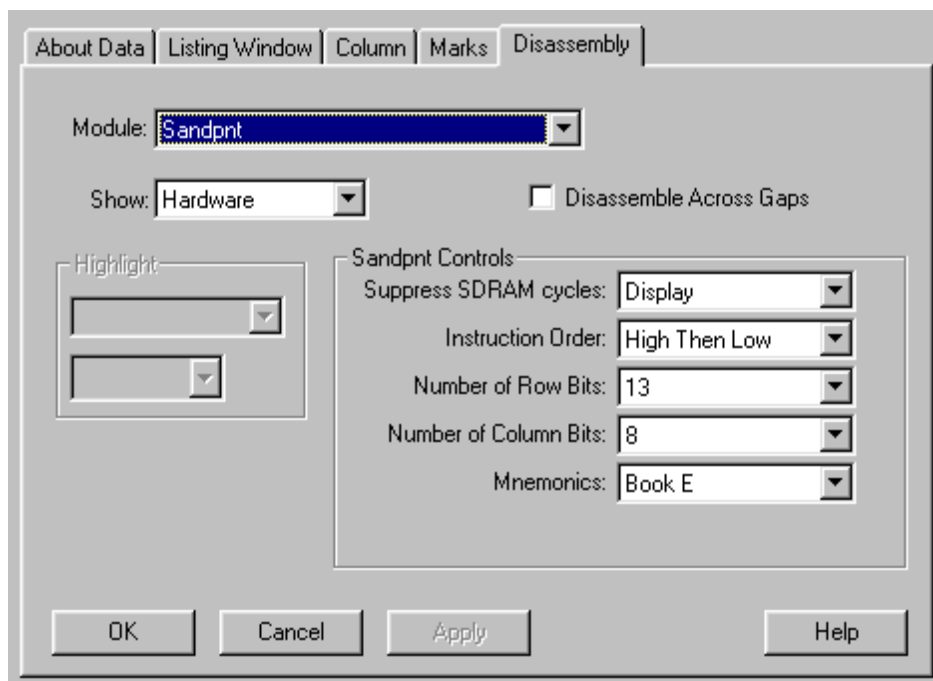
When no additional computation is being performed, the 'or' mnemonic is replaced by 'mr'.

Complement Register

When no additional computation is being performed, the 'nor' mnemonic is replaced by 'not'.

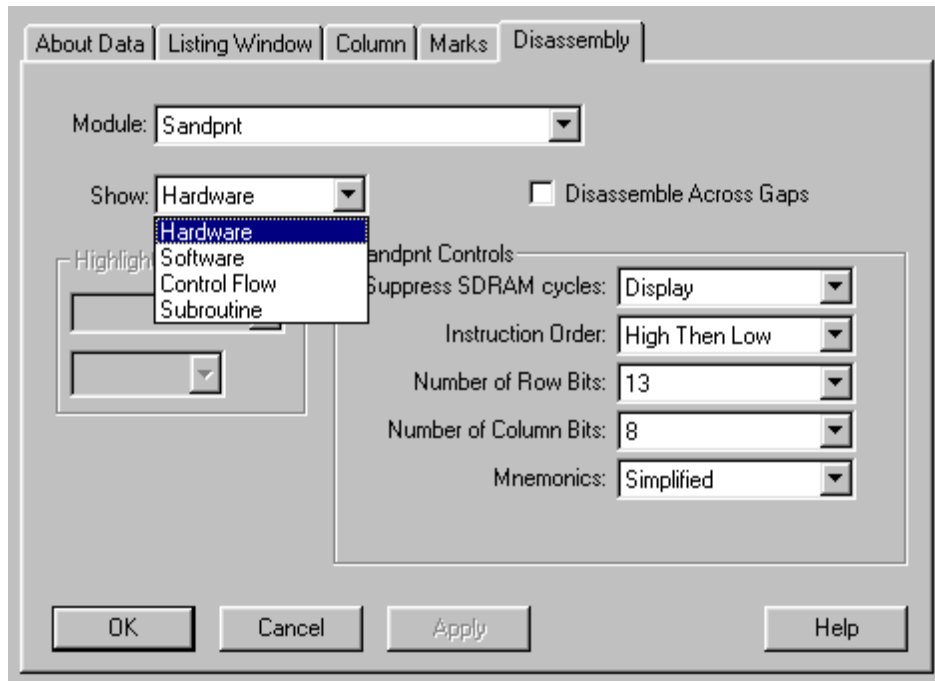
Move To Condition Register

When the low-order 32 bits of a General Purpose Register is moved to the Condition Register, the 'mtrf' mnemonic is translated to the 'mtr' form.

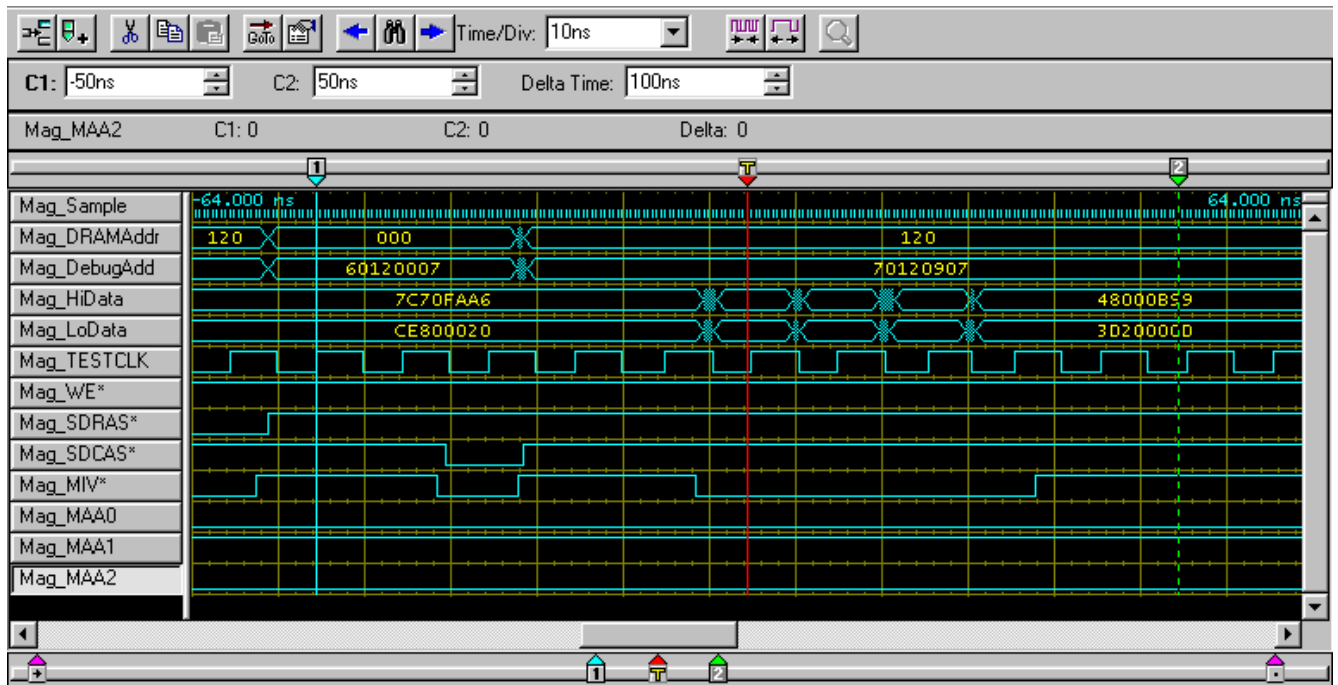


MPC824X Disassembly Controls

Note that when data is suppressed in this fashion that Timestamp information (in previous form) will be updated to show the time between displayed cycles.



Disassembly Display Filter Window



Timing Display

NEX-MPC8240 Mictor Pinout

NOTES: The pin numbers are given for the 352-pin Tape Ball Grid Array (TBGA) package. Blank entries in the MPC8240 Pin # and Signal columns denote unused TLA inputs that can be wired to any user signal.

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	CK0	RAS_CS5*	L2	36	6	CK1	RAS_CS4*	M2
4	7	A3:7	DL0 1	AD17	35	8	A1:7	DL16 1	B1
5	9	A3:6	DL1 1	AE17	34	10	A1:6	DL17 1	A1
6	11	A3:5	DL2 1	AE15	33	12	A1:5	DL18 1	A3
7	13	A3:4	DL3 1	AF15	32	14	A1:4	DL19 1	A4
8	15	A3:3	DL4 1	AC14	31	16	A1:3	DL20 1	A5
9	17	A3:2	DL5 1	AE13	30	18	A1:2	DL21 1	A6
10	19	A3:1	DL6 1	AF13	29	20	A1:1	DL22 1	A7
11	21	A3:0	DL7 1	AF12	28	22	A1:0	DL23 1	D7
12	23	A2:7	DL8 1	AF11	27	24	A0:7	DL24 1	A8
13	25	A2:6	DL9 1	AF10	26	26	A0:6	DL25 1	B8
14	27	A2:5	DL10 1	AF9	25	28	A0:5	DL26 1	A10
15	29	A2:4	DL11 1	AD8	24	30	A0:4	DL27 1	D10
16	31	A2:3	DL12 1	AF8	23	32	A0:3	DL28 1	A12
17	33	A2:2	DL13 1	AF7	22	34	A0:2	DL29 1	B11
18	35	A2:1	DL14 1	AF6	21	36	A0:1	DL30 1	B12
19	37	A2:0	DL15 1	AE5	20	38	A0:0	DL31 1	A14

A-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	Q0	RAS_CS0*	Y4	36	6	CK2	RAS_CS6*	M1
4	7	D3:7	DH0 1	AC17	35	8	D1:7	DH16 1	E4
5	9	D3:6	DH1 1	AF16	34	10	D1:6	DH17 1	A2
6	11	D3:5	DH2 1	AE16	33	12	D1:5	DH18 1	B3
7	13	D3:4	DH3 1	AE14	32	14	D1:4	DH19 1	D4
8	15	D3:3	DH4 1	AF14	31	16	D1:3	DH20 1	B4
9	17	D3:2	DH5 1	AC13	30	18	D1:2	DH21 1	B5
10	19	D3:1	DH6 1	AE12	29	20	D1:1	DH22 1	D6
11	21	D3:0	DH7 1	AE11	28	22	D1:0	DH23 1	C6
12	23	D2:7	DH8 1	AE10	27	24	D0:7	DH24 1	B7
13	25	D2:6	DH9 1	AE9	26	26	D0:6	DH25 1	C9
14	27	D2:5	DH10 1	AE8	25	28	D0:5	DH26 1	A9
15	29	D2:4	DH11 1	AC7	24	30	D0:4	DH27 1	B10
16	31	D2:3	DH12 1	AE7	23	32	D0:3	DH28 1	A11
17	33	D2:2	DH13 1	AE6	22	34	D0:2	DH29 1	A13
18	35	D2:1	DH14 1	AF5	21	36	D0:1	DH30 1	B13
19	37	D2:0	DH15 1	AC5	20	38	D0:0	DH31 1	A15

D-Group Mictor connector

Notes: Signal required for disassembly

NEX-MPC8240 Mictor Pinout (Cont'd)

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	Q3	RAS_CS3*	AC4	36	6	Q2	RAS_CS2*	AA4
4	7	E3:7	RCS1*	N2	35	8	E1:7	unused	
5	9	E3:6	RCS0*	N4	34	10	E1:6	unused	
6	11	E3:5	SDBA0 1	P2	33	12	E1:5	do not use	-----
7	13	E3:4	SDMA12/SDBA1 1	P1	32	14	E1:4	do not use	-----
8	15	E3:3	SDMA11 1	N1	31	16	E1:3	do not use	-----
9	17	E3:2	SDMA10 1	R1	30	18	E1:2	do not use	-----
10	19	E3:1	SDMA9 1	R2	29	20	E1:1	do not use	-----
11	21	E3:0	SDMA8 1	T1	28	22	E1:0	do not use	-----
12	23	E2:7	SDMA7 1	T2	27	24	E0:7	do not use	-----
13	25	E2:6	SDMA6 1	U4	26	26	E0:6	do not use	-----
14	27	E2:5	SDMA5 1	U2	25	28	E0:5	do not use	-----
15	29	E2:4	SDMA4 1	U1	24	30	E0:4	do not use	-----
16	31	E2:3	SDMA3 1	V1	23	32	E0:3	do not use	-----
17	33	E2:2	SDMA2 1	V3	22	34	E0:2	do not use	-----
18	35	E2:1	SDMA1 1	W1	21	36	E0:1	do not use	-----
19	37	E2:0	SDMA0 1	W2	20	38	E0:0	do not use	-----

E-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	CK3	SDRAM_CLK 2	see Note 1	36	6	Q1	RAS_CS1*	AA3
4	7	C3:7	CAS/DQM7 1	J1	35	8	C1:7	DA15 3	J2
5	9	C3:6	CAS/DQM6 1	K1	34	10	C1:6	DA14 3	F1
6	11	C3:5	CAS/DQM5 1	AC2	33	12	C1:5	DA13 3	AF19
7	13	C3:4	CAS/DQM4 1	AC1	32	14	C1:4	DA12 3	AF17
8	15	C3:3	CAS/DQM3 1	K2	31	16	C1:3	DA11 3	AD26
9	17	C3:2	CAS/DQM2 1	K3	30	18	C1:2	PLL0/DA10 3	A22
10	19	C3:1	CAS/DQM1 1	AB2	29	20	C1:1	PLL1/DA9 3	B19
11	21	C3:0	CAS/DQM0 1	AB1	28	22	C1:0	PLL2/DA8 3	A21
12	23	C2:7	RAS_CS7*	L1	27	24	C0:7	PLL3/DA7 3	B18
13	25	C2:6	MAA2 1	AE1	26	26	C0:6	PLL4/DA6 3	B17
14	27	C2:5	MAA1 1	AF1	25	28	C0:5	GNT4*/DA5 3	W26
15	29	C2:4	MAA0 1	AF2	24	30	C0:4	REQ4*/DA4 3	Y26
16	31	C2:3	SDRAS* 1	AD1	23	32	C0:3	PCICLK4/DA3 3	AF26
17	33	C2:2	SDCAS* 1	AD2	22	34	C0:2	DA2 3	C25
18	35	C2:1	WE* 1	AA1	21	36	C0:1	CKO/DA1 3	B15
19	37	C2:0	MIV* 1	A16	20	38	C0:0	QACK*/D0 3	F2

C-Group Mictor connector

Notes:

Signal required for disassembly

Any active SDRAM clock signal can be used.

These signals are used for Debug Address support.

NEX-MPC8240 Compression Pinout

Pad P4-PH2	Input	MPC8240 Signal Name	8240 Pin #
A15	Q3-	Gnd	Gnd
A13	Q3+	RAS_CS3*	AC4
B12	E3:7	RCS1*	N2
B10	E3:6	RCS0*	N4
A12	E3:5	SDBA0 1	P2
A10	E3:4	SDMA12/SDBA1 1	P1
B9	E3:3	SDMA11 1	N1
B7	E3:2	SDMA10 1	R1
A9	E3:1	SDMA9 1	R2
A7	E3:0	SDMA8 1	T1
B6	E2:7	SDMA7 1	T2
B4	E2:6	SDMA6 1	U4
A6	E2:5	SDMA5 1	U2
A4	E2:4	SDMA4 1	U1
B3	E2:3	SDMA3 1	V1
B1	E2:2	SDMA2 1	V3
A3	E2:1	SDMA1 1	W1
A1	E2:0	SDMA0 1	W2

Pad P4-PH1	Input	MPC8240 Signal Name	8240 Pin #
A15	Q2-	Gnd	Gnd
A13	Q2+	RAS_CS2*	AA4
B12	E1:7	unused	
B10	E1:6	unused	
A12	E1:5	do not use	-----
A10	E1:4	do not use	-----
B9	E1:3	do not use	-----
B7	E1:2	do not use	-----
A9	E1:1	do not use	-----
A7	E1:0	do not use	-----
B6	E0:7	do not use	-----
B4	E0:6	do not use	-----
A6	E0:5	do not use	-----
A4	E0:4	do not use	-----
B3	E0:3	do not use	-----
B1	E0:2	do not use	-----
A3	E0:1	do not use	-----
A1	E0:0	do not use	-----

Pad P3-PH2	Input	MPC8240 Signal Name	8240 Pin #
A15	CK0-	Gnd	Gnd
A13	CK0+	RAS_CS5*	L2
B12	A3:7	DL0 1	AD17
B10	A3:6	DL1 1	AE17
A12	A3:5	DL2 1	AE15
A10	A3:4	DL3 1	AF15
B9	A3:3	DL4 1	AC14
B7	A3:2	DL5 1	AE13
A9	A3:1	DL6 1	AF13
A7	A3:0	DL7 1	AF12
B6	A2:7	DL8 1	AF11
B4	A2:6	DL9 1	AF10
A6	A2:5	DL10 1	AF9
A4	A2:4	DL11 1	AD8
B3	A2:3	DL12 1	AF8
B1	A2:2	DL13 1	AF7
A3	A2:1	DL14 1	AF6
A1	A2:0	DL15 1	AE5

Pad P3-PH1	Input	MPC8240 Signal Name	8240 Pin #
A15	Q0-	Gnd	Gnd
A13	Q0+	RAS_CS0*	Y4
B12	D3:7	DH0 1	AC17
B10	D3:6	DH1 1	AF16
A12	D3:5	DH2 1	AE16
A10	D3:4	DH3 1	AE14
B9	D3:3	DH4 1	AF14
B7	D3:2	DH5 1	AC13
A9	D3:1	DH6 1	AE12
A7	D3:0	DH7 1	AE11
B6	D2:7	DH8 1	AE10
B4	D2:6	DH9 1	AE9
A6	D2:5	DH10 1	AE8
A4	D2:4	DH11 1	AC7
B3	D2:3	DH12 1	AE7
B1	D2:2	DH13 1	AE6
A3	D2:1	DH14 1	AF5
A1	D2:0	DH15 1	AC5

Notes: Signal required for disassembly

NEX-MPC8240 Compression Pinout (Cont'd)

Pad P2-PH2	Input	MPC8240 Signal Name	8240 Pin #
A15	CK1-	Gnd	Gnd
A13	CK1+	RAS_CS4*	M2
B12	A1:7	DL16 1	B1
B10	A1:6	DL17 1	A1
A12	A1:5	DL18 1	A3
A10	A1:4	DL19 1	A4
B9	A1:3	DL20 1	A5
B7	A1:2	DL21 1	A6
A9	A1:1	DL22 1	A7
A7	A1:0	DL23 1	D7
B6	A0:7	DL24 1	A8
B4	A0:6	DL25 1	B8
A6	A0:5	DL26 1	A10
A4	A0:4	DL27 1	D10
B3	A0:3	DL28 1	A12
B1	A0:2	DL29 1	B11
A3	A0:1	DL30 1	B12
A1	A0:0	DL31 1	A14

Pad P2-PH1	Input	MPC8240 Signal Name	8240 Pin#
A15	CK2-	Gnd	Gnd
A13	CK2+	RAS_CS6*	M1
B12	D1:7	DH16 1	E4
B10	D1:6	DH17 1	A2
A12	D1:5	DH18 1	B3
A10	D1:4	DH19 1	D4
B9	D1:3	DH20 1	B4
B7	D1:2	DH21 1	B5
A9	D1:1	DH22 1	D6
A7	D1:0	DH23 1	C6
B6	D0:7	DH24 1	B7
B4	D0:6	DH25 1	C9
A6	D0:5	DH26 1	A9
A4	D0:4	DH27 1	B10
B3	D0:3	DH28 1	A11
B1	D0:2	DH29 1	A13
A3	D0:1	DH30 1	B13
A1	D0:0	DH31 1	A15

Pad P1-PH2	Input	MPC8240 Signal Name	8240 Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	SDRAM_CLK 2	see Note 1
B12	C3:7	CAS/DQM7 1	J1
B10	C3:6	CAS/DQM6 1	K1
A12	C3:5	CAS/DQM5 1	AC2
A10	C3:4	CAS/DQM4 1	AC1
B9	C3:3	CAS/DQM3 1	K2
B7	C3:2	CAS/DQM2 1	K3
A9	C3:1	CAS/DQM1 1	AB2
A7	C3:0	CAS/DQM0 1	AB1
B6	C2:7	RAS_CS7*	L1
B4	C2:6	MAA2 1	AE1
A6	C2:5	MAA1 1	AF1
A4	C2:4	MAA0 1	AF2
B3	C2:3	SDRAS* 1	AD1
B1	C2:2	SDCAS* 1	AD2
A3	C2:1	WE* 1	AA1
A1	C2:0	MIV* 1	A16

Pad P1-PH1	Input	MPC8240 Signal Name	8240 Pin#
A15	Q1-	Gnd	Gnd
A13	Q1+	RAS_CS1*	AA3
B12	C1:7	DA15 3	J2
B10	C1:6	DA14 3	F1
A12	C1:5	DA13 3	AF19
A10	C1:4	DA12 3	AF17
B9	C1:3	DA11 3	AD26
B7	C1:2	PLL0/DA10 3	A22
A9	C1:1	PLL1/DA9 3	B19
A7	C1:0	PLL2/DA8 3	A21
B6	C0:7	PLL3/DA7 3	B18
B4	C0:6	PLL4/DA6 3	B17
A6	C0:5	GNT4*/DA5 3	W26
A4	C0:4	REQ4*/DA4 3	Y26
B3	C0:3	PCICLK4/DA3 3	AF26
B1	C0:2	DA2 3	C25
A3	C0:1	CKO/DA1 3	B15
A1	C0:0	QACK*/D0 3	F2

Notes:

Signal required for disassembly

Any active SDRAM clock signal can be used.

These signals are used for Debug Address support.

NEX-MPC8241/5 Mictor Pinout

NOTES: The pin numbers given for the MPC8241 are for the 357-pin Plastic Ball Grid Array (PBGA) package, and for the MPC8245 are for the 352-pin Tape Ball Grid Array (TBGA) package. Blank entries in the Pin # and Signal columns denote unused TLA inputs that may be wired to any user signal.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	CK0	RAS_CS5*	C8	L2	36	6	CK1	RAS_CS4*	C9	M2
4	7	A3:7	DL0 1	M19	AD17	35	8	A1:7	DL16 1	B3	B1
5	9	A3:6	DL1 1	M17	AE17	34	10	A1:6	DL17 1	C4	A1
6	11	A3:5	DL2 1	L16	AE15	33	12	A1:5	DL18 1	C2	A3
7	13	A3:4	DL3 1	L17	AF15	32	14	A1:4	DL19 1	D3	A4
8	15	A3:3	DL4 1	K18	AC14	31	16	A1:3	DL20 1	G5	A5
9	17	A3:2	DL5 1	J18	AE13	30	18	A1:2	DL21 1	E1	A6
10	19	A3:1	DL6 1	K17	AF13	29	20	A1:1	DL22 1	H5	A7
11	21	A3:0	DL7 1	K16	AF12	28	22	A1:0	DL23 1	E2	D7
12	23	A2:7	DL8 1	J15	AF11	27	24	A0:7	DL24 1	F1	A8
13	25	A2:6	DL9 1	J17	AF10	26	26	A0:6	DL25 1	F2	B8
14	27	A2:5	DL10 1	H18	AF9	25	28	A0:5	DL26 1	G2	A10
15	29	A2:4	DL11 1	F16	AD8	24	30	A0:4	DL27 1	J5	D10
16	31	A2:3	DL12 1	H16	AF8	23	32	A0:3	DL28 1	H1	A12
17	33	A2:2	DL13 1	H15	AF7	22	34	A0:2	DL29 1	H4	B11
18	35	A2:1	DL14 1	G17	AF6	21	36	A0:1	DL30 1	J4	B12
19	37	A2:0	DL15 1	D19	AE5	20	38	A0:0	DL31 1	J1	A14

A-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	Q0	RAS_CS0*	A17	Y4	36	6	CK2	RAS_CS6*	A10	M1
4	7	D3:7	DH0 1	M18	AC17	35	8	D1:7	DH16 1	C3	E4
5	9	D3:6	DH1 1	L18	AF16	34	10	D1:6	DH17 1	D4	A2
6	11	D3:5	DH2 1	L15	AE16	33	12	D1:5	DH18 1	E5	B3
7	13	D3:4	DH3 1	K19	AE14	32	14	D1:4	DH19 1	F5	D4
8	15	D3:3	DH4 1	K15	AF14	31	16	D1:3	DH20 1	D1	B4
9	17	D3:2	DH5 1	J19	AC13	30	18	D1:2	DH21 1	E4	B5
10	19	D3:1	DH6 1	J16	AE12	29	20	D1:1	DH22 1	D2	D6
11	21	D3:0	DH7 1	H17	AE11	28	22	D1:0	DH23 1	E3	C6
12	23	D2:7	DH8 1	G19	AE10	27	24	D0:7	DH24 1	F4	B7
13	25	D2:6	DH9 1	G18	AE9	26	26	D0:6	DH25 1	G3	C9
14	27	D2:5	DH10 1	G16	AE8	25	28	D0:5	DH26 1	G4	A9
15	29	D2:4	DH11 1	D18	AC7	24	30	D0:4	DH27 1	G1	B10
16	31	D2:3	DH12 1	F18	AE7	23	32	D0:3	DH28 1	H2	A11
17	33	D2:2	DH13 1	E18	AE6	22	34	D0:2	DH29 1	J3	A13
18	35	D2:1	DH14 1	G15	AF5	21	36	D0:1	DH30 1	J2	B13
19	37	D2:0	DH15 1	E15	AC5	20	38	D0:0	DH31 1	K5	A15

D Group Mictor connector

Notes: Signal required for disassembly

NEX-MPC8241/5 Mictor Pinout (Cont'd)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	Q3	RAS_CS3*	C17	AC4	36	6	Q2	RAS_CS2*	C16	AA4
4	7	E3:7	RCS0*	C10	N4	35	8	E1:7	SDBA1 1	C11	P1
5	9	E3:6	SDMA14/ CHKSTOP_IN* 1	K2	D14	34	10	E1:6	SDBA0 1	B11	P2
6	11	E3:5	SDMA13/TBEN 1	K3	B14	33	12	E1:5	RCS1*	B9	N2
7	13	E3:4	SDMA12/SRESET* 1	L3	B16	32	14	E1:4	RCS2*/TRIG_IN	P18	AF20
8	15	E3:3	SDMA11 1	A11	N1	31	16	E1:3	RCS3*/TRIG_OUT	N18	AC18
9	17	E3:2	SDMA10 1	B12	R1	30	18	E1:2			
10	19	E3:1	SDMA9 1	A12	R2	29	20	E1:1			
11	21	E3:0	SDMA8 1	C12	T1	28	22	E1:0			
12	23	E2:7	SDMA7 1	B13	T2	27	24	E0:7			
13	25	E2:6	SDMA6 1	C13	U4	26	26	E0:6			
14	27	E2:5	SDMA5 1	D12	U2	25	28	E0:5			
15	29	E2:4	SDMA4 1	A14	U1	24	30	E0:4			
16	31	E2:3	SDMA3 1	C14	V1	23	32	E0:3			
17	33	E2:2	SDMA2 1	B14	V3	22	34	E0:2			
18	35	E2:1	SDMA1 1	A15	W1	21	36	E0:1			
19	37	E2:0	SDMA0 1	B15	W2	20	38	E0:0			

E-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	CK3	SDRAM_CLK 2	Note 1	Note 1	36	6	Q1	RAS_CS1*	B17	AA3
4	7	C3:7	CAS/DQM7 1	B8	J1	35	8	C1:7	DA15 3	D8	J2
5	9	C3:6	CAS/DQM6 1	A9	K1	34	10	C1:6	DA14 3	B6	F1
6	11	C3:5	CAS/DQM5 1	D14	AC2	33	12	C1:5	DA13 3	N16	AF19
7	13	C3:4	CAS/DQM4 1	D15	AC1	32	14	C1:4	DA12 3	M16	AF17
8	15	C3:3	CAS/DQM3 1	C7	K2	31	16	C1:3	DA11 3	T13	AD26
9	17	C3:2	CAS/DQM2 1	A6	K3	30	18	C1:2	PLL0/DA10 3	N3	A22
10	19	C3:1	CAS/DQM1 1	B18	AB2	29	20	C1:1	PLL1/DA9 3	N2	B19
11	21	C3:0	CAS/DQM0 1	A18	AB1	28	22	C1:0	PLL2/DA8 3	N1	A21
12	23	C2:7	RAS_CS7*	B10	L1	27	24	C0:7	PLL3/DA7 3	M4	B18
13	25	C2:6	MAA2 1	C18	AE1	26	26	C0:6	PLL4/DA6 3	M3	B17
14	27	C2:5	MAA1 1	D17	AF1	25	28	C0:5	GNT4*/DA5 3	T11	W26
15	29	C2:4	MAA0 1	E17	AF2	24	30	C0:4	REQ4*/DA4 3	W13	Y26
16	31	C2:3	SDRAS* 1	B19	AD1	23	32	C0:3	PCICLK4/DA3 3	V17	AF26
17	33	C2:2	SDCAS* 1	D16	AD2	22	34	C0:2	DA2 3	R5	C25
18	35	C2:1	WE* 1	B16	AA1	21	36	C0:1	CKO/DA1 3	L1	B15
19	37	C2:0	MIV* 1	K1	A16	20	38	C0:0	QACK*/DA0 3	A3	F2

C-Group Mictor connector

Notes: Signal required for disassembly.
Any active SDRAM clock signal can be used.
These signals are used for Debug Address support.

NEX-MPC8241/5 Compression Pinout

Pad P4-PH2	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	Q3-	Gnd	Gnd	Gnd
A13	Q3+	RAS_CS3*	C17	AC4
B12	E3:7	RCS0*	C10	N4
B10	E3:6	SDMA14/ CHKSTOP_IN* 1	K2	D14
A12	E3:5	SDMA13/TBEN 1	K3	B14
A10	E3:4	SDMA12/SRESET* 1	L3	B16
B9	E3:3	SDMA11 1	A11	N1
B7	E3:2	SDMA10 1	B12	R1
A9	E3:1	SDMA9 1	A12	R2
A7	E3:0	SDMA8 1	C12	T1
B6	E2:7	SDMA7 1	B13	T2
B4	E2:6	SDMA6 1	C13	U4
A6	E2:5	SDMA5 1	D12	U2
A4	E2:4	SDMA4 1	A14	U1
B3	E2:3	SDMA3 1	C14	V1
B1	E2:2	SDMA2 1	B14	V3
A3	E2:1	SDMA1 1	A15	W1
A1	E2:0	SDMA0 1	B15	W2

Pad P4-PH1	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	Q2-	Gnd	Gnd	Gnd
A13	Q2+	RAS_CS2*	C16	AA4
B12	E1:7	SDBA1 1	C11	P1
B10	E1:6	SDBA0 1	B11	P2
A12	E1:5	RCS1*	B9	N2
A10	E1:4	RCS2*/TRIG_IN	P18	AF20
B9	E1:3	RCS3*/TRIG_O UT	N18	AC18
B7	E1:2			
A9	E1:1			
A7	E1:0			
B6	E0:7			
B4	E0:6			
A6	E0:5			
A4	E0:4			
B3	E0:3			
B1	E0:2			
A3	E0:1			
A1	E0:0			

Pad P3-PH2	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	CK0-	Gnd	Gnd	Gnd
A13	CK0+	RAS_CS5*	C8	L2
B12	A3:7	DL0 1	M19	AD17
B10	A3:6	DL1 1	M17	AE17
A12	A3:5	DL2 1	L16	AE15
A10	A3:4	DL3 1	L17	AF15
B9	A3:3	DL4 1	K18	AC14
B7	A3:2	DL5 1	J18	AE13
A9	A3:1	DL6 1	K17	AF13
A7	A3:0	DL7 1	K16	AF12
B6	A2:7	DL8 1	J15	AF11
B4	A2:6	DL9 1	J17	AF10
A6	A2:5	DL10 1	H18	AF9
A4	A2:4	DL11 1	F16	AD8
B3	A2:3	DL12 1	H16	AF8
B1	A2:2	DL13 1	H15	AF7
A3	A2:1	DL14 1	G17	AF6
A1	A2:0	DL15 1	D19	AE5

Pad P3-PH1	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	Q0-	Gnd	Gnd	Gnd
A13	Q0+	RAS_CS0*	A17	Y4
B12	D3:7	DH0 1	M18	AC17
B10	D3:6	DH1 1	L18	AF16
A12	D3:5	DH2 1	L15	AE16
A10	D3:4	DH3 1	K19	AE14
B9	D3:3	DH4 1	K15	AF14
B7	D3:2	DH5 1	J19	AC13
A9	D3:1	DH6 1	J16	AE12
A7	D3:0	DH7 1	H17	AE11
B6	D2:7	DH8 1	G19	AE10
B4	D2:6	DH9 1	G18	AE9
A6	D2:5	DH10 1	G16	AE8
A4	D2:4	DH11 1	D18	AC7
B3	D2:3	DH12 1	F18	AE7
B1	D2:2	DH13 1	E18	AE6
A3	D2:1	DH14 1	G15	AF5
A1	D2:0	DH15 1	E15	AC5

Notes: Signal required for disassembly

NEX-MPC8241/5 Compression Pinout (Cont'd)

Pad P2-PH2	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	CK1-	Gnd	Gnd	Gnd
A13	CK1+	RAS_CS4*	C9	M2
B12	A1:7	DL16 1	B3	B1
B10	A1:6	DL17 1	C4	A1
A12	A1:5	DL18 1	C2	A3
A10	A1:4	DL19 1	D3	A4
B9	A1:3	DL20 1	G5	A5
B7	A1:2	DL21 1	E1	A6
A9	A1:1	DL22 1	H5	A7
A7	A1:0	DL23 1	E2	D7
B6	A0:7	DL24 1	F1	A8
B4	A0:6	DL25 1	F2	B8
A6	A0:5	DL26 1	G2	A10
A4	A0:4	DL27 1	J5	D10
B3	A0:3	DL28 1	H1	A12
B1	A0:2	DL29 1	H4	B11
A3	A0:1	DL30 1	J4	B12
A1	A0:0	DL31 1	J1	A14

Pad P2-PH1	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	CK2-	Gnd	Gnd	Gnd
A13	CK2+	RAS_CS6*	A10	M1
B12	D1:7	DH16 1	C3	E4
B10	D1:6	DH17 1	D4	A2
A12	D1:5	DH18 1	E5	B3
A10	D1:4	DH19 1	F5	D4
B9	D1:3	DH20 1	D1	B4
B7	D1:2	DH21 1	E4	B5
A9	D1:1	DH22 1	D2	D6
A7	D1:0	DH23 1	E3	C6
B6	D0:7	DH24 1	F4	B7
B4	D0:6	DH25 1	G3	C9
A6	D0:5	DH26 1	G4	A9
A4	D0:4	DH27 1	G1	B10
B3	D0:3	DH28 1	H2	A11
B1	D0:2	DH29 1	J3	A13
A3	D0:1	DH30 1	J2	B13
A1	D0:0	DH31 1	K5	A15

Pad P1-PH2	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	CK3-	Gnd	Gnd	Gnd
A13	CK3+	SDRAM_CLK2	Note 1	Note 1
B12	C3:7	CAS/DQM7 1	B8	J1
B10	C3:6	CAS/DQM6 1	A9	K1
A12	C3:5	CAS/DQM5 1	D14	AC2
A10	C3:4	CAS/DQM4 1	D15	AC1
B9	C3:3	CAS/DQM3 1	C7	K2
B7	C3:2	CAS/DQM2 1	A6	K3
A9	C3:1	CAS/DQM1 1	B18	AB2
A7	C3:0	CAS/DQM0 1	A18	AB1
B6	C2:7	RAS_CS7*	B10	L1
B4	C2:6	MAA2 1	C18	AE1
A6	C2:5	MAA1 1	D17	AF1
A4	C2:4	MAA0 1	E17	AF2
B3	C2:3	SDRAS* 1	B19	AD1
B1	C2:2	SDCAS* 1	D16	AD2
A3	C2:1	WE* 1	B16	AA1
A1	C2:0	MIV* 1	K1	A16

Pad P1-PH1	Input	MPC824X Signal Name	8241 Pin #	8245 Pin #
A15	Q1-	Gnd	Gnd	Gnd
A13	Q1+	RAS_CS1*	B17	AA3
B12	C1:7	DA15 3	D8	J2
B10	C1:6	DA14 3	B6	F1
A12	C1:5	DA13 3	N16	AF19
A10	C1:4	DA12 3	M16	AF17
B9	C1:3	DA11 3	T13	AD26
B7	C1:2	PLL0/DA10 3	N3	A22
A9	C1:1	PLL1/DA9 3	N2	B19
A7	C1:0	PLL2/DA8 3	N1	A21
B6	C0:7	PLL3/DA7 3	M4	B18
B4	C0:6	PLL4/DA6 3	M3	B17
A6	C0:5	GNT4*/DA5 3	T11	W26
A4	C0:4	REQ4*/DA4 3	W13	Y26
B3	C0:3	PCICLK4/DA3 3	V17	AF26
B1	C0:2	DA2 3	R5	C25
A3	C0:1	CKO/DA1 3	L1	B15
A1	C0:0	QACK*/DA0 3	A3	F2

Notes: Signal required for disassembly.
Any active SDRAM clock signal can be used.
These signals are used for Debug Address support.

TLA600/700 System Requirements

TLA600 or TLA700 with a minimum of 136 channel acquisition module. The 200MHz sync.option is required on the TLA acquisition module when the 824X memory bus is running faster then 100MHz.

Support is not available for the DAS9200 or TLA5x0.

Ordering / Contact Information

Part Number NEX-MPC824X

Includes: Software to setup/configure the TLA600/700
NEX-8240, NEX-8245 (also used for the MPC8241) and NEX-SNDPNT (Motorola Sandpoint evaluation board)* disassembly software for the TLA600/700
on 3 1/2" Diskettes
Manual

*The Motorola Sandpoint evaluation board has Mictor connectors placed on it for easy access to the MPC8240 signals. However, in order for our Sandpoint support package to function properly several signals must be moved using two New Wave NEX-HDSWIZ adapters. One HDSWIZ is used with the TLA's 'E' Mictor cable; the second is used with the 'C' Mictor probe.

Postal: Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

Telephone: 877-595-8116

Fax: 877-595-8118

Email: support@nexustechnology.com
quotes@nexustechnology.com
techsupport@nexustechnology.com

Website: www.nexustechnology.com

Placing an Order

Credit Card orders can be placed directly at 877-595-8116.

Purchase orders can be faxed to 877-595-8118.

Nexus Technology, Inc. reserves the right to make changes in design or specification at any time without notice. Nexus Technology, Inc. does not assume responsibility for use of any circuitry described. All trademarks are the property of their respective owners.