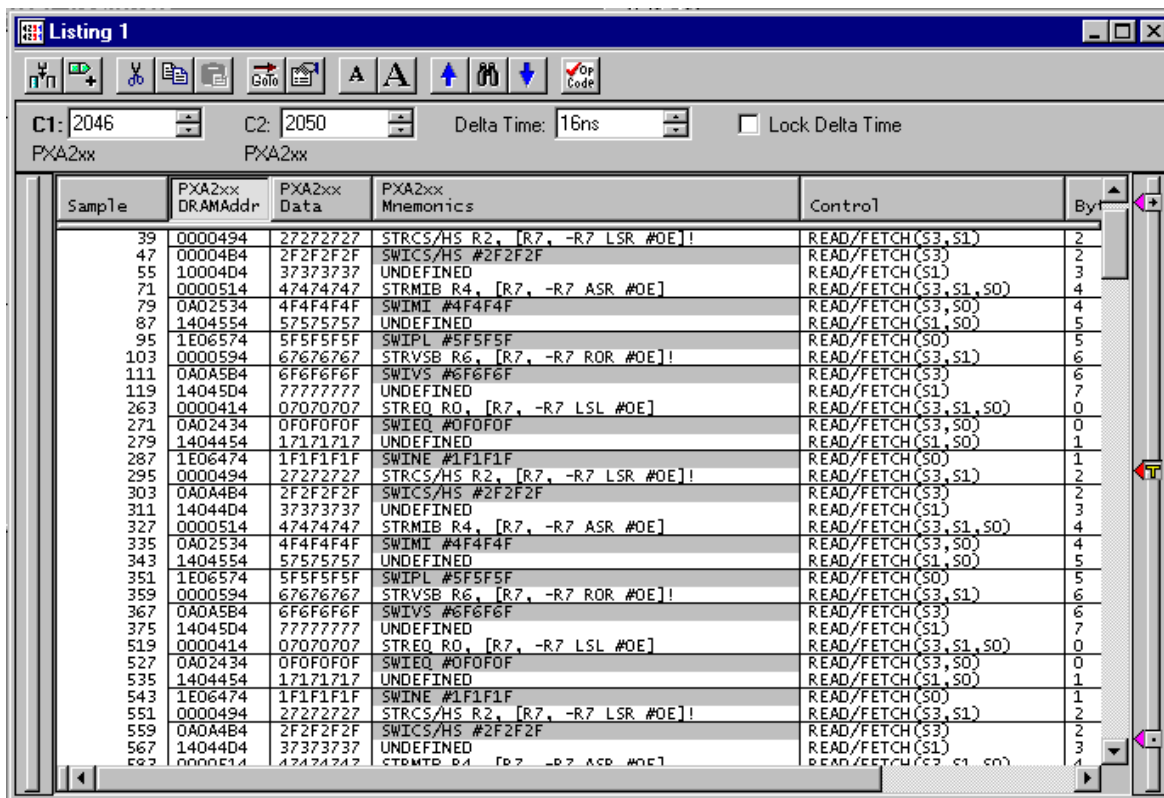


NEX-PXA2XX



Sample	PXA2xx DRAMAddr	PXA2xx Data	PXA2xx Mnemonics	Control	Byt
39	0000494	27272727	STRCS/HS R2, [R7, -R7 LSR #OE]!	READ/FETCH(S3, S1)	2
47	00004B4	2F2F2F2F	SWICS/HS #2F2F2F	READ/FETCH(S3)	2
55	10004D4	37373737	UNDEFINED	READ/FETCH(S1)	3
71	0000514	47474747	STRMIB R4, [R7, -R7 ASR #OE]	READ/FETCH(S3, S1, S0)	4
79	0A02534	4F4F4F4F	SWIMI #4F4F4F	READ/FETCH(S3, S0)	4
87	1404554	57575757	UNDEFINED	READ/FETCH(S1, S0)	5
95	1E06574	5F5F5F5F	SWIPL #5F5F5F	READ/FETCH(S0)	5
103	0000594	67676767	STRVSB R6, [R7, -R7 ROR #OE]!	READ/FETCH(S3, S1)	6
111	0A0A5B4	6F6F6F6F	SWIVS #6F6F6F	READ/FETCH(S3)	6
119	14045D4	77777777	UNDEFINED	READ/FETCH(S1)	7
263	0000414	07070707	STREQ R0, [R7, -R7 LSL #OE]	READ/FETCH(S3, S1, S0)	0
271	0A02434	0F0F0F0F	SWIEQ #0F0F0F	READ/FETCH(S3, S0)	0
279	1404454	17171717	UNDEFINED	READ/FETCH(S1, S0)	1
287	1E06474	1F1F1F1F	SWINE #1F1F1F	READ/FETCH(S0)	1
295	0000494	27272727	STRCS/HS R2, [R7, -R7 LSR #OE]!	READ/FETCH(S3, S1)	2
303	0A0A4B4	2F2F2F2F	SWICS/HS #2F2F2F	READ/FETCH(S3)	2
311	14044D4	37373737	UNDEFINED	READ/FETCH(S1)	3
327	0000514	47474747	STRMIB R4, [R7, -R7 ASR #OE]	READ/FETCH(S3, S1, S0)	4
335	0A02534	4F4F4F4F	SWIMI #4F4F4F	READ/FETCH(S3, S0)	4
343	1404554	57575757	UNDEFINED	READ/FETCH(S1, S0)	5
351	1E06574	5F5F5F5F	SWIPL #5F5F5F	READ/FETCH(S0)	5
359	0000594	67676767	STRVSB R6, [R7, -R7 ROR #OE]!	READ/FETCH(S3, S1)	6
367	0A0A5B4	6F6F6F6F	SWIVS #6F6F6F	READ/FETCH(S3)	6
375	14045D4	77777777	UNDEFINED	READ/FETCH(S1)	7
519	0000414	07070707	STREQ R0, [R7, -R7 LSL #OE]	READ/FETCH(S3, S1, S0)	0
527	0A02434	0F0F0F0F	SWIEQ #0F0F0F	READ/FETCH(S3, S0)	0
535	1404454	17171717	UNDEFINED	READ/FETCH(S1, S0)	1
543	1E06474	1F1F1F1F	SWINE #1F1F1F	READ/FETCH(S0)	1
551	0000494	27272727	STRCS/HS R2, [R7, -R7 LSR #OE]!	READ/FETCH(S3, S1)	2
559	0A0A4B4	2F2F2F2F	SWICS/HS #2F2F2F	READ/FETCH(S3)	2
567	14044D4	37373737	UNDEFINED	READ/FETCH(S1)	3
575	0000514	47474747	STRMIB R4, [R7, -R7 ASR #OE]	READ/FETCH(S3, S1, S0)	4

- Quick setup of the Logic Analyzer
- Disassembly of the acquired PXA210/250 data acquired from the SDRAM interface
- Support included for Intel BBPXA2XX Evaluation Board & the WindRiver PXA2XX Development Board
- Custom clocking or Clock on every edge
- Up to 8GHz Timing acquisition on every channel

When installed on the TLA600 or TLA700 the NEX-PXA2XX software provides quick and easy setup of the TLA and disassembly of the acquired PXA210/250 data.

The NEX-PXA2XX support is software only. Please see below for information on probing.

General Description

Connecting the TLA to a PXA210/250 target

The user must add Mictor connectors or Tektronix Compression Pads to their target for the interface to the TLA600/700 using Tektronix P6434 high-density probes or P6860 probes.

IMPORTANT: Specific wiring must be followed when routing the PXA210/250 signals to Mictor connectors or compression pads if the NEX-PXA2XX support is going to be used.

The NEX-PXA2XX support software acquires and decodes PXA2XX SDRAM bus activity and displays the information as assembly language mnemonics (machine code). This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types of interest to the software engineer. The user can choose to display the acquired data in Hardware, Software, Control Flow, or Subroutine modes.

Every stored cycle has a timestamp value stored with it. This time information, accurate to 500ps in the TLA7L/M/N/P/Q series, and accurate to 125ps in the TLA7AA/B series, permits precise measurements of microprocessor bus activity. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

NOTE: For the PXA2XX support to acquire all cycles in proper order, instruction prefetch caching **MUST BE DISABLED**.

Instruction Decoding/Addressing Modes Supported

The following lists the particular feature sets that the NEX-PXA2XX disassembler packages supports.

IMPORTANT: The Thumb instruction set is not supported at this time.

Architecture v4 Level Instructions and Addressing modes

- Load data read cycle detection
- LDM and LDC multiple load read cycle detection
- Branch Prefetch Instruction flush detection
- Mark-Opcode support

All five addressing modes:

Addressing Mode 1

- Shifter operands
- Immediate
- Register
- Logical shift left by immediate
- Logical shift left by register
- Logical shift right by immediate
- Logical shift right by register
- Arithmetic shift right by immediate
- Arithmetic shift right by register
- Rotate right by immediate
- Rotate right by register
- Rotate right with extend

Addressing Mode 2

- Register offset
- Scaled register offset
- Immediate pre-indexed
- Register pre-indexed
- Immediate post-indexed
- Register post-indexed
- Scaled register post-indexed
- Scaled register pre-indexed

Addressing Mode 3

- Immediate offset
- Register offset
- Immediate pre-indexed
- Immediate post-indexed
- Register pre-indexed
- Register post-indexed

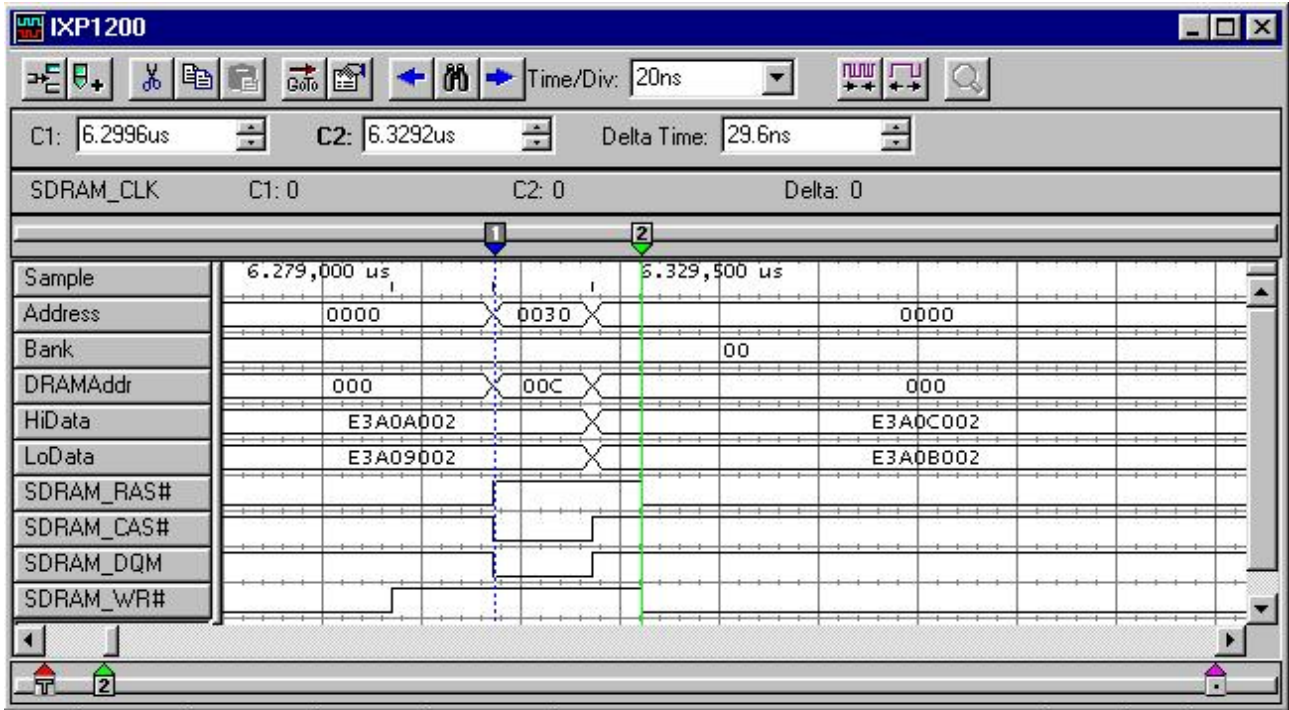
Addressing Mode 4

- Increment after
- Increment before
- Decrement after
- Decrement before

Addressing Mode 5

- Immediate offset
- Immediate pre-indexed
- Immediate post-indexed

Timing Display



PXA2XX Mictor Pin Assignments

Amp Mictor Pin #	Tek Mictor Pin #	TLA700 Channel	PXA2XX Signal Name	Amp Mictor Pin #	Tek Mictor Pin #	TLA700 Channel	PXA2XX Signal Name
5	3	CK0	SDCLKx	6	36	CK1	SDCLKx
7	4	A3:7	MA[25]	8	35	A1:7	MA[09]
9	5	A3:6	MA[24]	10	34	A1:6	MA[08]
11	6	A3:5	MA[23]	12	33	A1:5	MA[07]
13	7	A3:4	MA[22]	14	32	A1:4	MA[06]
15	8	A3:3	MA[21]	16	31	A1:3	MA[05]
17	9	A3:2	MA[20]	18	30	A1:2	MA[04]
19	10	A3:1	MA[19]	20	29	A1:1	MA[03]
21	11	A3:0	MA[18]	22	28	A1:0	MA[02]
23	12	A2:7	MA[17]	24	27	A0:7	MA[01]
25	13	A2:6	MA[16]	26	26	A0:6	MA[00]
27	14	A2:5	MA[15]	28	25	A0:5	
29	15	A2:4	MA[14]	30	24	A0:4	
31	16	A2:3	MA[13]	32	23	A0:3	
33	17	A2:2	MA[12]	34	22	A0:2	
35	18	A2:1	MA[11]	36	21	A0:1	
37	19	A2:0	MA[10]	38	20	A0:0	

'A' Mictor Probe

PXA2XX Mictor Pin Assignments (cont'd.)

Amp Mictor Pin #	Tek Mictor Pin #	TLA700 Channel	PXA2XX Signal Name	Amp Mictor Pin #	Tek Mictor Pin #	TLA700 Channel	PXA2XX Signal Name
5	3	CK3	nSDCS1	6	36	Q1	nSDCS0
7	4	C3:7	SDCKE1	8	35	C1:7	MD[15]
9	5	C3:6	SDCKE0	10	34	C1:6	MD[14]
11	6	C3:5		12	33	C1:5	MD[13]
13	7	C3:4		14	32	C1:4	MD[12]
15	8	C3:3		16	31	C1:3	MD[11]
17	9	C3:2		18	30	C1:2	MD[10]
19	10	C3:1		20	29	C1:1	MD[09]
21	11	C3:0		22	28	C1:0	MD[08]
23	12	C2:7	DQM3 ¹	24	27	C0:7	MD[07]
25	13	C2:6	DQM2 ¹	26	26	C0:6	MD[06]
27	14	C2:5	DQM1	28	25	C0:5	MD[05]
29	15	C2:4	DQM0	30	24	C0:4	MD[04]
31	16	C2:3	nOE	32	23	C0:3	MD[03]
33	17	C2:2	nWE	34	22	C0:2	MD[02]
35	18	C2:1	nSDCAS	36	21	C0:1	MD[01]
37	19	C2:0	nSDRAS	38	20	C0:0	MD[00]

'C' Mictor Probe

Amp Mictor Pin #	Tek Mictor Pin #	TLA700 Channel	PXA2XX Signal Name	Amp Mictor Pin #	Tek Mictor Pin #	TLA700 Channel	PXA2XX Signal Name
5	3	Q0	nSDCS3	6	36	CK2	nSDCS2
7	4	D3:7	²	8	35	D1:7	MD[31] ¹
9	5	D3:6	²	10	34	D1:6	MD[30] ¹
11	6	D3:5	²	12	33	D1:5	MD[29] ¹
13	7	D3:4	²	14	32	D1:4	MD[28] ¹
15	8	D3:3	²	16	31	D1:3	MD[27] ¹
17	9	D3:2	²	18	30	D1:2	MD[26] ¹
19	10	D3:1	²	20	29	D1:1	MD[25] ¹
21	11	D3:0	²	22	28	D1:0	MD[24] ¹
23	12	D2:7	²	24	27	D0:7	MD[23] ¹
25	13	D2:6	²	26	26	D0:6	MD[22] ¹
27	14	D2:5	²	28	25	D0:5	MD[21] ¹
29	15	D2:4	²	30	24	D0:4	MD[20] ¹
31	16	D2:3	²	32	23	D0:3	MD[19] ¹
33	17	D2:2	²	34	22	D0:2	MD[18] ¹
35	18	D2:1	²	36	21	D0:1	MD[17] ¹
37	19	D2:0	²	38	20	D0:0	MD[16] ¹

'D' Mictor Probe

Notes: 1)PXA250 only 2)Do not use (recommended)

TLA700 system requirements

TLA600 or TLA700 with a TLA7x3 or TLA7x4 (102 channel card min) or TLA7xx with a TLA7Ax3 or TLA7Ax4 (102 channel card min.).

Ordering / Contact Information

Part Number NEX-PXA2xx

Includes: Software to setup/configure the TLA600/700
PXA210/250 disassembly software for the TLA600/700 on 3 1/2" diskette
User Manual

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Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

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