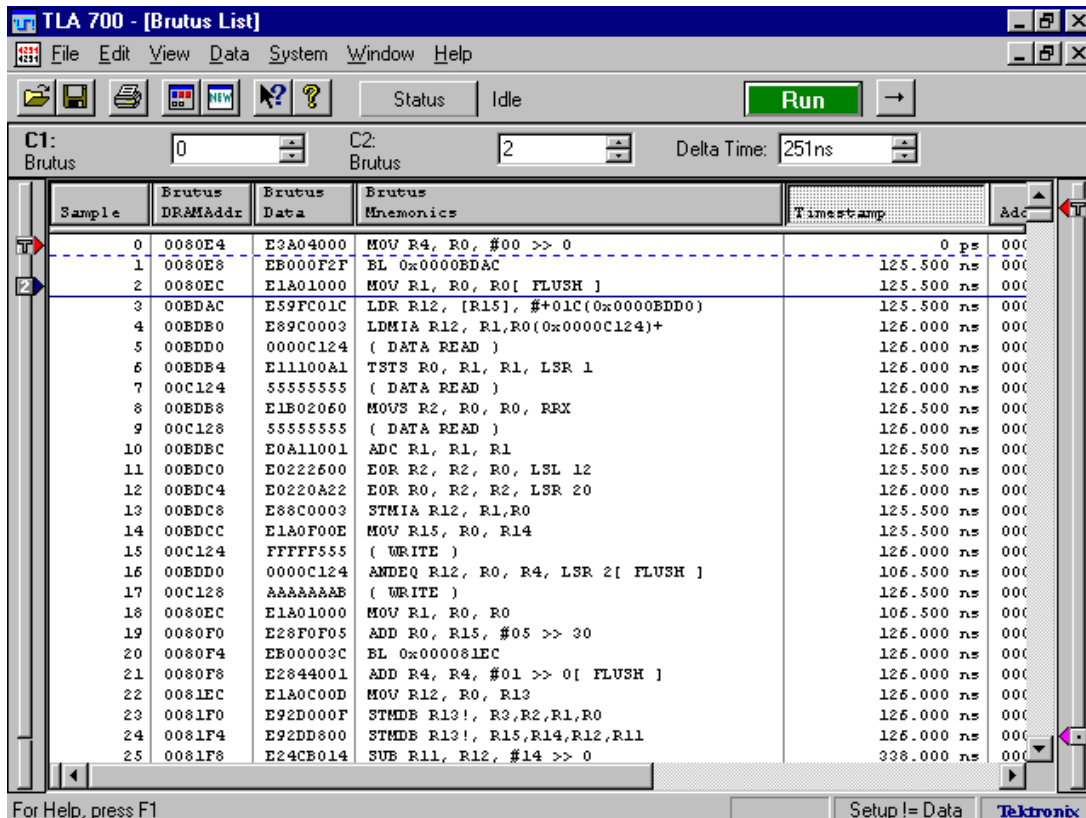


NEX-SA11XX



Sample	Brutus DRAMAddr	Brutus Data	Brutus Mnemonics	Timestamp	Adc
0	0080E4	E3A04000	MOV R4, R0, #00 >> 0	0 ps	000
1	0080E8	EB000F2F	BL 0x0000BDAC	125.500 ns	000
2	0080EC	E1A01000	MOV R1, R0, R0[FLUSH]	125.500 ns	000
3	00BDAC	E59FC01C	LDR R12, [R15], #+01C(0x0000BDD0)	125.500 ns	000
4	00EBE0	E89C0003	LDMIA R12, R1,R0(0x0000C124)+	126.000 ns	000
5	00EBD0	0000C124	(DATA READ)	126.000 ns	000
6	00EBE4	E11100A1	TSTS R0, R1, R1, LSR 1	126.000 ns	000
7	00C124	55555555	(DATA READ)	126.000 ns	000
8	00EBE8	E1B02060	MOVS R2, R0, R0, RFX	126.500 ns	000
9	00C128	55555555	(DATA READ)	126.000 ns	000
10	00EBEC	E0A11001	ADC R1, R1, R1	126.500 ns	000
11	00EBCC	E0222600	EOR R2, R2, R0, LSL 12	125.500 ns	000
12	00EBCC4	E0220A22	EOR R0, R2, R2, LSR 20	126.000 ns	000
13	00EBCC8	E88C0003	STMIA R12, R1,R0	125.500 ns	000
14	00EBCC	E1A0F00E	MOV R15, R0, R14	125.500 ns	000
15	00C124	FFFFFF55	(WRITE)	126.000 ns	000
16	00EBD0	0000C124	ANDEQ R12, R0, R4, LSR 2[FLUSH]	106.500 ns	000
17	00C128	AAAAAAAB	(WRITE)	126.500 ns	000
18	0080EC	E1A01000	MOV R1, R0, R0	106.500 ns	000
19	0080F0	E28F0F05	ADD R0, R15, #05 >> 30	126.000 ns	000
20	0080F4	EB00003C	BL 0x000081EC	126.000 ns	000
21	0080F8	E2844001	ADD R4, R4, #01 >> 0[FLUSH]	126.000 ns	000
22	0081EC	E1A0C00D	MOV R12, R0, R13	126.000 ns	000
23	0081F0	E92D000F	STMDB R13!, R3,R2,R1,R0	126.000 ns	000
24	0081F4	E92DD800	STMDB R13!, R15,R14,R12,R11	126.000 ns	000
25	0081F8	E24CB014	SUB R11, R12, #14 >> 0	338.000 ns	000

- Quick setup of the Logic Analyzer
- Disassembly of the data acquired from a SA1100 target or BRUTUS evaluation board from Intel
- Custom clocking or Clock on every edge Cycle Identification
- 2GHz Timing acquisition on every channel

When installed on the TLA600/700, the NEX-SA1100 software provides quick and easy setup of the TLA600/700 and disassembly of the acquired SA1100 data.

General Description

The NEX-SA1100 support is software only. Please see below for information on requirements for acquiring data and probing.

Connecting the TLA600/700 to a SA1100 target

When possible it is recommended that the user add Mictor connectors to their target for the interface to the TLA600/700 using Tektronix P6434 high-density probes.

IMPORTANT: Specific wiring must be followed when routing the SA1100 signals to Mictor connectors if the NEX-SA1100 support is going to be used. Table 2 shows this pinout.

Target and Logic Analyzer Requirements for Acquiring SA1100 Data

Target:

- GPIO26 must be available for use as an external clock
- Acquisition and disassembly of DRAM cycles only. SRAM or ROM bus cycles cannot be acquired because there is no end-of-cycle indication during burst reads.
- For most accurate disassembly both Icache and Dcache must be disabled. Example source is supplied to do this and also enable GPIO as a clock output.

Logic Analyzer:

- 200MHz TLA acquisition card necessary for core clock rates exceeding 200MHz.
- 136 channel TLA600/700 acquisition card required

Connecting the TLA600/700 to a BRUTUS Evaluation Board

The BRUTUS evaluation board has mictor connectors on it that connect directly to the Tektronix P6434 probes for the TLA600/700. However, two signals required for acquisition must be moved to specific input channels on the TLA600/700. This is accomplished by using a NEX-HDSWIZ adapter from Nexus Technology. Please order a NEX-HDSWIZ with the SA1100 software support if acquisition from a BRUTUS evaluation board is planned.

BRUTUS and Logic Analyzer Requirements for Acquiring SA1100 Data

BRUTUS Evaluation Board:

- Supplied code must be used to enable GPIO26 as a clock output
- It is recommended that the supplied code is run to disable both Icache and Dcache
- Acquisition and disassembly of DRAM cycles only. SRAM or ROM bus cycles cannot be acquired because there is no end-of-cycle indication during burst reads.
- One NEX-HDSWIZ must be used to route SA1100 clock to TLA600/700 clock input.

Logic Analyzer:

- 200MHz TLA acquisition card necessary for core clock rates exceeding 100MHz.
- 136 channel TLA600/700 acquisition card required

Disassembly Features

Identification / Support of the following:

- Architecture v4 Level Instructions and Addressing modes
- Load data read cycle detection
- LDM and LDC multiple load read cycle detection
- Branch Prefetch Instruction flush detection
- Mark-Opcode support

Support of all five addressing modes

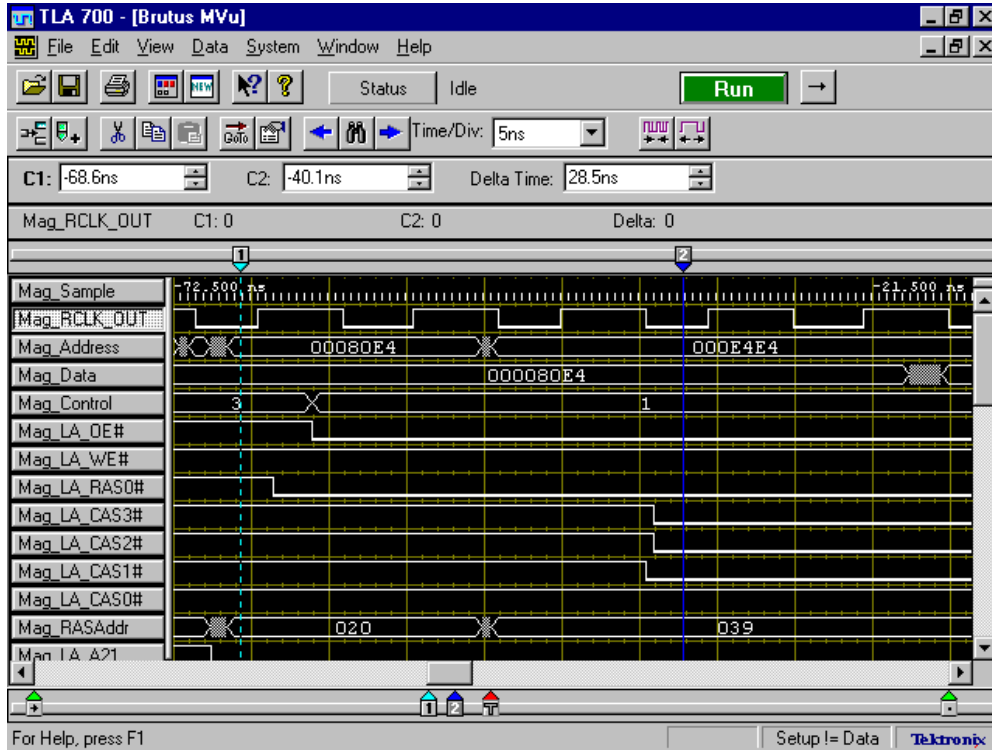
Instructions supported:

ADC, ADD, AND, B, BL, BIC, BX, CDP, CMN, CMP, EOR, LDC, LDM(1), LDM(2), LDM(3), LDR, LDRB, LDRBT, LDRH, LDRSB, LDRSH, LDRT, MCR, MLA, MOV, MRC, MRS (CPSR and SPSR), MSR (CPSR and SPSR), MUL, MVN, ORR, RSB, RSC, SBC, SMLAL, SMULL, STC, STM(1), STM(2), STR, STRB, STRBT, STRH, STRT, SUB, SWI, SWP, SWPB, TEQ, TST, UMLAL, UMULL

Thumb instruction set not supported at this time.

The SA1100 supports only 32-bit instruction Data Width.

Timing Display



Trigger Menu

The screenshot shows the Trigger Menu dialog box. The "Look for values in selected groups:" section is checked. The "Select definition:" dropdown is set to "Word 1". The "Rename..." button is visible. The dialog contains several input fields for defining trigger conditions:

- Address =
- DRAMAddr =
- Data =
- Control = (dropdown menu shows "READ/FETCH (XXXXXXXX01)" and "WRITE (XXXXXXXX10)")
- RASAddr =
- CASAddr =
- RASlines =
- CASlines =
- Selects =
- Misc =

The "Group Radix" section has a dropdown set to "Symbolic" and a "Symbol File..." button. The file path is "c:\program.\brutus_ctrl.tsf". The bottom of the dialog has buttons for "OK", "Cancel", "Add...", "Delete", and "Help".

Use the Add and Delete buttons to create or remove Word Event definitions. Use the Rename button to change the Word Event definition's name. Check the box next to a group to activate recognition of its value during an acquisition.

SA1100 TLA600/700 Signal Grouping

Name	Signal Name	SA1100 Pin #	TLA600/700 input	Group Name	Signal Name	SA1100 Pin #	TLA600/700 input
Address (Hex)	A[25]		A3:1	Data (Hex)	D[31]		E3:7
	A[24]		A3:0		D[30]		E3:6
	A[23]		A2:7		D[29]		E3:5
	A[22]		A2:6		D[28]		E3:4
	A[21]		A2:5		D[27]		E3:3
	A[20]		A2:4		D[26]		E3:2
	A[19]		A2:3		D[25]		E3:1
	A[18]		A2:2		D[24]		E3:0
	A[17]		A2:1		D[23]		E2:7
	A[16]		A2:0		D[22]		E2:6
	A[15]		A1:7		D[21]		E2:5
	A[14]		A1:6		D[20]		E2:4
	A[13]		A1:5		D[19]		E2:3
	A[12]		A1:4		D[18]		E2:2
	A[11]		A1:3		D[17]		E2:1
	A[10]		A1:2		D[16]		E2:0
	A[9]		A1:1		D[15]		E1:7
	A[8]		A1:0		D[14]		E1:6
	A[7]		A0:7		D[13]		E1:5
	A[6]		A0:6		D[12]		E1:4
	A[5]		A0:5		D[11]		E1:3
	A[4]		A0:4		D[10]		E1:2
	A[3]		A0:3		D[9]		E1:1
	A[2]		A0:2		D[8]		E1:0
	A[1]		A0:1		D[7]		E0:7
	A[0]		A0:0		D[6]		E0:6
DRAMAddr	CASAddr10		D2:4		D[5]		E0:5
	CASAddr9		D2:3		D[4]		E0:4
	CASAddr8		D2:2		D[3]		E0:3
	A[21]		A2:5		D[2]		E0:2
	A[20]		A2:4		D[1]		E0:1
	A[19]		A2:3		D[0]		E0:0
	A[18]		A2:2				
	A[17]		A2:1		Control (Sym)	nOE	C2:3
	A[16]		A2:0			nWE	C2:2
	A[15]		A1:7		RASlines	nRAS3	CK3
	A[14]		A1:6			nRAS2	CK2
	A[13]		A1:5			nRAS1	C2:1
	A[12]		A1:4			nRAS0	C2:0
	A[11]		A1:3		CASlines	nCAS3	Q3
	A[10]		A1:2			nCAS2	Q2
	CASAddr7		D2:1			nCAS1	Q1
	CASAddr6		D2:0			nCAS0	Q0
	CASAddr5		D1:7		Selects	nCS3	C2:7
	CASAddr4		D1:6			nCS2	C2:6
	CASAddr3		D1:5			nCS1	C2:5
	CASAddr2		D1:4			nCS0	C2:4
	CASAddr1		D1:3		Misc	RCLK_OUT	CK1
	CASAddr0		D1:2			nRESET_OUT	CK0
	DRAM_A1	---	D1:1				
	DRAM_A0	---	D1:0				

NEX-SA1100 Mictor Pinout

NOTES: The pin numbers are identical for the 208-pin Quad Flat Pack and 256-pin Mini-Ball Grid Array packages. Blank entries in the SA1100 Pin # and Signal columns denote unused TLA inputs that can be wired to any user signal.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal	Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal
3	5	CK0	192	nRESET_OUT	36	CK1	52	GP26
4	7	A3:7			35	A1:7	149	A15
5	9	A3:6			34	A1:6	150	A14
6	11	A3:5			33	A1:5	155	A13
7	13	A3:4			32	A1:4	156	A12
8	15	A3:3			31	A1:3	157	A11
9	17	A3:2			30	A1:2	158	A10
10	19	A3:1	137	A25	29	A1:1	159	A9
11	21	A3:0	138	A24	28	A1:0	160	A8
12	23	A2:7	139	A23	27	A0:7	163	A7
13	25	A2:6	140	A22	26	A0:6	164	A6
14	27	A2:5	143	A21	25	A0:5	165	A5
15	29	A2:4	144	A20	24	A0:4	166	A4
16	31	A2:3	145	A19	23	A0:3	167	A3
17	33	A2:2	146	A18	22	A0:2	168	A2
18	35	A2:1	147	A17	21	A0:1	169	A1
19	37	A2:0	148	A16	20	A0:0	170	A0

Mictor Group A

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal	Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal
3	5	CK3	121	nRAS3	36	Q1	127	nCAS1
4	7	C3:7			35	C1:7		
5	9	C3:6			34	C1:6		
6	11	C3:5			33	C1:5		
7	13	C3:4			32	C1:4		
8	15	C3:3			31	C1:3		
9	17	C3:2			30	C1:2		
10	19	C3:1			29	C1:1		
11	21	C3:0			28	C1:0		
12	23	C2:7	133	nCS3	27	C0:7		
13	25	C2:6	134	nCS2	26	C0:6		
14	27	C2:5	135	nCS1	25	C0:5		
15	29	C2:4	136	nCS0	24	C0:4		
16	31	C2:3	118	nOE	23	C0:3		
17	33	C2:2	117	nWE	22	C0:2		
18	35	C2:1	123	nRAS1	21	C0:1		
19	37	C2:0	124	nRAS0	20	C0:0		

Mictor Group C

NEX-SA1100 Mictor Pinout (cont'd)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal	Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal
3	5	Q0	128	nCAS0	36	CK2	122	nRAS2
4	7	D3:7			35	D1:7	DNU	Do Not Use
5	9	D3:6			34	D1:6	DNU	Do Not Use
6	11	D3:5			33	D1:5	DNU	Do Not Use
7	13	D3:4			32	D1:4	DNU	Do Not Use
8	15	D3:3			31	D1:3	DNU	Do Not Use
9	17	D3:2			30	D1:2	DNU	Do Not Use
10	19	D3:1			29	D1:1	DNU	Do Not Use
11	21	D3:0			28	D1:0	DNU	Do Not Use
12	23	D2:7	DNU	Do Not Use	27	D0:7		
13	25	D2:6	DNU	Do Not Use	26	D0:6		
14	27	D2:5	DNU	Do Not Use	25	D0:5		
15	29	D2:4	DNU	Do Not Use	24	D0:4		
16	31	D2:3	DNU	Do Not Use	23	D0:3		
17	33	D2:2	DNU	Do Not Use	22	D0:2		
18	35	D2:1	DNU	Do Not Use	21	D0:1		
19	37	D2:0	DNU	Do Not Use	20	D0:0		

Mictor Group D

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal	Mictor Pin #	TLA Channel	SA1100 Pin #	SA1100 Signal
3	5	Q3	125	nCAS3	36	Q2	126	nCAS2
4	7	E3:7	46	D31	35	E1:7	44	D15
5	9	E3:6	42	D30	34	E1:6	40	D14
6	11	E3:5	36	D29	33	E1:5	34	D13
7	13	E3:4	32	D28	32	E1:4	30	D12
8	15	E3:3	24	D27	31	E1:3	22	D11
9	17	E3:2	20	D26	30	E1:2	18	D10
10	19	E3:1	14	D25	29	E1:1	12	D9
11	21	E3:0	10	D24	28	E1:0	8	D8
12	23	E2:7	45	D23	27	E0:7	43	D7
13	25	E2:6	41	D22	26	E0:6	39	D6
14	27	E2:5	35	D21	25	E0:5	33	D5
15	29	E2:4	31	D20	24	E0:4	29	D4
16	31	E2:3	23	D19	23	E0:3	21	D3
17	33	E2:2	19	D18	22	E0:2	17	D2
18	35	E2:1	13	D17	21	E0:1	11	D1
19	37	E2:0	9	D16	20	E0:0	7	D0

Mictor Group E

TLA600/700 system requirements

TLA600 or TLA700 with a minimum of 136 channel acquisition card. Because of the setup/hold specifications of the SA1100, support is not available for the DAS9200 or TLA5x0.

Ordering / Contact Information

Part Number NEX-SA11XX

Please add one NEX-HDSWIZ if support for the BRUTUS evaluation board from Intel is required.
A NEX-HDSWIZ **is not** included and **is required** if support for the BRUTUS evaluation board from Intel is required.

Includes: Software to setup/configure the TLA600/700
StrongARM SA1100 disassembly software
BRUTUS / SA1100 disassembly software
Manual

Postal: Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

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techsupport@nexustechnology.com

Website: www.nexustechnology.com

Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.