

# DDR3-1600 SODIMM Slot Interposer

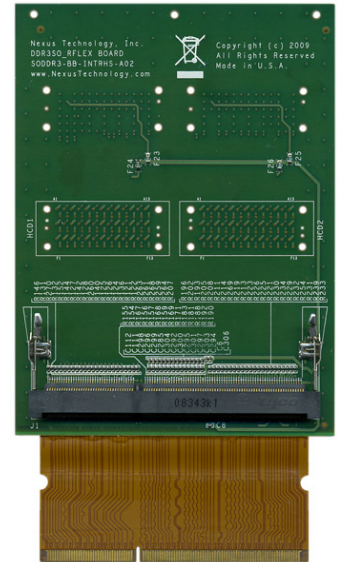
Flexible SODIMM Digital Validation



- High Speed DDR3 Digital Validation
- Passive 204-pin SODIMM Slot Interposer
- Acquisition Up to DDR3-1600
- Passive 50% Module Reduction w/MR Technology™
- Automated Logic Analyzer Setup
- DDR3 Protocol Violation Analysis
- Supports JEDEC PC3-12800, PC3-10600, PC3-8500, and PC3-6400 DDR3 modules

## Passive Module Reduction (MR) Technology™

Nexus Technology's Module Reduction Technology™ is available with this interposer. Products implementing MR Technology™ allow for full acquisition, including read and write data, while cutting the hardware requirements in half.



Module Reduction Technology™ is a software solution. No qualifier sideband signals are required and no active circuitry is implemented in MR Technology™ which would otherwise force double-probing and increase the load on the DDR3 target.

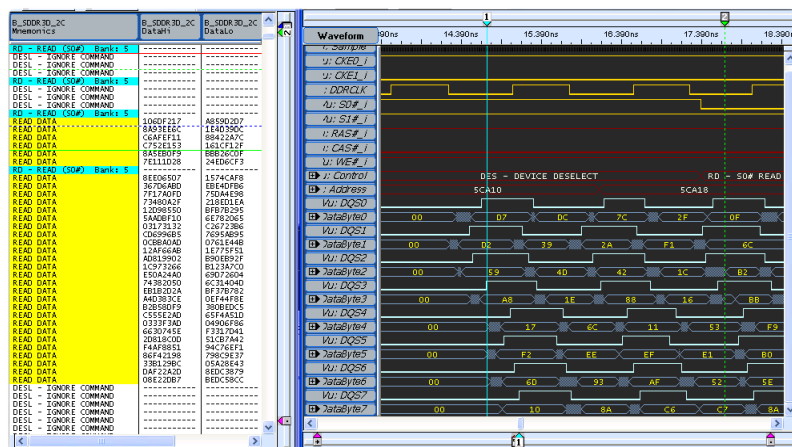
## Interposer Design

Nexus Technology recommends DDR3 slot interposers for applications where the customer must have the greatest flexibility in the probing of different DDR3 SODIMMs.

This interposer is an extender design and does not require a dedicated SODIMM slot. The logic analyzer connects above the normal SODIMM height so that there is no mechanical interference with adjacent SODIMMs.

This is a passive interposer with no added buffers to conceal system performance.

## Performance You Can See™



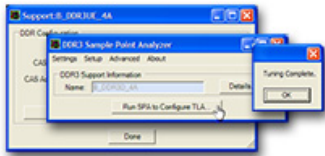
## Software

This DDR3-1600 SODIMM slot interposer comes with logic analyzer setup software, DDR3 protocol decode software, DDR3 data eye sample point analysis software, and protocol violation software.

### Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions for easy display and logic analyzer triggering/filtering.

### Data Sample Point Analysis Software



In order for the logic analyzer to capture data, the DDR3 signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDR3 data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes are purposely skewed - as per the DDR3

specification - on a byte basis relative to the DDR clock. The valid eyes also contain skew (again relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

These, among other factors, make reliable and accurate DDR3 read and write data bus acquisition extremely difficult - if done manually. [NEX-DDR3-SPA](#), provided free, automates this process enabling quick and reliable DDR3 read and write data bus acquisition in only minutes. For more information, please see the [NEX-DDR3-SPA](#) product.

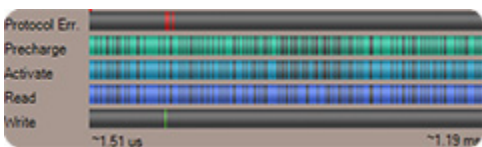
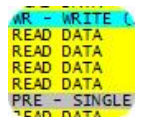
### Protocol Violation Software



There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Please see the [NEX-DDR-PROTOCOL](#) product for more information.

## Digital Validation

Logic analyzer setup software (TLA support package) is included with these products. This setup software acquires/reconstructs the 800MHz command/address bus and acquires/reconstructs the 1,600MT/s read write data from the data bus. The software also decodes and displays the bus protocol, shows the valid read/write data and provides easy DDR protocol triggering to quickly capture relevant data.

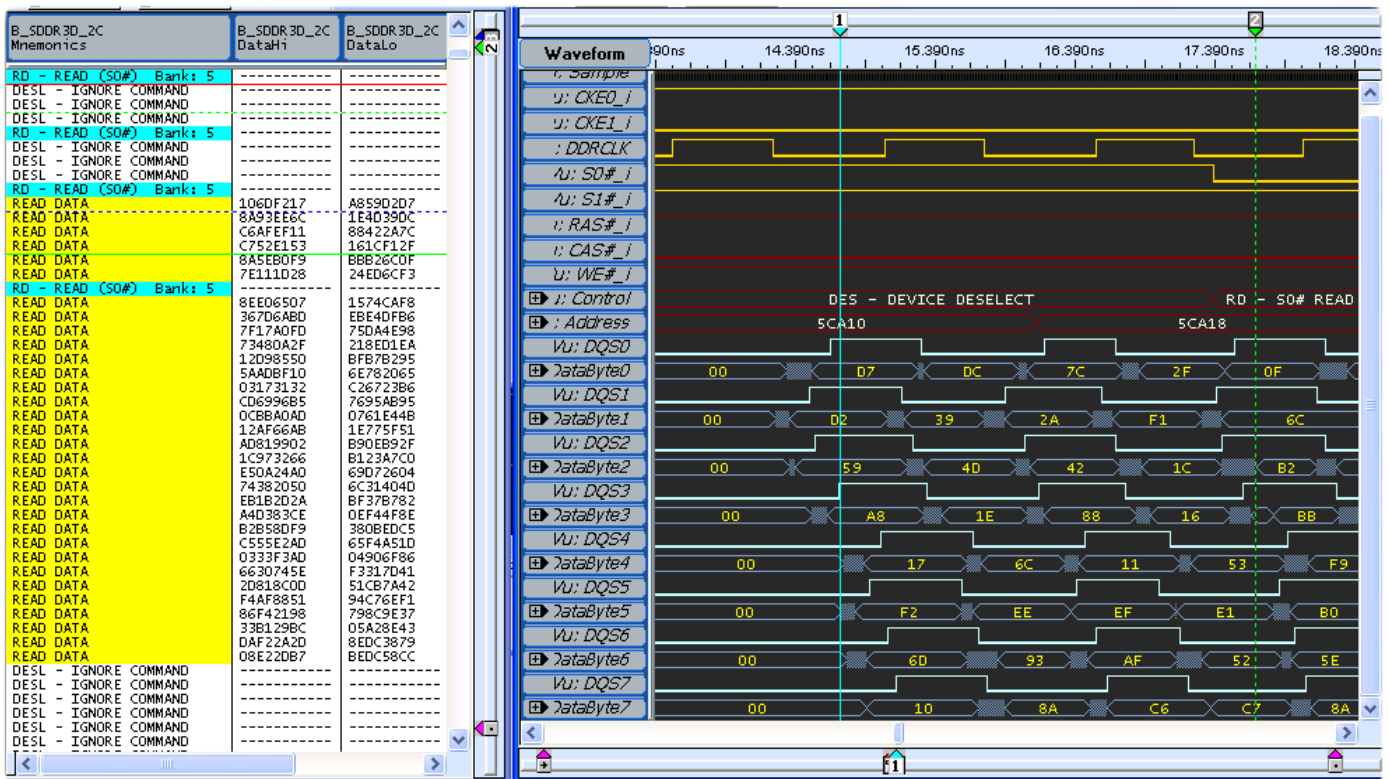


These products also come with the [NEX-DDR-PROTOCOL](#) software tool. This software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs basic protocol

violation checking. Advanced protocol violation checking is available for purchase separately. Please see the [NEX-DDR-PROTOCOL](#) product for more information on this powerful tool.

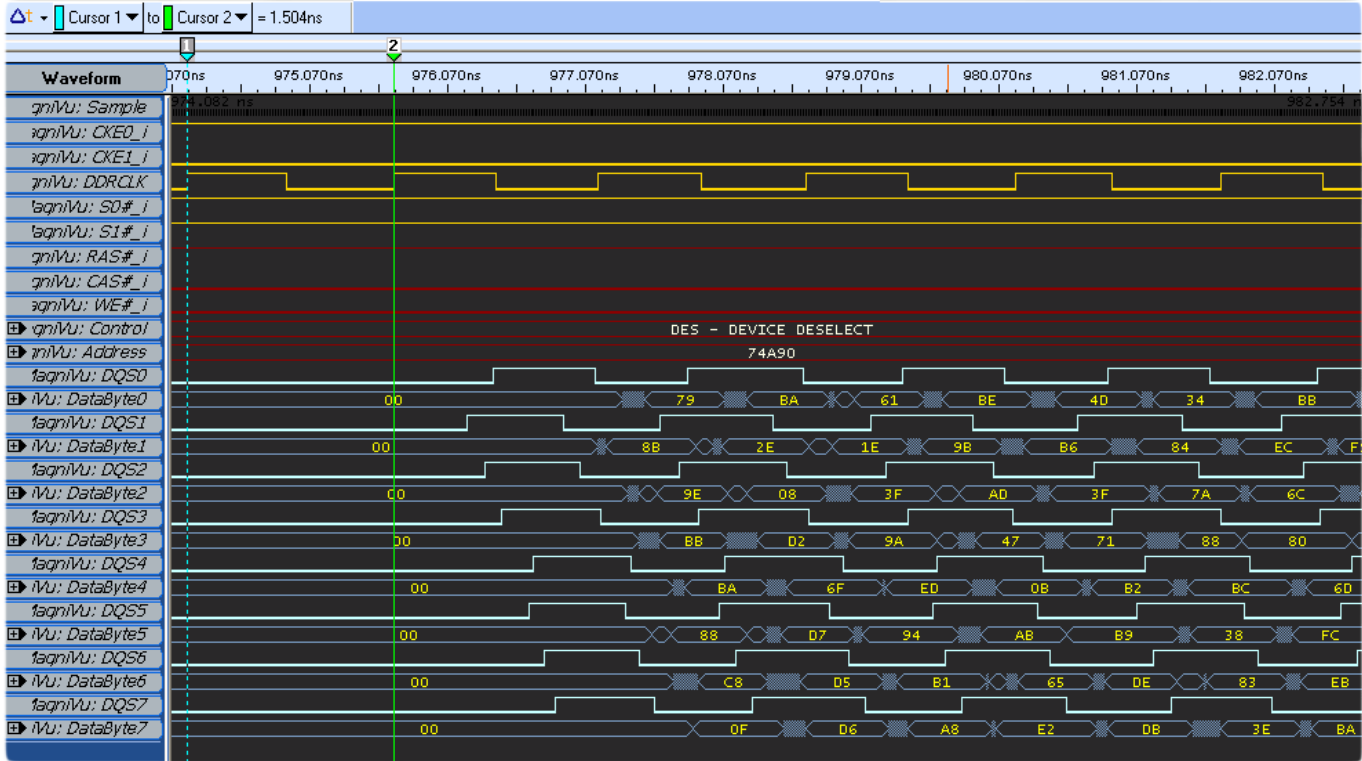
Nexus Technology has designed this interposer to have a minimal effect in your target. As with any interposer solution, approximately one inch of trace length will be added between your target and the SODIMM. Depending on the target layout, memory controller, SODIMM type and SODIMM socket being probed, an interposer may affect the performance of your system. All users are given 30 days to qualify the interposer in their system. Should performance issues arise it is important to know that alternate solutions are available. Nexus Technology offers NEXVu SO-VDIMMs which provide both optimal probe points (at the memory components) and no added trace length or interposer effects. Also available are memory component products which also provide optimal probe points, extremely small added trace lengths, and extremely small interposer effects.

## Performance You Can See™



DDR3-1600 State Decode

# Performance You Can See™ (cont.)



DDR3-1600 MagniVu Write Timing



DDR3-1600 MagniVu Reads Timing

## Tektronix Hardware Requirements

DDR Speed	Acquisition	Mainframe Required	Module(s) Required	Probes Required
DDR3-1600	Cmd/Address Read <b>and</b> Write	TLA7000	2- TLA7BB4 1.4GHz	4- Tektronix P6960HCD
DDR3-1333 DDR3-1067 DDR3-800	Cmd/Address Read <b>and</b> Write	TLA7000	1- TLA7BB4 750MHz (or 1.4GHz)	4- Nexus NEX-PRB1XL

## Product Configuration Table

Nomenclature	Nexus Probes Included	Nexus Hardware Included	Nexus Software Included
NEX-SODDR3INTR-HS	No–Note 1	1- DDR3-1600 SODIMM Slot Interposer	1- TLA Setup & Protocol Decode Support Packages w/MR Technology™ 1- NEX-DDR3SPA Data Threshold & Sample Point Analysis 1- NEX-DDR-PROTOCOL Protocol Violation
NEX-SODDR3INTR-HS-PR2	Yes-Note 1	1- DDR3-1600 SODIMM Slot Interposer 4- NEX-PRB1XL	1- TLA Setup & Protocol Decode Support Packages /wMR Technology™ 1- NEX-DDR3SPA Data Threshold & Sample Point Analysis 1- NEX-DDR-PROTOCOL Protocol Violation
NEX-SODDR3INTRHS-UPG-MRT	No	None – Note 2	1- TLA Setup & Protocol Decode Support Packages w/MR Technology™

**Note 1:** Two Nexus Technology NEX-PRB1XL probes and two Nexus Technology NEX-PRB2XL probes can be used at/up to DDR3-1333 and can be ordered as a complete package as shown in the table above. Two Tektronix P6960HCD probes and two Tektronix P6962HCD probes are required for DDR3-1600 and must be purchased from Tektronix.

**Note 2:** Proof of purchase of a NEX-SODDR3INTR-HS or NEX-SODDR3INTR-HS-PR on or before 12/17/2009 necessary to purchase this product. Qualifying customers who purchased a NEX-SODDR3INTR-HS or NEX-SODDR3INTR-HS-PR on or after 10/1/2009 and on or before 12/23/2009 can obtain this product at no additional charge.

## Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST.

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