

# DDR3-1600 SODIMM NEXVu Products

Premier SODIMM Digital Validation



DDR3-1600 SODIMM NEXVu products allow for logic analyzer acquisition of command, address, read and write data of 204-pin, unbuffered DDR3-1600. These products also support slower speeds of DDR3, including DDR3-1333, DDR3-1067, and DDR3-800. The following SODIMMs are supported: PC3-12800, PC3-10600, PC3-8500, and PC3-6400.



## Premier NEXVu VDIMM Design

Optimal DDR3 validation requires analysis of the DDR3 signals, as seen by the memory components. This allows for the highest confidence that the signals captured are representative, contain little interference, and present the maximum possible data eye size. NEXVu VDIMMs are standard DDR3 SODIMMs with built in logic analyzer probe points. This design allows for logic analyzer probing of the DDR3 signals extremely close to the memory components.

NEXVu VDIMMs are designed to JEDEC DDR3 Raw Card standards. These standards, published only after stringent JEDEC committee review, provide an extremely robust platform which the entire memory industry relies upon for their DDR3 DIMM designs.



All NEXVu VDIMMs are available with or without DDR3 component sockets. These sockets allow for the quick swapping & testing of different memory components on the NEXVu. The NEXVu Sockets Quick Start Guide provides more information.



## Software

All NEXVu VDIMMs come with logic analyzer setup software, DDR3 protocol decode software, DDR3 data eye sample point analysis software, and protocol violation software.

### Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions for easy display and logic analyzer triggering/filtering.

### Data Sample Point Analysis Software

In order for the logic analyzer to capture data, the DDR3 signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDR3 data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes are purposely skewed - as per the DDR3 specification - on a byte basis relative to the DDR clock. The valid eyes also contain skew (again relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

These, among other factors, make reliable and accurate DDR3 read and write data bus acquisition extremely difficult - if done manually. [NEX-DDR3-SPA](#), provided free, automates this process

Time	Setup	Lock
10	48.35 %	3.75
11	48.65 %	3.51
12	48.81 %	3.51
13	48.47 %	3.77
14	48.25 %	3.52
15	48.70 %	3.72
16	51.43 %	3.3
17	48.48 %	3.78
18	52.84 %	3.78
19	50.23 %	3.84
20	48.72 %	3.77

enabling quick and reliable DDR3 read and write data bus acquisition in only minutes. For more information, please see the [NEX-DDR3-SPA](#) product page on our website.

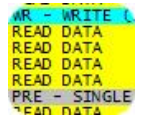
## Protocol Violation Software



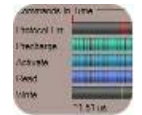
There's a **BIG** difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Please see the [NEX-DDR-PROTOCOL](#) product for more information.

## Digital Validation

Logic analyzer setup software (TLA support package) is included with these products. This setup software acquires/reconstructs the 800MHz command/address bus and acquires/reconstructs the 1,600MT/s read/write data from the data bus. The software also decodes and displays the bus protocol, shows the valid read/write data and provides easy DDR protocol triggering to quickly capture relevant data.



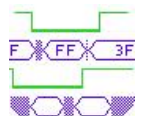
These products also come with the NEX-DDR-PROTOCOL software tool. This software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs basic protocol violation checking. Advanced protocol violation checking is available for purchase separately. Please see the [NEX-DDR-PROTOCOL](#) product for more information on this powerful tool.



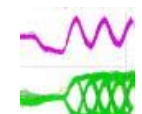
## Analog Validation

Although these NEXVu VDIMMs are designed for optimal digital validation, there are a number of useful features and tools available to assist in the analog validation process.

The most readily available tool is the Tektronix Logic Analyzer's 20ps (50GHz) MagniVu timing. This 2.5us deep acquisition space, separate from state acquisition memory is simultaneously acquired with state data, and is typically filled with bus activity that occurred around the state trigger. A wealth of analog information can be found in this data, including: positive/negative pulse widths, signal skew, and data glitches. Activity that appears too short, too long, unreasonably skewed relative to another signal, or that contains glitches are indications that there is an analog characteristic of that signal that deserves further attention.



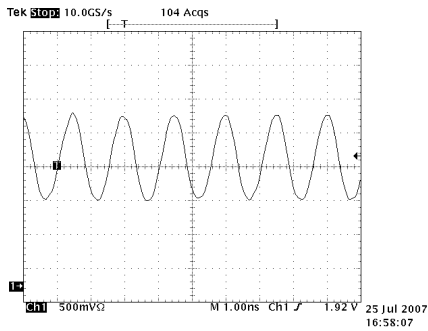
Another powerful analog validation feature is the Tektronix Logic Analyzer's Analog Mux capability. When paired with an oscilloscope, this feature enables analog visibility of every DDR3 signal probed by the NEXVu. Any of the ten or so command bits, sixteen-plus address bits and any of the 64-/72- data bits can be viewed on an oscilloscope in seconds and - literally - with a touch of a button. This feature comes with two significant limitations. First, there is no calibration specification for the channel-to-channel skew through the Analog Mux. Second, the signals are bandwidth limited to 3GHz. This limitation acts as a high speed filter, limiting the visibility of the signal's harmonics that are over 3GHz. For DDR3-1600, this filtering will cause artificial increases in the slew rates which appears as rising/falling edges that take longer to transition. The effect on the data eyes will be similar, showing a rounding effect. Although these limitations force the user to find alternate methods (see our [DDR3 Component Interposers](#)) for accurate DDR3-1600 analog validation, the importance of this tool for preliminary analog validation can not be understated. The ability of an digital validation engineer to



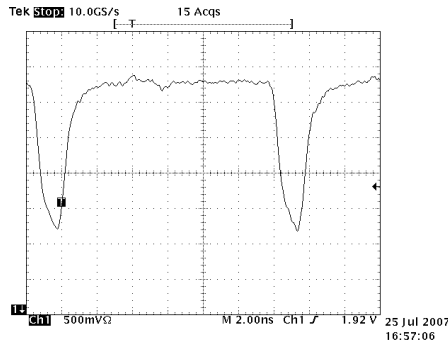
quickly and easily assess the general analog health of a target can save an enormous amount of time and resources.

Tektronix discusses some of these topics in more detail in the application note, Debugging Timing Problems with a Logic Analyzer available for download from [tek.com](http://tek.com). Nexus Technology recommends these products for the debugging methods and practices described in this application note.

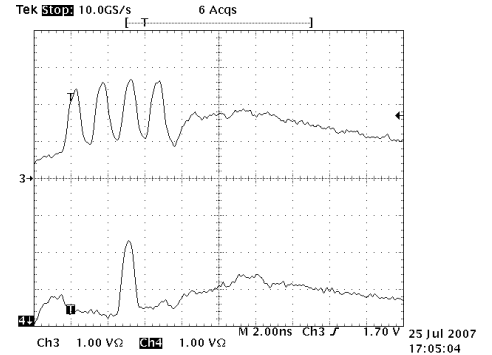
## Performance You Can See®



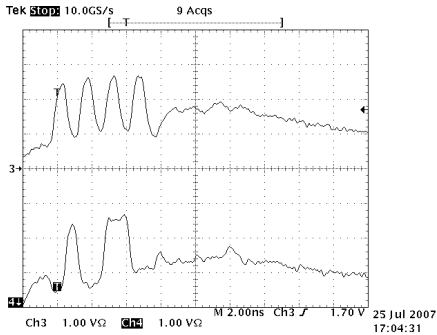
Clock 0 (CK0)



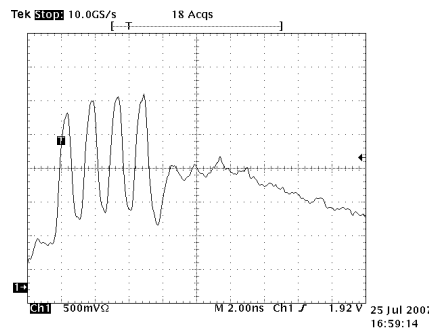
Chip Select 0 (S0#)



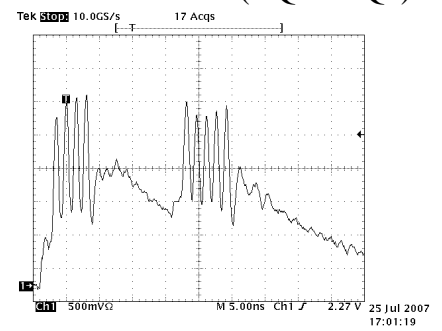
Strobe0/Data0 (DQS0/DQ0)



Strobe0/Data0 (DQS0/DQ0)



Strobe3 (DQS3)



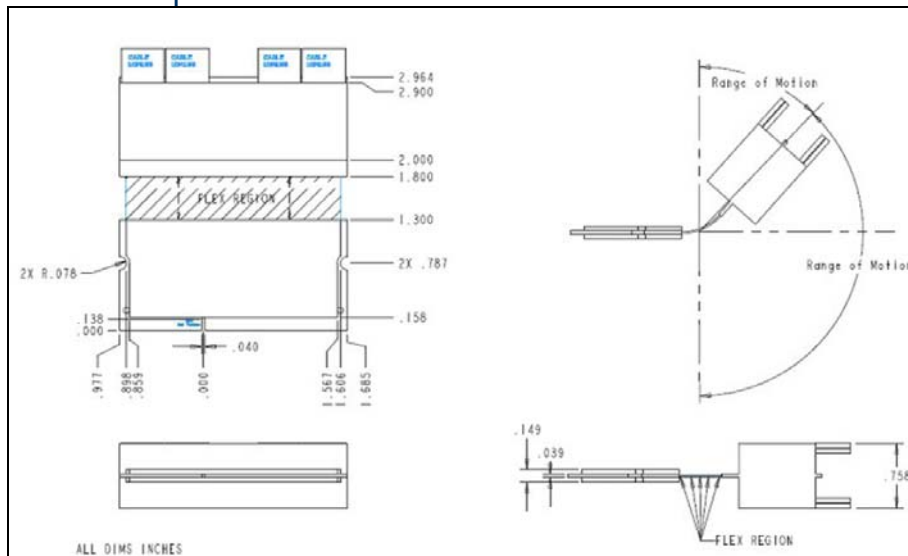
Strobe3 (DQS3)

## Product Configuration Table

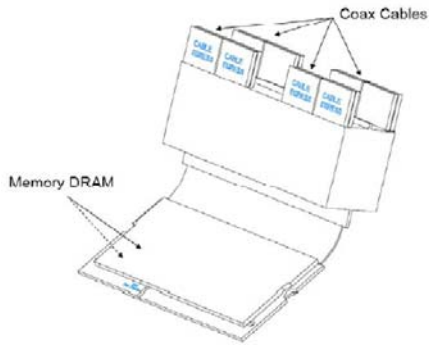
Nomenclature	DDR Speed	Memory Configuration	Raw Card Supported	Requirements
NEX-SONV316X16DRSK0U	DDR3-1600	Sockets & Memory Components-Note 1	A – Unbuffered x16, Dual Rank	1- TLA7000 Series Mainframe
NEX-SONV316X16DR1GU	DDR3-1600	Memory Components	A – Unbuffered x16, Dual Rank	4- TLA7Bx4 1.4GHz 4- P6962HCD
NEX-SONV313X8DRSK0U	DDR3-1333	Sockets & Memory Components-Note 1	F – Unbuffered x8, Dual Rank	1- TLA7000 Series Mainframe
NEX-SONV313X8DR2GU	DDR3-1333	Memory Components	F – Unbuffered x8, Dual Rank	2- TLA7Bx4
NEX-SONV313X16DRSK0U	DDR3-1333	Sockets & Memory Components-Note 1	A – Unbuffered x16, Dual Rank	750MHz 4- NEX-PRB2X
NEX-SONV313X16DR1GU	DDR3-1333	Memory Components	A – Unbuffered x16, Dual Rank	
NEX-SONV310X8DRSK0U	DDR3-1067	Sockets & Memory Components-Note 1	F – Unbuffered x8, Dual Rank	
NEX-SONV310X8DR2GU	DDR3-1067	Memory Components	F – Unbuffered x8, Dual Rank	
NEX-SONV310X16DRSK0U	DDR3-1067	Sockets & Memory Components-Note 1	A – Unbuffered x16, Dual Rank	
NEX-SONV310X16DR1GU	DDR3-1067	Memory Components	A – Unbuffered x16, Dual Rank	

**Note 1:** The socket configuration will exceed the keep-out-volume in targets with standard SODIMM connector to system board spacing. Options are available to ensure interoperability. Please [contact us](#) for more information.

## Probe Keep-Out Volume



## Probe Egress



## Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST.

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