



# **NEX-563XX**

## **Disassembly Software Users Manual**

**Including these Software Support packages:**

**563XX18**

**563XX24**

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## **1.0 OVERVIEW**

### **1.1 General Information**

The NEX-563XX disassembly software provides disassembly of acquired Motorola 563XX DSP bus cycles using a TLA600/700 102-channel or 136-channel acquisition module. The NEX-563XX support is software only. Please see Section 3.0 “Connecting to a 563XX Target” for information on probing.

The NEX-563XX provides full instruction decoding of 563XX DSP instructions. Note that two different supports are included. One, NEX-563XX18, is to be used with 563XX variants that have an 18-bit external address bus. The other, NEX-563XX24, is to be used with variations that have a 24-bit external data bus. Both versions shall be referred to generically as NEX-563XX support except when particular distinctions need to be pointed out.

Note that at the present time 8-bit instruction fetch decode is not supported.

This manual assumes that the user is familiar with the 563XX DSP series' specifications and the Tektronix TLA600/700 Logic Analyzer. It is also expected that the user is familiar with Windows 95. The TLA600/700 Application must also be at V1.1 or later for the NEX-563XX support to work properly.

## **2.0 SOFTWARE INSTALLATION**

Two 3½” diskettes have been included with the NEX-563XX disassembly product, and they contain the software support for the Logic Analyzer. The NEX-563XX18 support is for 18-bit address variants; the NEX-563XX24 is for those versions that have a 24-bit external address bus. The version to be used should be loaded in the same method as other Windows programs. Place the NEX-563XX18 (or NEX-563XX24) Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the 563XX support in its proper place on the hard disk.

To load the support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose 563XX18 for 18-bit address support, or 563XX24 for 24-bit address support, and then click on **Okay**.

## **3.0 CONNECTING TO A 563XX TARGET**

### **3.1 General**

When possible it is recommended that the user add Mictor connectors to their target for the interface to the TLA600/700 using Tektronix P6434 high-density probes. Compression pads should be added to the target if Tektronix P6860 probes will be used. Table 1 shows the wiring and Channel Grouping required for NEX-563XX support.

Group Name	563XX Signal	TLA600/700 input	Group Name	563XX Signal	TLA600/700 input
Address (Hex)	A23 <sup>1</sup>	A2:7	Data (Hex)	D23	D2:7
	A22 <sup>1</sup>	A2:6		D22	D2:6
	A21 <sup>1</sup>	A2:5		D21	D2:5
	A20 <sup>1</sup>	A2:4		D20	D2:4
	A19 <sup>1</sup>	A2:3		D19	D2:3
	A18 <sup>1</sup>	A2:2		D18	D2:2
	A17	A2:1		D17	D2:1
	A16	A2:0		D16	D2:0
	A15	A1:7		D15	C1:7
	A14	A1:6		D14	C1:6
	A13	A1:5		D13	C1:5
	A12	A1:4		D12	C1:4
	A11	A1:3		D11	C1:3
	A10	A1:2		D10	C1:2
	A9	A1:1		D9	C1:1
	A8	A1:0		D8	C1:0
	A7	A0:7		D7	C0:7
	A6	A0:6		D6	C0:6
	A5	A0:5		D5	C0:5
	A4	A0:4		D4	C0:4
A3	A0:3	D3	C0:3		
A2	A0:2	D2	C0:2		
A1	A0:1	D1	C0:1		
A0	A0:0	D0	C0:0		
CasAddr (Hex)	CAS11	D1:3 <sup>2</sup>	Control (Sym)	RESET~	C2:0
	CAS10	D1:2 <sup>2</sup>		BG~	C2:3
	CAS9	D1:1 <sup>2</sup>		WR~	C2:2
	CAS8	D1:0 <sup>2</sup>		RD~	C2:1
	CAS7	D0:7 <sup>2</sup>	Misc (Off)	CLKOUT	Clock:3
	CAS6	D0:6 <sup>2</sup>		CAS~	Clock:2
	CAS5	D0:5 <sup>2</sup>		AA3_RAS3~	Qual:1
	CAS4	D0:4 <sup>2</sup>		AA2_RAS2~	Qual:0
	CAS3	D0:3 <sup>2</sup>		AA1_RAS1~	Clock:1
	CAS2	D0:2 <sup>2</sup>		AA0_RAS0~	Clock:0
	CAS1	D0:1 <sup>2</sup>			
	CAS0	D0:0 <sup>2</sup>			

**Table 1-NEX-563XX18/24 TLA600/700 Wiring**

Notes:

- 1) These signals are only needed for 24-bit address support
- 2) It is not necessary to connect these signals. Data will be acquired using Demux mode.

## **4.0 CLOCK SELECTION**

### **4.1 General Information**

There are five clocking options available when using a NEX-563XX support package. Each is explained in detail below.

The clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the proper operating mode in the **DRAM Banks** select field.

### **4.2 Clocking Options - Explanation**

**None** - This is the default clocking selection. In this mode the software treats the AA0-3~ signals as selects to Static RAM memory. In this mode, CLKOUT, RD~, and WR~ are the necessary signals for acquiring bus cycle data.

**AA0**

**AA1**

**AA2**

**AA3** - These modes indicate that the selected signal (AA0~, AA1~, AA2~, or AA3~) is connected to a DRAM memory bank as a RAS~ signal. All other AAx~ signals are assumed to be connected to Static memory. In these modes, the selected AAx~ signal and CAS~ are also required for proper bus cycle data acquisition, in addition to the three signals mentioned above.

## **5.0 VIEWING DATA**

### **5.1 Viewing Timing Data on the TLA600/700**

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: 563XX and 563XX-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, 563XX-MagniVu, will show all of the channels in 2GHz MagniVu mode when using a TLA7X3/4 module and 8GHz MagniVu mode when using a TLA7AX3/4 module, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

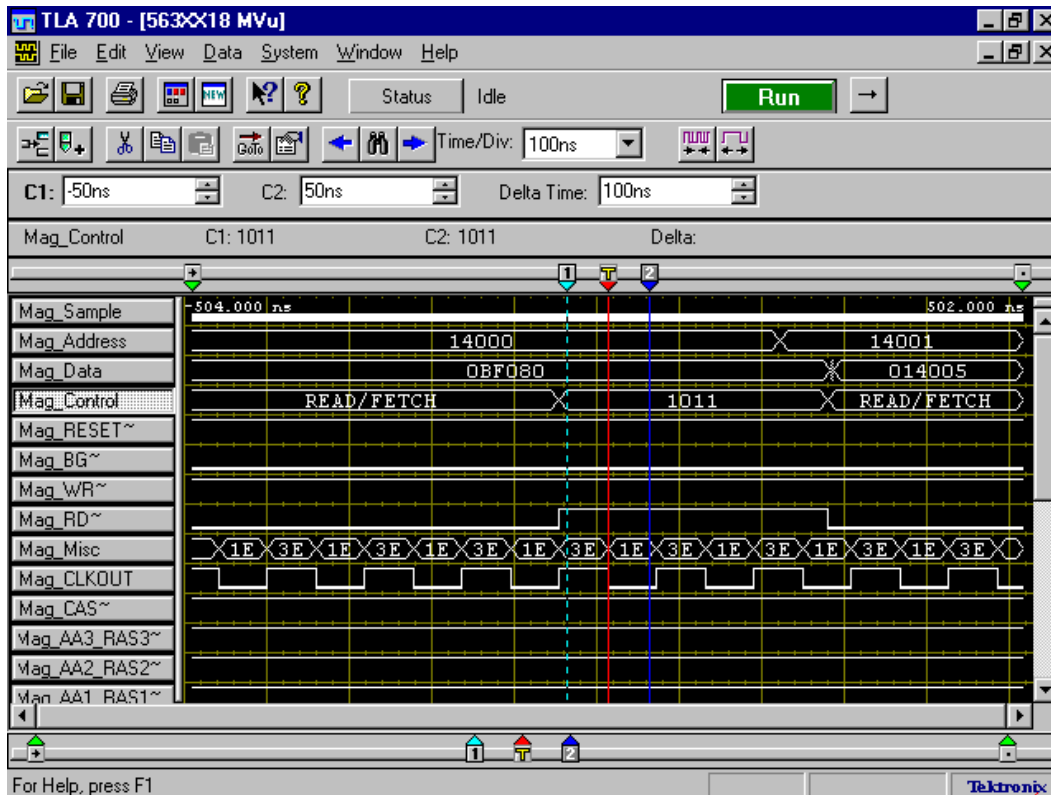


Figure 1- 563XX MagniVu Display on TLA600/799

## 6.0 USING THE DISASSEMBLY SOFTWARE

### 6.1 General

The NEX-563XX support software acquires and decodes Motorola 563XX DSP bus activity and displays the information as assembly language mnemonics (machine code) - see Figure 2. This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types of interest to the software engineer (Figure 3). The user can choose to display the acquired data in Hardware, Software, Control Flow, or Subroutine modes.

A major feature of the NEX-563XX software is its ability to intelligently acquire bus cycle information. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the 563XX software is able to acquire only the valid 563XX bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more microprocessor bus cycles.

Every stored cycle (bus or clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps when using a TLA7X3/4 module and 125ps

when using a TLA7AX3/4 module, permits precise measurements of microprocessor bus activity. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

## 6.2 Disassembly Using the TLA600/700

The TLA600/700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

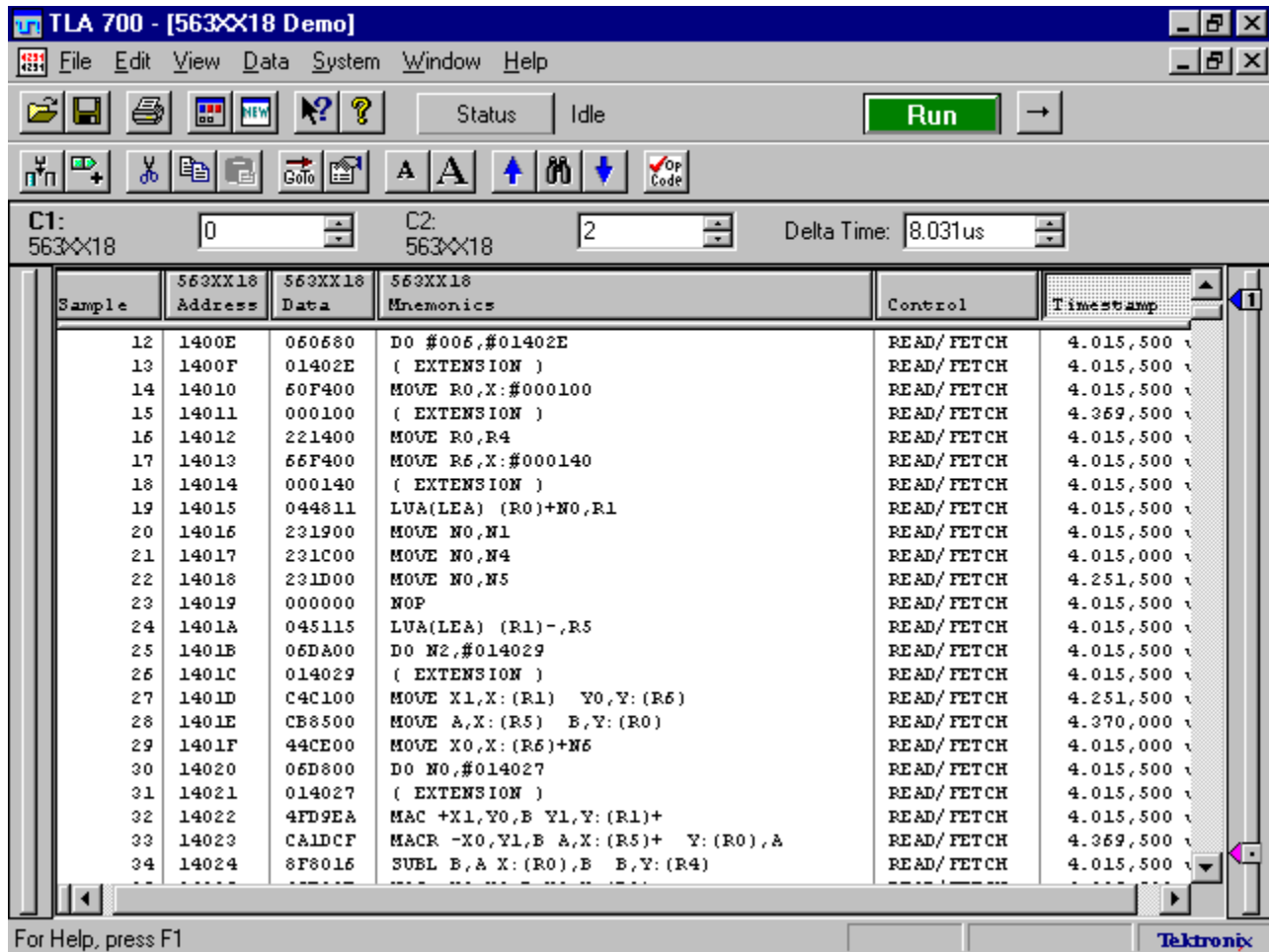


Figure 2- 563XX Disassembly

The other column of interest is the Mnemonics column, where the 563XX disassembly information is displayed. As mentioned previously, it is possible to filter the 563XX instructions that are displayed. This is done via selections made in the Disassembly tab of the Properties window (see Figure 3). By default the display is in Hardware mode, where all bus cycles are displayed (Memory Reads, Memory Writes, Instructions, etc.). Other choices are: Software (only executed instructions are displayed), Control Flow (display of instructions affecting code flow such as Jumps, Branches, etc.), and Subroutine (only instructions such as Calls, Returns, etc. are displayed).

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

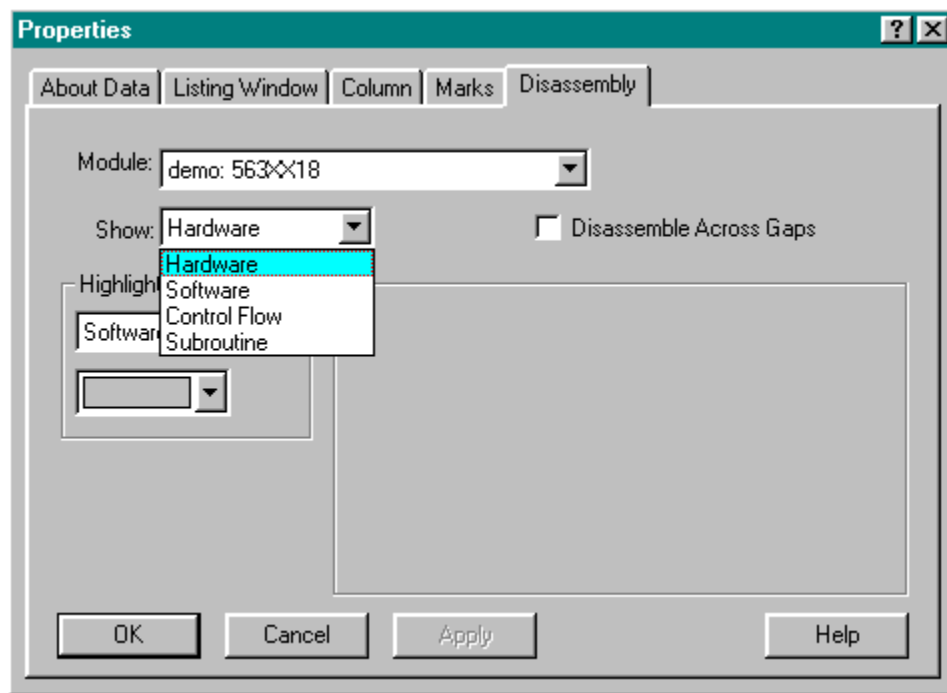
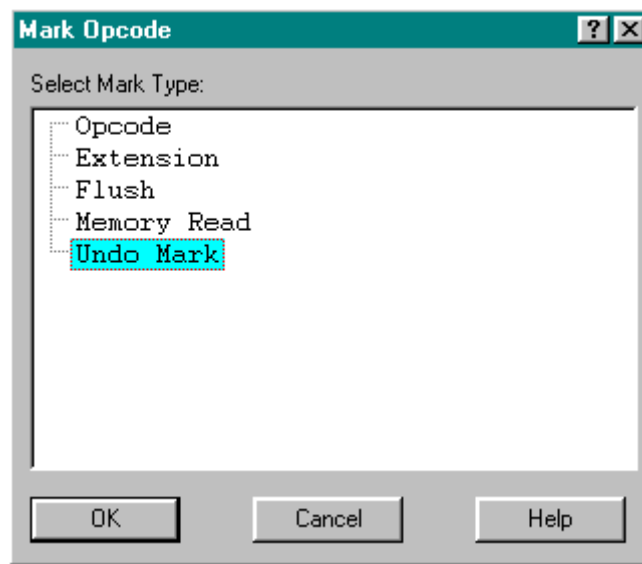


Figure 3- Disassembly Display Filter Window

### 6.3 Help! The Disassembler's Confused (or: Using Mark Opcode)

Because the 563XX series does not have a signal to denote an opcode fetch, it is difficult to distinguish between a Read cycle and an Opcode Fetch. The disassembly software does the best it can to figure this out, but it assumes that every Read from contiguous memory cycles is a Fetch, and this may not always be the case. When this happens the user can Mark an Opcode (a Sample or Cycle in the List display) to help the disassembler re-synchronize. To do this, the user first moves the mouse cursor to the cycle that is to be marked. Click on the right mouse button to bring up the menu selections, then click on Mark Opcode. Another window will appear (see Figure 4) which permits selecting the type of cycle that is to be marked (Opcode Fetch, Memory Read, etc.). Select the desired cycle and then click on Okay. To remove an existing Mark, select Undo Mark and then click on OK.



**Figure 4- Mark Opcode Window**

## 6.4 Instruction Decoding/Addressing Modes Supported

The following lists the particular feature sets that the NEX-563XX disassembler packages supports:

Supports Parallel and Non-parallel instructions.

Addressing modes supported:

Register Direct:

- Data or Control Register Direct
- Address Register Direct

Address Register Indirect:

- |                              |            |
|------------------------------|------------|
| - No Update                  | (Rn)       |
| - Postincrement By 1         | (Rn)+      |
| - Postdecrement By 1         | (Rn)-      |
| - Postincrement By Offset Nn | (Rn)+Nn    |
| - Postdecrement By Offset Nn | (Rn)-Nn    |
| - Indexed By Offset Nn       | (Rn+Nn)    |
| - Predecrement By 1          | -(Rn)      |
| - Short displacement         | (Rn+short) |
| - Long displacement          | (Rn+long)  |

PC Relative:

- Short Displacement PC Relative
- Long Displacement PC Relative
- Address Register PC Relative

Special Addressing Modes:

- Immediate Data
- Immediate Short Data
- Absolute Address
- Absolute Short Address
- Short Jump Address
- I/O Short Address
- Implicit Reference

## 6.5 Instructions supported:

### Data Move Instructions

(.....)	<NO MOVE>
(.....) #xx,D	<IMMEDIATE SHORT>
(.....) S,D	<REGISTER TO REGISTER>
(.....) ea	<Address Register Update>

### X Memory Data Moves

(.....) X:ea,D	<EFFECTIVE>
(.....) X:aa,D	<ABSOLUTE>
(.....) S,X:ea	<EFFECTIVE>
(.....) S,X:aa	<ABSOLUTE>
MOVE X:(Rn+xxx),D	<RELATIVE>
MOVE X:(Rn+xxxx),D	<RELATIVE>
MOVE D,X:(Rn+xxx)	<RELATIVE>
MOVE D,X:(Rn+xxxx)	<RELATIVE>

### X Memory and Register Data Move

(.....) X:ea,D1 S2,D2	<EFFECTIVE>
(.....) S1,X:ea S2,D2	<EFFECTIVE>
(.....) #xxxxxx,D1 S2,D2	<IMMEDIATE>
(.....) A->X:ea X0->A	<EFFECTIVE>
(.....) B->X:ea X0->B	<EFFECTIVE>

### Y Memory Data Moves

(.....) Y:ea,D	<EFFECTIVE>
(.....) Y:aa,D	<ABSOLUTE>
(.....) S,Y:ea	<EFFECTIVE>
(.....) S,Y:aa	<ABSOLUTE>
MOVE Y:(Rn+xxx),D	<RELATIVE>
MOVE Y:(Rn+xxxx),D	<RELATIVE>
MOVE D,Y:(Rn+xxx)	<RELATIVE>
MOVE D,Y:(Rn+xxxx)	<RELATIVE>

### Y Memory and Register Data Move

(.....) S1,D1 Y:ea,D2	<EFFECTIVE>
(.....) S1,D1 S2,Y:ea	<EFFECTIVE>
(.....) S1,D1 #xxxxxx,D2	<IMMEDIATE>
(.....) Y0->A A->Y:ea	<EFFECTIVE>
(.....) Y0->B B->Y:ea	<EFFECTIVE>

### Long Data Memory Move

(.....) L:ea,D	<EFFECTIVE>
(.....) L:aa,D	<ABSOLUTE>
(.....) S,L:ea	<EFFECTIVE>
(.....) S,L:aa	<ABSOLUTE>

### XY Memory Data Move

(.....) X:<eax>,D1 Y:<eay>,D2
(.....) X:<eax>,D1 S2,Y:<eay>
(.....) S1,X:<eax> Y:<eay>,D2
(.....) S1,X:<eax> S2,Y:<eay>

### Parallel Instructions

ABS D	<EFFECTIVE>
ADC S,D	<EFFECTIVE>
ADD S,D	<EFFECTIVE>
ADDL S,D	<EFFECTIVE>
ADDR S,D	<EFFECTIVE>
AND S,D	<EFFECTIVE>
ASL D	<EFFECTIVE>
ASR D	<EFFECTIVE>
CLR D	<EFFECTIVE>
CMP S1,S2	<EFFECTIVE>
CMPM S1,S2	<EFFECTIVE>
EOR S,D	<EFFECTIVE>
LSL D	<EFFECTIVE>
LSR D	<EFFECTIVE>
MAX A,B	<EFFECTIVE>
MAXM A,B	<EFFECTIVE>
MAC (+-)S1,S2,D	<EFFECTIVE>
MACR (+-)S1,S2,D	<EFFECTIVE>
MOVE(NOP)	
MPY (+-)S1,S2,D	<EFFECTIVE>
MPYR (+-)S1,S2,D	<EFFECTIVE>
NEG D	<EFFECTIVE>
NOT D	<EFFECTIVE>
OR S,D	<EFFECTIVE>
RND D	<EFFECTIVE>
ROL D	<EFFECTIVE>

ROR D	<EFFECTIVE>
SBC S,D	<EFFECTIVE>
SUB S,D	<EFFECTIVE>
SUBL S,D	<EFFECTIVE>
SUBR S,D	<EFFECTIVE>
TFR S,D	<EFFECTIVE>
TST S	<EFFECTIVE>

#### Other Instructions

ADD #xxxxxx,D	<IMMEDIATE>
ADD #xx,D	<IMMEDIATE>
AND #xxxxxx,D	<IMMEDIATE>
AND #xx,D	<IMMEDIATE>
AND(I)	<IMMEDIATE>
ASL #ii,S2,D	<IMMEDIATE>
ASL S1,S2,D	
ASR #ii,S2,D	<IMMEDIATE>
ASR S1,S2,D	
Bcc Rn	
Bcc xxx	<RELATIVE>
Bcc xxxx	<RELATIVE>
BCHG #n,[XorY]:aa	<ABSOLUTE>
BCHG #n,[XorY]:ea	<EFFECTIVE>
BCHG #n,[XorY]:pp	<IO SHORT>
BCHG #n,[XorY]:qq	<IO SHORT>
BCHG #n,D	
BCLR #n,[XorY]:aa	<ABSOLUTE>
BCLR #n,[XorY]:ea	<EFFECTIVE>
BCLR #n,[XorY]:pp	<IO SHORT>
BCLR #n,[XorY]:qq	<IO SHORT>
BCLR #n,D	
BRA Rn	
BRA xxx	<RELATIVE>
BRA xxxx	<RELATIVE>
BRCLR #n	<RELATIVE>
BRCLR #n,[XorY]:aa,xxxx	<RELATIVE>
BRCLR #n,[XorY]:ea,xxxx	<RELATIVE>
BRCLR #n,[XorY]:pp,xxxx	<RELATIVE>
BRCLR #n,[XorY]:qq,xxxx	<RELATIVE>
BRCLR #n,S,xxxx	<RELATIVE>
BRKcc	
BRSET #n,[XorY]:aa,xxxx	<RELATIVE>
BRSET #n,[XorY]:ea,xxxx	<RELATIVE>
BRSET #n,[XorY]:pp,xxxx	<RELATIVE>
BRSET #n,[XorY]:qq,xxxx	<RELATIVE>
BRSET #n,S,xxxx	<RELATIVE>
BScC Rn	
BScC xxx	<RELATIVE>

BScC xxxx	<RELATIVE>
BSCLR #n,[XorY]:aa,xxxx	<RELATIVE>
BSCLR #n,[XorY]:ea,xxxx	<RELATIVE>
BSCLR #n,[XorY]:pp,xxxx	<RELATIVE>
BSCLR #n,[XorY]:qq,xxxx	<RELATIVE>
BSCLR #n,S,xxxx	<RELATIVE>
BSET #n,[XorY]:aa	<ABSOLUTE>
BSET #n,[XorY]:ea	<EFFECTIVE>
BSET #n,[XorY]:pp	<IO SHORT>
BSET #n,[XorY]:qq	<IO SHORT>
BSET #n,D	
BSR Rn	
BSR xxx	<RELATIVE>
BSR xxxx	<RELATIVE>
BSSET #n,[XorY]:aa	<ABSOLUTE>
BSSET #n,[XorY]:ea	<EFFECTIVE>
BSSET #n,[XorY]:pp	<IO SHORT>
BSSET #n,[XorY]:qq	<IO SHORT>
BSSET #n,D	
BTST #n,[XorY]:aa	<ABSOLUTE>
BTST #n,[XorY]:ea	<EFFECTIVE>
BTST #n,[XorY]:pp	<IO SHORT>
BTST #n,[XorY]:qq	<IO SHORT>
BTST #n,D	
CLB S,D	
CMP #xx,S2	<IMMEDIATE>
CMP #xxxxxxx,S2	<IMMEDIATE>
CMPU S1,S2	
DEBUG	
DEBUGcc	
DEC D	
DIV S,D	
DMACss (+-)S1,S2,D	
DMACsu (+-)S1,S2,D	
DMACuu (+-)S1,S2,D	
DO #xxx,expr	<ABSOLUTE>
DO S,expr	<ABSOLUTE>
DO [XorY]:aa,expr	<ABSOLUTE>
DO [XorY]:ea,expr	<ABSOLUTE>
DO FOREVER,expr	<ABSOLUTE>
DOR #xxx,label	<RELATIVE>
DOR S,label	<RELATIVE>
DOR [XorY]:aa,label	<RELATIVE>
DOR [XorY]:ea,label	<RELATIVE>
DOR FOREVER,label	<RELATIVE>
ENDDO	
EOR #xx,D	<IMMEDIATE>
EOR #xxxxxxx,D	<IMMEDIATE>

EXTRACT #CO,S2,D	<CONTROL>
EXTRACT S1,S2,D	
EXTRACTU #CO,S2,D	<CONTROL>
EXTRACTU S1,S2,D	
IFcc	
IFcc.U	
ILLEGAL	
INC D	
INSERT #CO,S2,D	<CONTROL>
INSERT S1,S2,D	
Jcc ea	<EFFECTIVE>
Jcc xxx	
JCLR #n,[XorY]:aa,xxxx	<ABSOLUTE>
JCLR #n,[XorY]:ea,xxxx	< ABSOLUTE>
JCLR #n,[XorY]:pp,xxxx	< ABSOLUTE>
JCLR #n,[XorY]:qq,xxxx	< ABSOLUTE>
JCLR #n,S,xxxx	< ABSOLUTE>
JMP ea	<EFFECTIVE>
JMP xxx	
JSc ea	<EFFECTIVE>
JSc xxx	
JSCLR #n,[XorY]:aa,xxxx	<ABSOLUTE>
JSCLR #n,[XorY]:ea,xxxx	< ABSOLUTE>
JSCLR #n,[XorY]:pp,xxxx	< ABSOLUTE>
JSCLR #n,[XorY]:qq,xxxx	< ABSOLUTE>
JSCLR #n,S,xxxx	< ABSOLUTE>
JSET #n,[XorY]:aa,xxxx	<ABSOLUTE>
JSET #n,[XorY]:ea,xxxx	< ABSOLUTE>
JSET #n,[XorY]:pp,xxxx	< ABSOLUTE>
JSET #n,[XorY]:qq,xxxx	< ABSOLUTE>
JSET #n,S,xxxx	< ABSOLUTE>
JSR ea	<EFFECTIVE>
JSR xxx	
JSSET #n,[XorY]:aa,xxxx	<ABSOLUTE>
JSSET #n,[XorY]:ea,xxxx	< ABSOLUTE>
JSSET #n,[XorY]:pp,xxxx	< ABSOLUTE>
JSSET #n,[XorY]:qq,xxxx	< ABSOLUTE>
JSSET #n,S,xxxx	< ABSOLUTE>
LRA Rn,D	
LRA xxxx,D	<LONG>
LSL #i,D	
LSL S,D	
LSR #i,D	
LSR S,D	
LUA(LEA) (Rn+aa),D	
LUA(LEA) ea,D	
MAC (+-)S,#n,D	
MACI (+-)#xxxxxxx,S,D	<IMMEDIATE>

MACuu (+-)S1,S2,D	
MACsu (+-)S2,S1,D	
MACR (+-)S,#n,D	
MACRI (+-)#xxxxxx,S,D	<IMMEDIATE>
MERGE S,D	
MOVE(C) [XorY]:aa,D1	<ABSOLUTE>
MOVE(C) [XorY]:ea,D1	<EFFECTIVE>
MOVE(C) S1,[XorY]:aa	<ABSOLUTE>
MOVE(C) S1,[XorY]:ea	<EFFECTIVE>
MOVE(C) S1,D2	
MOVE(C) S2,D1	
MOVE(C) #xx,D1	<IMMEDIATE>
MOVE(C) #xxxxxx,D1	<IMMEDIATE>
MOVE(M) S,P:aa	<ABSOLUTE>
MOVE(M) S,P:ea	<EFFECTIVE>
MOVE(M) P:aa,D	<ABSOLUTE>
MOVE(M) P:ea,D	<EFFECTIVE>
MOVEP [XorY]:pp,D	<EFFECTIVE>
MOVEP [XorY]:qq,D	<EFFECTIVE>
MOVEP [XorY]:pp,[XorY]:ea	<EFFECTIVE>
MOVEP [XorY]:qq,[XorY]:ea	<EFFECTIVE>
MOVEP [XorY]:pp,P:ea	<EFFECTIVE>
MOVEP [XorY]:qq,P:ea	<EFFECTIVE>
MOVEP S,[XorY]:pp	<EFFECTIVE>
MOVEP S,[XorY]:qq	<EFFECTIVE>
MOVEP [XorY]:ea,[XorY]:pp	<EFFECTIVE>
MOVEP [XorY]:ea,[XorY]:qq	<EFFECTIVE>
MOVEP P:ea,[XorY]:pp	<EFFECTIVE>
MOVEP P:ea,[XorY]:qq	<EFFECTIVE>
MPY (+-)S,#n,D	
MPYuu (+-)S1,S2,D	
MPYsu (+-)S2,S1,D	
MPYI (+-)#xxxxxx,S,D	<IMMEDIATE>
MPYR (+-)S,#n,D	
MPYRI (+-)#xxxxxx,S,D	<IMMEDIATE>
NORM Rn,D	
NORMF S,D	
OR #xx,D	<IMMEDIATE>
OR #xxxxxx,D	<IMMEDIATE>
OR(I) #xx,D	<IMMEDIATE>
PFLUSH	
PFLUSHUN	
PFREE	
PLOCKR xxxx	<EXTENSION>
PUNLOCK ea	<EXTENSION>
PUNLOCKR xxxx	<EXTENSION>
REP #xxx	<IMMEDIATE>
REP S	

REP [XorY]:aa	<ABSOLUTE>
REP [XorY]:ea	<EFFECTIVE>
RESET	
RTI	
RTS	
STOP	
SUB #xx,D	<IMMEDIATE>
SUB #xxxxxx,D	<IMMEDIATE>
Tcc S1,D1	
Tcc S1,D1 S2,D2	
Tcc S2,D2	
TRAP	
TRAPcc	
WAIT	

## **7.0 THE NEX-563XX CONTROL GROUP SYMBOL TABLE**

The use of Symbol Tables when displaying state data and defining a trigger enables the user to quickly determine the type of bus cycle that occurred or is desired. A symbol table for the Control group (563XX\_Ctrl, Table 2) has been provided to quickly show the type of bus transaction acquired when viewing data in Listing display. This same symbol table can be used in the Trigger area of the TLA to easily define the sort of bus cycle that is to be triggered on.

<b>Pattern</b>	<b>TLA700 Symbols</b>	<b>Meaning</b>
1x10	READ/FETCH	Memory Read or Fetch Cycle
1x01	WRITE	Memory Write Cycle
0xxx	RESET	Target Reset

**Table 2- NEX-563XX Control Symbol Table**

Signals, from left to right: RESET~, BG~, WR~, RD~

## **APPENDIX A - NEX-563XX Mictor Pinout**

The following Mictor wiring must be followed if the NEX-563XX disassembly software is to be used. Please refer to the Tektronix P6434 Mass Termination Probe Instruction Manual for further information on designing the Mictor connectors into your target. TLA inputs that are blank in the 563XX Signal columns are unassigned, and may be connected to any target signal desired. The 563XX Pin # column is blank so that the appropriate pin number can be filled in by the user. The signal pinout for the various 563XX devices is listed in Appendix C.

<b>Tek Mictor Pin #</b>	<b>AMP Mictor Pin #</b>	<b>TLA Channel</b>	<b>563XX Signal</b>	<b>563XX Pin #</b>	<b>Tek Mictor Pin #</b>	<b>AMP Mictor Pin #</b>	<b>TLA Channel</b>	<b>563XX Signal</b>	<b>563XX Pin #</b>
3	5	CK0	AA0~		36	6	CK1	AA1~	
4	7	A3:7			35	8	A1:7	A15	
5	9	A3:6			34	10	A1:6	A14	
6	11	A3:5			33	12	A1:5	A13	
7	13	A3:4			32	14	A1:4	A12	
8	15	A3:3			31	16	A1:3	A11	
9	17	A3:2			30	18	A1:2	A10	
10	19	A3:1			29	20	A1:1	A9	
11	21	A3:0			28	22	A1:0	A8	
12	23	A2:7	A23 <sup>2</sup>		27	24	A0:7	A7	
13	25	A2:6	A22 <sup>2</sup>		26	26	A0:6	A6	
14	27	A2:5	A21 <sup>2</sup>		25	28	A0:5	A5	
15	29	A2:4	A20 <sup>2</sup>		24	30	A0:4	A4	
16	31	A2:3	A19 <sup>2</sup>		23	32	A0:3	A3	
17	33	A2:2	A18 <sup>2</sup>		22	34	A0:2	A2	
18	35	A2:1	A17		21	36	A0:1	A1	
19	37	A2:0	A16		20	38	A0:0	A0	

### **Mictor Group A**

Notes:

- 1) All signals are required for disassembly.
- 2) These signals are needed for 24-bit address support only.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	563XX Signal	563XX Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	563XX Signal	563XX Pin #
3	5	CK3	CLKOUT		36	6	Q1	AA3~	
4	7	C3:7			35	8	C1:7	D15	
5	9	C3:6			34	10	C1:6	D14	
6	11	C3:5			33	12	C1:5	D13	
7	13	C3:4			32	14	C1:4	D12	
8	15	C3:3			31	16	C1:3	D11	
9	17	C3:2			30	18	C1:2	D10	
10	19	C3:1			29	20	C1:1	D9	
11	21	C3:0			28	22	C1:0	D8	
12	23	C2:7			27	24	C0:7	D7	
13	25	C2:6			26	26	C0:6	D6	
14	27	C2:5			25	28	C0:5	D5	
15	29	C2:4			24	30	C0:4	D4	
16	31	C2:3	BG~		23	32	C0:3	D3	
17	33	C2:2	WR~		22	34	C0:2	D2	
18	35	C2:1	RD~		21	36	C0:1	D1	
19	37	C2:0	RESET~		20	38	C0:0	D0	

### Mictor Group C

Notes:

- 1) All signals are required for disassembly.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	563XX Signal	563XX Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	563XX Signal	563XX Pin #
3	5	Q0	AA2~ <sup>1</sup>		36	6	CK2	CAS~ <sup>1</sup>	---
4	7	D3:7			35	8	D1:7	do not use <sup>2</sup>	---
5	9	D3:6			34	10	D1:6	do not use <sup>2</sup>	---
6	11	D3:5			33	12	D1:5	do not use <sup>2</sup>	---
7	13	D3:4			32	14	D1:4	do not use <sup>2</sup>	---
8	15	D3:3			31	16	D1:3	do not use <sup>2</sup>	---
9	17	D3:2			30	18	D1:2	do not use <sup>2</sup>	---
10	19	D3:1			29	20	D1:1	do not use <sup>2</sup>	---
11	21	D3:0			28	22	D1:0	do not use <sup>2</sup>	---
12	23	D2:7	D23 <sup>1</sup>		27	24	D0:7	do not use <sup>2</sup>	---
13	25	D2:6	D22 <sup>1</sup>		26	26	D0:6	do not use <sup>2</sup>	---
14	27	D2:5	D21 <sup>1</sup>		25	28	D0:5	do not use <sup>2</sup>	---
15	29	D2:4	D20 <sup>1</sup>		24	30	D0:4	do not use <sup>2</sup>	---
16	31	D2:3	D19 <sup>1</sup>		23	32	D0:3	do not use <sup>2</sup>	---
17	33	D2:2	D18 <sup>1</sup>		22	34	D0:2	do not use <sup>2</sup>	---
18	35	D2:1	D17 <sup>1</sup>		21	36	D0:1	do not use <sup>2</sup>	---
19	37	D2:0	D16 <sup>1</sup>		20	38	D0:0	do not use <sup>2</sup>	---

### Mictor Group D

Notes:

- 1) These signals are required for disassembly.
- 2) These TLA inputs must be left unused.

## **APPENDIX B – NEX-563XX P6860 Compression Pinouts**

For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

<b>Pad #</b>	<b>TLA Channel</b>	<b>563XX Signal Name</b>	<b>563XX Pin #</b>
A15	CK1-	Gnd	Gnd
A13	CK1+	AA1~	
B12	A1:7	A15	
B10	A1:6	A14	
A12	A1:5	A13	
A10	A1:4	A12	
B9	A1:3	A11	
B7	A1:2	A10	
A9	A1:1	A9	
A7	A1:0	A8	
B6	A0:7	A7	
B4	A0:6	A6	
A6	A0:5	A5	
A4	A0:4	A4	
B3	A0:3	A3	
B1	A0:2	A2	
A3	A0:1	A1	
A1	A0:0	A0	

**Probe Connection A0/A1**

<b>Pad #</b>	<b>TLA Channel</b>	<b>563XX Signal Name</b>	<b>563XX Pin #</b>
A15	CK0-	Gnd	Gnd
A13	CK0+	AA0~	
B12	A3:7		
B10	A3:6		
A12	A3:5		
A10	A3:4		
B9	A3:3		
B7	A3:2		
A9	A3:1		
A7	A3:0		
B6	A2:7	A23 <sup>2</sup>	
B4	A2:6	A22 <sup>2</sup>	
A6	A2:5	A21 <sup>2</sup>	
A4	A2:4	A20 <sup>2</sup>	
B3	A2:3	A19 <sup>2</sup>	
B1	A2:2	A18 <sup>2</sup>	
A3	A2:1	A17	
A1	A2:0	A16	

**Probe Connection A2/A3**

Notes:

- 1) All signals are required for disassembly.
- 2) These signals are needed for 24-bit address support only.

Pad #	TLA Channel	563XX Signal Name	563XX Pin #
A15	Q1-	Gnd	Gnd
A13	Q1+	AA3~	
B12	C1:7	D15	
B10	C1:6	D14	
A12	C1:5	D13	
A10	C1:4	D12	
B9	C1:3	D11	
B7	C1:2	D10	
A9	C1:1	D9	
A7	C1:0	D8	
B6	C0:7	D7	
B4	C0:6	D6	
A6	C0:5	D5	
A4	C0:4	D4	
B3	C0:3	D3	
B1	C0:2	D2	
A3	C0:1	D1	
A1	C0:0	D0	

**Probe Connection C0/C1**

Pad #	TLA Channel	563XX Signal Name	563XX Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	CLKOUT	
B12	C3:7		
B10	C3:6		
A12	C3:5		
A10	C3:4		
B9	C3:3		
B7	C3:2		
A9	C3:1		
A7	C3:0		
B6	C2:7		
B4	C2:6		
A6	C2:5		
A4	C2:4		
B3	C2:3	BG~	
B1	C2:2	WR~	
A3	C2:1	RD~	
A1	C2:0	RESET~	

**Probe Connection C2/C3**

Notes:

- 1) All signals are required for disassembly.

Pad #	TLA Channel	563XX Signal Name	563XX Pin #
A15	CK2-	Gnd	Gnd
A13	CK2+	CAS~ <sup>1</sup>	---
B12	D1:7	do not use <sup>2</sup>	---
B10	D1:6	do not use <sup>2</sup>	---
A12	D1:5	do not use <sup>2</sup>	---
A10	D1:4	do not use <sup>2</sup>	---
B9	D1:3	do not use <sup>2</sup>	---
B7	D1:2	do not use <sup>2</sup>	---
A9	D1:1	do not use <sup>2</sup>	---
A7	D1:0	do not use <sup>2</sup>	---
B6	D0:7	do not use <sup>2</sup>	---
B4	D0:6	do not use <sup>2</sup>	---
A6	D0:5	do not use <sup>2</sup>	---
A4	D0:4	do not use <sup>2</sup>	---
B3	D0:3	do not use <sup>2</sup>	---
B1	D0:2	do not use <sup>2</sup>	---
A3	D0:1	do not use <sup>2</sup>	---
A1	D0:0	do not use <sup>2</sup>	---

**Probe Connection D0/D1**

Pad #	TLA Channel	563XX Signal Name	563XX Pin #
A15	Q0-	Gnd	Gnd
A13	Q0+	AA2~ <sup>1</sup>	
B12	D3:7		
B10	D3:6		
A12	D3:5		
A10	D3:4		
B9	D3:3		
B7	D3:2		
A9	D3:1		
A7	D3:0		
B6	D2:7	D23 <sup>1</sup>	
B4	D2:6	D22 <sup>1</sup>	
A6	D2:5	D21 <sup>1</sup>	
A4	D2:4	D20 <sup>1</sup>	
B3	D2:3	D19 <sup>1</sup>	
B1	D2:2	D18 <sup>1</sup>	
A3	D2:1	D17 <sup>1</sup>	
A1	D2:0	D16 <sup>1</sup>	

**Probe Connection D2/D3**

Notes:

- 1) These signals are required for disassembly. These TLA inputs must be left unused.

## **APPENDIX C - Necessary Signals for Clocking**

To properly acquire 563XX bus activity in Bus Cycle Clocking mode (see Section 4.0 for further information on this mode), the following signals must be provided: CLKOUT, RD~, WR~, and for any DRAM memory regions, CAS~ and AA0-3~. If Bus Cycle Clocking does not work, move to the Activity Indicator window of the TLA and observe the following:

CLKOUT (CK3) - Should be toggling

RD~ (C2:1) - Should toggle during any Read operations; high otherwise

WR~ (C2:2) - Should toggle during any Write operations; high otherwise

CAS~ (CK2) - Will toggle only during DRAM accesses; high otherwise

AA0~ (CK0)

AA1~ (CK1)

AA2~ (Q0)

AA3~ (Q1) - These signals should toggle during any external memory accesses.

## APPENDIX D – 563XX Family Pinouts

Signal Name	TLA Input	56302	56301	56301	56303	56303	56305	56307	56309	56309	56362
		144 TQFP	208 TQFP	252 PBGA	144 TQFP	196 PBGA	252 PBGA GSM	196 PBGA 100	144 TQFP	196 PBGA	144 TQFP Audio added
		80Mhz max.	66/80/100 MHz		Mem. diff.		Europe	MHz w/	Repl 302		
			w/PCI					co-proc.			
A23			66	M16			M16				
A22			65	M15			M15				
A21			62	M14			M14				
A20			61	N15			N15				
A19			60	M13			M13				
A18			59	P16			P16				
A17	A2:1	99	56	N14	99	E12	N14	E12	99	E12	99
A16	A2:0	98	55	N13	98	E13	N13	E13	98	E13	98
A15	A1:7	97	52	P14	97	F14	P14	F14	97	F14	97
A14	A1:6	94	51	R14	94	F13	R14	F13	94	F13	94
A13	A1:5	93	48	T14	93	G12	T14	G12	93	G12	93
A12	A1:4	92	47	P12	92	G14	P12	G14	92	G14	92
A11	A1:3	89	46	R13	89	H14	R13	H14	89	H14	89
A10	A1:2	88	45	T13	88	H13	T13	H13	88	H13	88
A9	A1:1	85	42	R12	85	J14	R12	J14	85	J14	85
A8	A1:0	84	41	P11	84	J12	P11	J12	84	J12	84
A7	A0:7	83	40	T12	83	J13	T12	J13	83	J13	83
A6	A0:6	82	39	R11	82	K14	R11	K14	82	K14	82
A5	A0:5	79	36	P10	79	K13	P10	K13	79	K13	79
A4	A0:4	78	35	T11	78	L14	T11	L14	78	L14	78
A3	A0:3	77	34	R10	77	L13	R10	L13	77	L13	77
A2	A0:2	76	33	N10	76	M14	N10	M14	76	M14	76
A1	A0:1	73	30	N9	73	M13	N9	M13	73	M13	73
A0	A0:0	72	29	T10	72	N14	T10	N14	72	N14	72
D23	D2:7	133	100	D16	133	A6	D16	A6	133	A6	133
D22	D2:6	132	99	E15	132	C6	E15	C6	132	C6	132
D21	D2:5	131	98	E16	131	B6	E16	B6	131	B6	131
D20	D2:4	128	95	F15	128	B7	F15	B7	128	B7	128
D19	D2:3	125	94	F14	125	A8	F14	A8	125	A8	125
D18	D2:2	124	93	F13	124	C8	F13	C8	124	C8	124
D17	D2:1	123	92	F16	123	B8	F16	B8	123	B8	123
D16	D2:0	122	91	G15	122	A9	G15	A9	122	A9	122
D15	C1:7	121	90	G14	121	B9	G14	B9	121	B9	121
D14	C1:6	118	87	G16	118	A10	G16	A10	118	A10	118
D13	C1:5	117	86	H15	117	B10	H15	B10	117	B10	117
D12	C1:4	116	85	G13	116	C10	G13	C10	116	C10	116
D11	C1:3	115	84	H13	115	A11	H13	A11	115	A11	115
D10	C1:2	114	83	J15	114	B11	J15	B11	114	B11	114
D9	C1:1	113	82	H14	113	A12	H14	A12	113	A12	113
D8	C1:0	110	77	H16	110	B12	H16	B12	110	B12	110
D7	C0:7	109	76	J16	109	A13	J16	A13	109	A13	109
D6	C0:6	108	75	K15	108	C12	K15	C12	108	C12	108
D5	C0:5	107	74	J14	107	B13	J14	B13	107	B13	107
D4	C0:4	106	73	K16	106	C14	K16	C14	106	C14	106
D3	C0:3	105	72	K14	105	C13	K14	C13	105	C13	105
D2	C0:2	102	69	L15	102	D13	L15	D13	102	D13	102
D1	C0:1	101	68	L16	101	D12	L16	D12	101	D12	101
D0	C0:0	100	67	L14	100	E14	L4	E14	100	E14	100

Signal Name	TLA Input	56302 144 TQFP	56301 208 TQFP	56301 252 PBGA	56303 144 TQFP	56303 196 PBGA	56305 252 PBGA	56307 196 PBGA	56309 144 TQFP	56309 196 PBGA	56362 144 TQFP
RESET~	C2:0	44	10	T4	44	N5	T4	N5	44	N5	44
BG~	C2:3	71	16	P7	71	P13	P7	P13	71	P13	71
WR~	C2:2	67	22	T8	67	M11	T8	M11	67	M11	67
RD~	C2:1	68	23	T9	68	M12	T9	M12	68	M12	68
CLKOUT	Clk:3	59	5	P4	59	M9	P4	M9	59	M9	59
CAS~	Clk:2	52	7	R4	52	N8	R4	N8	52	N8	52
AA3_RAS3~	Qual:1	50	21	P8	50	N7	P8	N7	50	N7	50
AA2_RAS2~	Qual:0	51	20	R7	51	P7	R7	P7	51	P7	51
AA1_RAS1~	Clk:1	69	2	R3	69	P12	R3	P12	69	P12	69
AA0_RAS0~	Clk:0	70	1	P3	70	N13	P3	N13	70	N13	70
PCI Bus											
AD31	A3:7		107	B14			B14				
AD30	A3:6		108	A14			A14				
AD29	A3:5		109	B13			B13				
AD28	A3:4		110	D12			D12				
AD27	A3:3		113	A13			A13				
AD26	A3:2		114	C12			C12				
AD25	A3:1		115	B12			B12				
AD24	A3:0		116	A12			A12				
AD23	A2:7		118	A11			A11				
AD22	A2:6		119	B11			B11				
AD21	A2:5		120	C10			C10				
AD20	A2:4		121	A10			A10				
AD19	A2:3		124	B10			B10				
AD18	A2:2		125	C9			C9				
AD17	A2:1		126	A9			A9				
AD16	A2:0		127	A8			A8				
AD15	A1:7		151	A3			A3				
AD14	A1:6		152	B3			B3				
AD13	A1:5		153	C4			C4				
AD12	A1:4		154	C3			C3				
AD11	A1:3		159	C2			C2				
AD10	A1:2		160	D4			D4				
AD9	A1:1		161	D3			D3				
AD8	A1:0		162	C1			C1				
AD7	A0:7		164	D2			D2				
AD6	A0:6		165	E3			E3				
AD5	A0:5		166	D1			D12				
AD4	A0:4		167	E2			E2				
AD3	A0:3		170	F3			F3				
AD2	A0:2		171	E1			E1				
AD1	A0:1		172	F1			F1				
AD0	A0:0		173	F2			F2				
RST~	C3:5		147	B5			B5				
FRAME~	C2:0		130	C8			C8				
DEVSEL~	C3:0		138	B7			B7				
STOP~	C2:3		139	D7			D7				
IRDY~	C2:1		133	A7			A7				
TRDY~	C2:2		134	D8			D8				
C/BE#[3]	C2:7		117	C11			C11				
C/BE#[2]	C2:6		128	B9			B9				
C/BE#[1]	C2:5		150	C5			C5				
C/BE#[0]	C2:4		163	E4			E4				

Signal Name	TLA Input	56302 144 TQFP	56301 208 TQFP	56301 252 PBGA	56303 144 TQFP	56303 196 PBGA	56305 252 PBGA	56307 196 PBGA	56309 144 TQFP	56309 196 PBGA	56362 144 TQFP
INTD#			N/A	N/A			N/A				
INTC#			N/A	N/A			N/A				
INTB#			N/A	N/A			N/A				
INTA#	C0:0		181	H2			H2				
REQ#	C0:5		146	C6			C6				
GNT#	C0:6		149	B4			B4				
LOCK#	C3:4		140	C7			C7				
IDSEL	C0:4		129	B8			B8				
PERR#	C3:3		141	A6			A6				
PAR	C3:2		145	A5			A5				
SERR#	C3:1		142	B6			B6				
CLK	C3:6		148	A4			A4				
CLK	Clock:0		148	A4			A4				
DEVSEL#	Clock:2		138	B7			B7				

## **APPENDIX E - Support**

### **About Nexus Technology, Inc.**



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.  
78 Northeastern Blvd. #2  
Nashua, NH 03062

TEL: 877-595-8116  
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

### **Support Contact Information**

Technical Support	<b><a href="mailto:techsupport@nexustechnology.com">techsupport@nexustechnology.com</a></b>
General Information	<b><a href="mailto:support@nexustechnology.com">support@nexustechnology.com</a></b>
Quote Requests	<b><a href="mailto:quotes@nexustechnology.com">quotes@nexustechnology.com</a></b>

We will try to respond within one business day.

### **If Problems Are Found**

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

## **APPENDIX F - References**

DSP56300 24-Bit Digital Signal Processor Family Manual (PDL Version)  
Motorola, Inc., Semiconductor Products Sector, DSP Division  
William Cannon Drive, West, Austin, Texas, 78735-8598

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual