



# NEX-DDRII400BM

## DDRII 400 Synchronous DRAM Interposer Support

Including these Software Support packages:

DDR2M400

DDRSPA

Copyright © 2008 Nexus Technology, Inc. All rights reserved.

Contents of this publication may not be reproduced in any form without the written permission of Nexus Technology, Inc.

Brand and product names used throughout this manual are the trademarks of their respective holders.

## **Warranty Terms and License Agreement**

For warranty terms, refer to the Terms and Conditions of Sale document that was included in the product shipment. The Software License Agreement is displayed during installation. A hardcopy of that agreement may be obtained from Nexus Technology.

All Nexus Technology products to which this manual refers are subject to the Terms and Conditions of Sale document and the Software License Agreement, as appropriate.

## **Compliance with WEEE and RoHS Directives**

This product is subject to European Union regulations on Waste Electrical and Electronics Equipment. Return to Nexus Technology for recycle at end of life. Costs associated with the return to Nexus Technology are the responsibility of the sender.

## **TABLE OF CONTENTS**

1.0 OVERVIEW .....	5
1.1 General Information.....	5
2.0 SOFTWARE INSTALLATION.....	6
3.0 CONNECTING to the NEX-DDR2M400BM ADAPTER .....	6
3.1 General.....	6
4.0 CLOCK SELECTION .....	11
5.0 CONFIGURING FOR DATA ACQUISITION .....	12
5.1 Adjusting Input Thresholds for Proper Data Acquisition.....	12
5.2 Selecting DDR2M400 Read Sample Points .....	12
5.3 Selecting DDR2M400 Write Sample Points .....	14
5.4 DDR2M400 Support.....	15
6.0 VIEWING DATA.....	21
6.1 Viewing State Data on the TLA - General .....	21
6.2 Viewing DDR2M400 Data .....	22
6.3 DDR2M400 Mnemonics Description.....	26
6.4 Viewing Timing Data on the TLA700.....	27
7.0 HINTS & TIPS .....	28
7.1 Triggering on a Command.....	28
7.2 Capturing MRS (Mode Register Set) Data.....	29
APPENDIX A - How DDR2M400 Data is Clocked.....	31
A.1 Background.....	31
A.2 DDR Acquisition - General .....	31
A.3 DDR2M400 Support.....	32
APPENDIX B - Considerations.....	32
APPENDIX B - Considerations.....	33
B.1 DDR2M400 Bus Loading .....	33
APPENDIX C - DDR2M400 DIMM 240-pin Pinout .....	34
APPENDIX C - DDR2M400 DIMM 240-pin Pinout (cont'd.) .....	36
APPENDIX D- NEX-DDR2M400BM P6860 Compression Pinouts .....	37
APPENDIX D- NEX-DDR2M400BM P6860 Compression Pinouts (cont'd.) .....	38
APPENDIX D- NEX-DDR2M400BM P6860 Compression Pinouts (cont'd.) .....	39
APPENDIX D- NEX-DDR2M400BM P6860 Compression Pinouts (cont'd.) .....	40
APPENDIX D- NEX-DDR2M400BM P6860 Compression Pinouts (cont'd.) .....	41
APPENDIX E - NEX-DDR2M400BM Silkscreen .....	42
APPENDIX F – Data Group / Data Byte / Strobe Cross-Reference .....	43
APPENDIX F – Data Group / Data Byte / Strobe Cross-Reference (cont'd.) .....	44
APPENDIX G - References.....	45
APPENDIX H - Support.....	46

## **TABLE OF FIGURES**

Figure 1- Read Cycle, CAS Latency = 2 cycles .....	13
Figure 2- Read Cycle, CAS Latency = 2.5 cycles .....	13
Figure 3- Write Cycle, Maximum Strobe Delay.....	14
Figure 4- Write Cycle, Minimum Strobe Delay .....	15
Figure 5- Locating Minimum Valid DDRII Read Data Window .....	16
Figure 6- Measuring DDRII Read Data Setup & Hold .....	16
Figure 7- Setting DDR2M400 Read Data Setup & Hold Sample Points .....	17
Figure 8- Locating Minimum Valid DDRII Write Data Window .....	18
Figure 9- Measuring DDRII Write Data Setup & Hold.....	18
Figure 10- Setting DDR2M400 Write Data Setup & Hold Sample Points .....	19
Figure 11- Viewing Individual 8-bit Read Data Groups .....	20
Figure 12- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups.....	20
Figure 13- 400DDR2M State Display- Show All Data? = Yes.....	22
Figure 14- DDR2M400 Disassembly Properties .....	23
Figure 15- DDR2M400 State Display- Show All Data? = No .....	24
Figure 16- DDR2M400 State Display- Show Control Flow .....	25
Figure 17- DDR2M400 MagniVu Display on TLA .....	27
Figure 18- Recommended DDR2M400 Command Trigger .....	28
Figure 19- Recommended DDR2M400 Command Trigger - Detail .....	29
Figure 20- DDR2M400 MRS Trigger .....	30
Figure 21- MRS Cycle Acquisition Disassembly.....	30

## **TABLE OF TABLES**

Table 1- DDR2M400 TLA700 Channel Grouping.....	7
Table 2- DDR2M400 Command Symbol Table.....	21
Table 3- DDR2M400 Mnemonics Definition.....	26

## **1.0 OVERVIEW**

### **1.1 General Information**

The NEX-DDRII400BM adapter has been designed to provide a quick and easy connection to interface a Tektronix TLA700 Logic Analyzer to a 240-pin 2.5volt 64/72-bit wide DDRII (Double Data Rate II) Synchronous DRAM Dual In-Line Memory Module (DDRII SDRAM DIMM) socket. Analyzer connections are made through P6860 High-Density Connectorless probes to help minimize the size of the adapter board, thus reducing trace length and keeping signal loading to a minimum. The NEX-DDRII400BM is a “Mirror” image adapter, in that it facilitates both Logic Analyzer connection and DIMM socket on the back side. The NEX-DDRII400BM adapter is used in places where the standard adapter with the Logic Analyzer connections and DIMM socket placed on the front of the adapter will not fit in to the system under test.

The NEX-DDRII400BM support requires two merged TLA7Ax4 136-channel acquisition cards for 400MT/s support. For this support to work, both cards must have the 450MHz state clocking option (refer to Section 5.0 for further information). The NEX-DDRII400BM support is usable with a TLA7XX-series Logic Analyzer only, and the TLA must be running V4.2 or later of the TLA Application Software. The NEX-DDRII400BM software also post-processes the acquisition to display valid cycle information to the user.

The NEX- DDRII400BM software disk includes to supports listed below:

**MDDR2** allows the user to acquire both Read AND Write DDRII data from a target. This support requires 8-P6860 High-Density Compression probes.

Note that this manual uses some terms generically. For instance, references to the TLA700 apply to all suitable TLA700 Logic Analyzers.

Appendix E has a silk-screened print of the NEX-DDRII400BM adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the DDR-II SDRAM Specification and the Tektronix TLA700 Logic Analyzers. It is also expected that the user is familiar with the Windows environment used on the TLA.

## **2.0 SOFTWARE INSTALLATION**

The NEX-DDR2M400 software is installed using the same method as other Windows programs. Place the DDR2M400 Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer module in the Setup window, select Load Support Package from the File pull-down, then choose DDR2M400 and click on **Okay**. Note that the support requires two merged modules and that the TLA acquisition cards must be configured properly for the software to load.

## **3.0 CONNECTING to the NEX-DDR2M400 ADAPTER**

### **3.1 General**

Care should be taken to support the weight of the acquisition probes so that the adapter board and/or target socket are not damaged

The NEX-DDR2M400 adapter is larger than a standard DDR DIMM module and is designed to function as an extender card, providing an easy connection to the logic analyzer for DDR data acquisition. Because of this design approach it is entirely possible that placing a target card onto the NEX-DDR2M400 adapter may result in improper operation of the target card or system.

Care should be used when removing a DIMM under test from the Adapter. The extraction tabs will break if excessive force is used.

The DDR2M400 support requires two merged TLA7Ax4 acquisition cards. The Master card is the card in the lower-numbered slots; the Slave card is the card in the higher-numbered slots. When using the DDR2M400 support the acquisition cards must be connected to the NEX-DDR2M400 adapter as follows using eight (8) P6860 probes:

TLA Master P6860 A2/A3 probe head to DDR2 MA-A2/A3 position  
TLA Master P6860 A0/A1 probe head to DDR2 MA-A0/A1 position  
TLA Master P6860 D0/D1 probe head to DDR2 MA-D0/D1 position  
TLA Master P6860 C2/C3 probe head to DDR2 MA-C2/C3 position  
TLA Master P6860 C0/C1 probe head to DDR2 MA-C0/C1 position  
TLA Master P6860 E2/E3 probe head to DDR2 MA-E2/E3 position  
TLA Slave P6860 A2/A3 probe head to DDR2 SL-A2/A3 position  
TLA Slave P6860 A0/A1 probe head to DDR2 SL-A0/A1 position  
TLA Slave P6860 C2/C3 probe head to DDR2 SL-C2/C3 position  
TLA Slave P6860 E2/E3 probe head to DDR2 SL-E2/E3 position

Table 1 shows the Channel Grouping / Wiring for use with the DDR2M400 support.

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RDDatHi (Hex)	RD_DQ63	236	SL_E2:1	RDDatLo (Hex)	RD_DQ31	159	SL_A1:5
	RD_DQ62	235	SL_E2:3		RD_DQ30	158	SL_A1:7
	RD_DQ61	230	SL_E2:5		RD_DQ29	153	SL_C2:1
	RD_DQ60	229	SL_E2:7		RD_DQ28	152	SL_C2:3
	RD_DQ59	117	SL_E2:0		RD_DQ27	40	SL_A1:4
	RD_DQ58	116	SL_E2:2		RD_DQ26	39	SL_A1:6
	RD_DQ57	111	SL_E2:4		RD_DQ25	34	SL_C2:0
	RD_DQ56	110	SL_E2:6		RD_DQ24	33	SL_C2:2
	RD_DQ55	227	SL_E3:1		RD_DQ23	150	SL_C2:5
	RD_DQ54	226	SL_E3:3		RD_DQ22	149	SL_C2:7
	RD_DQ53	218	SL_E3:5		RD_DQ21	144	SL_C3:1
	RD_DQ52	217	SL_E3:7		RD_DQ20	143	SL_C3:3
	RD_DQ51	108	SL_E3:0		RD_DQ19	31	SL_C2:4
	RD_DQ50	107	SL_E3:2		RD_DQ18	30	SL_C2:6
	RD_DQ49	99	SL_E3:4		RD_DQ17	25	SL_C3:0
	RD_DQ48	98	SL_E3:6		RD_DQ16	24	SL_C3:2
	RD_DQ47	215	SL_A2:1		RD_DQ15	141	SL_C3:5
	RD_DQ46	214	SL_A2:3		RD_DQ14	140	SL_C3:7
	RD_DQ45	209	SL_A2:5		RD_DQ13	132	MA_E2:5
	RD_DQ44	208	SL_A2:7		RD_DQ12	131	MA_E2:7
	RD_DQ43	96	SL_A2:0		RD_DQ11	22	SL_C3:4
	RD_DQ42	95	SL_A2:2		RD_DQ10	21	SL_C3:6
	RD_DQ41	90	SL_A2:4		RD_DQ9	13	MA_E2:4
	RD_DQ40	89	SL_A2:6		RD_DQ8	12	MA_E2:6
	RD_DQ39	206	SL_A3:1		RD_DQ7	129	MA_E3:1
	RD_DQ38	205	SL_A3:3		RD_DQ6	128	MA_E3:3
	RD_DQ37	200	SL_A3:5		RD_DQ5	123	MA_E3:5
	RD_DQ36	199	SL_A3:7		RD_DQ4	122	MA_E3:7
	RD_DQ35	87	SL_A3:0		RD_DQ3	10	MA_E3:0
	RD_DQ34	86	SL_A3:2		RD_DQ2	9	MA_E3:2
	RD_DQ33	81	SL_A3:4		RD_DQ1	4	MA_E3:4
	RD_DQ32	80	SL_A3:6		RD_DQ0	3	MA_E3:6

**Table 1- DDR2M400 TLA700 Channel Grouping**

Notes:

1. The 'SL' in front of a TLA channel denotes the Slave card of the merged pair
2. The 'MA' in front of a TLA channel denotes the Master card of the merged pair
3. All signals are required for accurate post-processing of acquired data

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
WRDatHi (Hex)	WR_DQ63	236	SL_E0:1	WRDatLo (Hex)	WR_DQ31	159	SL_D1:5
	WR_DQ62	235	SL_E0:3		WR_DQ30	158	SL_D1:7
	WR_DQ61	230	SL_E0:5		WR_DQ29	153	SL_C2:1
	WR_DQ60	229	SL_E0:7		WR_DQ28	152	SL_C2:3
	WR_DQ59	117	SL_E0:0		WR_DQ27	40	SL_D1:4
	WR_DQ58	116	SL_E0:2		WR_DQ26	39	SL_D1:6
	WR_DQ57	111	SL_E0:4		WR_DQ25	34	SL_C0:0
	WR_DQ56	110	SL_E0:6		WR_DQ24	33	SL_C0:2
	WR_DQ55	227	SL_E1:1		WR_DQ23	150	SL_C0:5
	WR_DQ54	226	SL_E1:3		WR_DQ22	149	SL_C0:7
	WR_DQ53	218	SL_E1:5		WR_DQ21	144	SL_C1:1
	WR_DQ52	217	SL_E1:7		WR_DQ20	143	SL_C1:3
	WR_DQ51	108	SL_E1:0		WR_DQ19	31	SL_C0:4
	WR_DQ50	107	SL_E1:2		WR_DQ18	30	SL_C0:6
	WR_DQ49	99	SL_E1:4		WR_DQ17	25	SL_C1:0
	WR_DQ48	98	SL_E1:6		WR_DQ16	24	SL_C1:2
	WR_DQ47	215	SL_D2:1		WR_DQ15	141	SL_C1:5
	WR_DQ46	214	SL_D2:3		WR_DQ14	140	SL_C1:7
	WR_DQ45	209	SL_D2:5		WR_DQ13	132	MA_E0:5
	WR_DQ44	208	SL_D2:7		WR_DQ12	131	MA_E0:7
	WR_DQ43	96	SL_D2:0		WR_DQ11	22	SL_C1:4
	WR_DQ42	95	SL_D2:2		WR_DQ10	21	SL_C1:6
	WR_DQ41	90	SL_D2:4		WR_DQ9	13	MA_E0:4
	WR_DQ40	89	SL_D2:6		WR_DQ8	12	MA_E0:6
	WR_DQ39	206	SL_D3:1		WR_DQ7	129	MA_E1:1
	WR_DQ38	205	SL_D3:3		WR_DQ6	128	MA_E1:3
	WR_DQ37	200	SL_D3:5		WR_DQ5	123	MA_E1:5
	WR_DQ36	199	SL_D3:7		WR_DQ4	122	MA_E1:7
	WR_DQ35	87	SL_D3:0		WR_DQ3	10	MA_E1:0
	WR_DQ34	86	SL_D3:2		WR_DQ2	9	MA_E1:2
	WR_DQ33	81	SL_D3:4		WR_DQ1	4	MA_E1:4
	WR_DQ32	80	SL_D3:6		WR_DQ0	3	MA_E1:6

**Table 1 – DDR2M400 TLA700 Channel Grouping (cont'd.)**

Notes:

1. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
2. All signals are required for accurate post-processing of acquired data
3. All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR II Pin #	TLA700 Input	Group Name	Signal Name	DDR II Pin #	TLA700 Input
Address (Hex)	BA1	190	MA_D0:3	Command (Sym)	* S1#	76	MA_Ck3+
	BA0	71	MA_D0:2		* S0#	193	MA_C2:2
	A16/BA2	54	MA_C0:4		* RAS#	192	MA_C2:0
	A15	173	MA_C0:5		* CAS#	74	MA_C2:3
	A14	174	MA_C0:3		* WE#	73	MA_C2:1
	A13	196	MA_C2:5	Strobes (Hex)	DQS7	114	MA_A3:0
	A12	176	MA_C0:1		DQS6	105	MA_A3:4
	A11	57	MA_C0:0		DQS5	93	MA_C3:5
	A10	70	MA_D0:4		DQS4	84	MA_C3:1
	A9	177	MA_D1:7		DQS3	37	MA_C1:4
	A8	179	MA_D1:5		DQS2	28	MA_A1:6
	A7	58	MA_D1:6	DQS1	16	MA_A0:7	
	A6	180	MA_D1:3	DQS0	7	MA_A0:3	
	A5	60	MA_D1:4	WrtMasks	DM7_DQS16	232	MA_A3:3
	A4	61	MA_D1:2		DM6_DQS15	223	MA_A3:7
	A3	182	MA_D1:1		DM5_DQS14	211	MA_C3:2
	A2	63	MA_D1:0		DM4_DQS13	202	MA_C2:6
A1	183	MA_D0:7	DM3_DQS12		155	MA_C1:7	
A0	188	MA_D0:5	DM2_DQS11		146	MA_A1:7	
RDChkBits	NC_DQS8	46	MA_C1:0	DM2_DQS10	134	MA_A0:4	
	RD_NC_CB7	168	SL_A0:5	DM0_DQS9	125	MA_A0:0	
	RD_NC_CB6	167	SL_A0:7	Hi_Strobes	NC_DM8_DQS17	164	MA_C1:3
	RD_NC_CB5	162	SL_A1:1		DM7_DQS16	232	MA_A3:3
	RD_NC_CB4	161	SL_A1:3		DM6_DQS15	223	MA_A3:7
	RD_NC_CB3	49	SL_A0:4		DM5_DQS14	211	MA_C3:2
	RD_NC_CB2	48	SL_A0:6		DM4_DQS13	202	MA_C2:6
	RD_NC_CB1	43	SL_A1:0		DM3_DQS12	155	MA_C1:7
	RD_NC_CB0	42	SL_A1:2		DM2_DQS11	146	MA_A1:7
					DM2_DQS10	134	MA_A0:4
			DM0_DQS9		125	MA_A0:0	
WRChkBits <sup>4</sup>	NC_DQS8	46	MA_C1:0	Misc	* DDRCK2 +/-	220/221	MA_CK0+-
	WR_NC_CB7	168	SL_D0:5		* DDRCK1 +/-	137/138	MA_CK1+-
	WR_NC_CB6	167	SL_D0:7		* DDRCK0 +/-	185/186	MA_CK2+-
	WR_NC_CB5	162	SL_D1:1				
	WR_NC_CB4	161	SL_D1:3				
	WR_NC_CB3	49	SL_D0:4				
	WR_NC_CB2	48	SL_D0:6				
	WR_NC_CB1	43	SL_D1:0				
	WR_NC_CB0	42	SL_D1:2				

Table 1 – DDR2M400 TLA700 Channel Grouping (cont'd.)

Notes:

1. ‘ # ‘ denotes a low-true signal
2. The ‘SL’ in front of a TLA channel denotes the Slave card of the merged pair

3. Signal names preceded by an asterisk ( \* ) are required for accurate acquisition and post-processing of acquired data
4. Signals in this group are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input	
Ungrouped	NC_DQS17 #	165	MA_C1:1		NC_DQS8#	45	MA_C1:2	
	NC_DQS16 #	233	MA_A3:1		DQS7#	113	MA_A3:2	
	NC_DQS15 #	224	MA_A3:5		DQS6 #	104	MA_A3:6	
	NC_DQS14 #	212	MA_C3:4		DQS5 #	92	MA_C3:3	
	NC_DQS13 #	203	MA_C3:0		DQS4 #	83	MA_C2:7	
	NC_DQS12 #	156	MA_C1:5		DQS3 #	36	MA_C1:6	
	NC_DQS11 #	147	MA_A1:5		DQS2 #	27	MA_A1:4	
	NC_DQS10 #	135	MA_A0:6		DQS1 #	15	MA_A0:5	
	NC_DQS9 #	126	MA_A0:2		DQS0 #	6	MA_A0:1	
	CKE1	171	MA_C0:7		SA2	101	MA_C3:6	
	CKE0	52	MA_C0:6		SA1	240	MA_A2:4	
	ODT1	77	MA_D0:1		SA0	239	MA_A2:6	
	ODT0	195	MA_C2:4		NC_TEST	102	MA_C3:7	
	RC1_RESET	18	MA_A1:0		NC_68	68	MA_D0:6	
	#							
	SCL	120	MA_A2:5		NC_19	19	MA_A1:0	
	SDA	119	MA_A2:7		RC0	55	MA_C0:2	

**Table 1 – DDR2M400 TLA700 Channel Grouping (cont'd.)**

Notes:

1. ' # ' denotes a low-true signal
2. The 'SL' in front of a TLA channel denotes the Slave card of the merged pair

## **4.0 CLOCK SELECTION**

There are three clocking option fields available when using the DDR2M400 support package. These select fields permit the user to setup the TLA acquisition as follows:

**SDRAM Clocking:** – Permits selecting the DDR Clock to be used to acquire data. Also allows user to use only Chip Select S0~ or Chip Selects S0~ and S1~ for acquisition. The field choices are:

DDR CK0; S0~ only active (default)  
DDR CK0; S0~ & S1~ active  
DDR CK1; S0~ only active  
DDR CK1 S0~ & S1~ active  
DDR CK2 S0~ only active  
DDR CK2 S0~ & S1~ active

**Clock Mode** – Allows the user to choose the kind of data acquisition that will be made:

**Selective Clocking** (default) – This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS~ or CAS~ is asserted low along with S0~ or S1~. After every assertion of CAS~ (with either S0~ or S1~) a sample is taken on each edge of the next 13 DDR CLK cycles for a total of 26 samples. If CAS~ and a Chip Select are asserted during these 13 cycles the count is reset.

**Every SDRAM Clock Edge** – As the name implies this will cause the acquisition card to store data on every Rising and Falling edge of the selected SDRAM clock.

**Refresh Cycles:** – Permits choosing whether Refresh Cycles will be stored or not. The field choices are:

**Do Not Acquire** (default) – This mode will reduce the number of Refresh cycles stored by the acquisition card to provide optimum use of the acquisition memory.

**Acquire** – Refresh Cycles will be stored.

## **5.0 CONFIGURING FOR DATA ACQUISITION**

### ***IMPORTANT !***

Prior to configuring your NEX-DDRII400BM support package it is *strongly* recommended that Appendix A (“How DDR Data is Clocked”), section 5.2 (“Selecting DDR Read Sample Points”) and section 5.3 (“Selecting DDR Write Sample Points”) be read. This background information is very helpful in properly configuring the support.

#### **5.1 Adjusting Input Thresholds for Proper Data Acquisition**

The voltage threshold must be properly set on the TLA for proper acquisition of the DDR bus. We recommend that you verify the center point of the SDRAM CK0, any DDR strobe, and any DDR data bit. The CLK threshold should be set close to 0v because the clock is a differential signal. The threshold setting can be verified that it is correct by taking a TLA acquisition and verifying a 50% duty cycle on the clock by looking at the DDRCK2, DDRCK1 or DDRCK0 MagniVu trace. All other signals should be set close to center of the voltage swing. Please note that synchronous acquisition using a TLA7AAx or TLA7ABx card requires a valid data window of approximately 625ps.

Although you should measure and set the thresholds as described, you can start with a 1.1V threshold value for all signals except for TLA CK3 (DDRCK0), CK1 (DDRCLK2), and CK0 (DDRCK1), which should be set to 0.07V because they are differential signals. These values can be used as a starting point.

#### **5.2 Selecting DDRII Read Sample Points**

For the DDRII400BM post-processing software to accurately show valid data it is necessary to choose the proper sample points to ensure that valid data is acquired when the software expects it. Since valid DDR Read data is straddled by the Strobes (see Figures 1 and 2), and the Strobes are phase-aligned with the DDR clock for Reads, the Setup & Hold sample point must be set for the valid data that occurs after the clock edge. The correct clock edge is determined by adding the CAS Latency to the Additive Latency which equals the number of clock cycles that Read data will be delayed from the Read command.

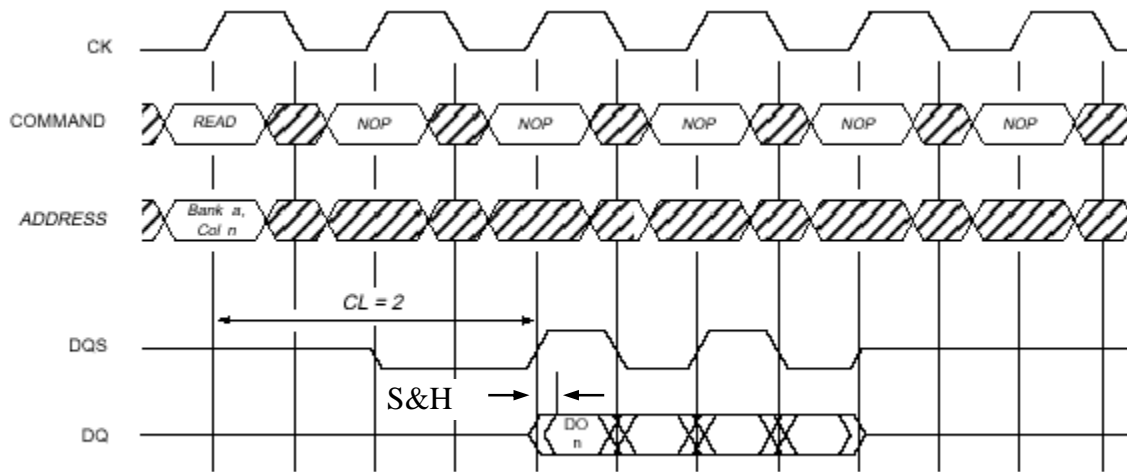


Figure 1- Read Cycle, CAS Latency = 2 cycles

For DDRII400BM support data is acquired on both rising and falling clock edges so only one sample point (illustrated by *S&H Sample Point 1* in Figures 1 and 2) need be set.

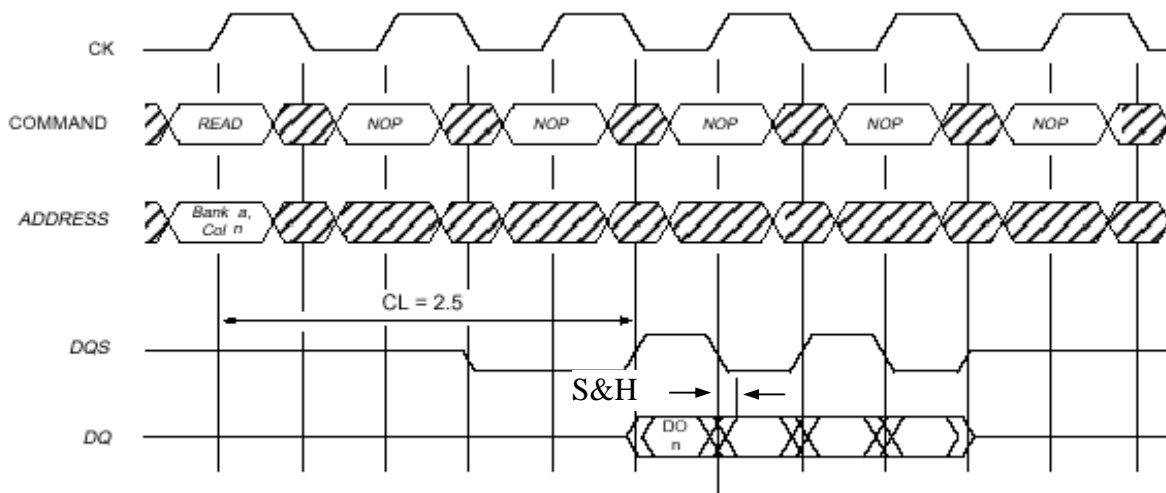


Figure 2- Read Cycle, CAS Latency = 2.5 cycles

### 5.3 Selecting DDRII Write Sample Points

Unlike valid DDR Read data, valid Write data is bisected by the Strobes. This is complicated by the delay from the Write command to the first Strobe rising edge varying anywhere from 75% to 125% of a clock cycle. These two extremes are illustrated in Figures 3 and 4.

IMPORTANT!

For valid Write data to be acquired and stored at the proper point for the DDRII400BM software to interpret it, the Setup & Hold sample points *must* be determined relative to the appropriate rising clock edge after the Write command. The correct rising edge is determined by adding the CAS Latency and the Additive Latency and then subtracting one from their sum. If the Strobes transition from zeroes to ones before the clock edge then positive Setup and negative Hold values will be entered. If the Strobe transition after the edge then negative Setup and positive Hold values will be correct.

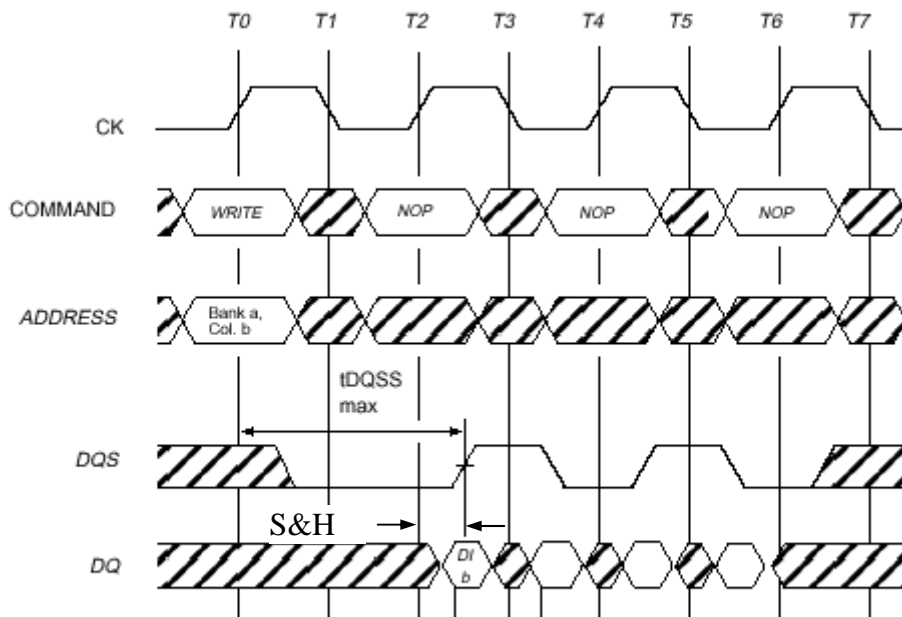
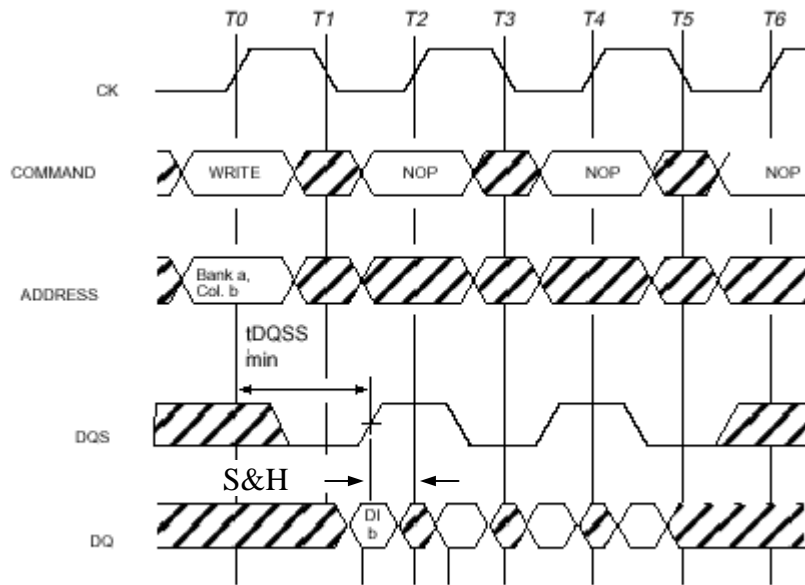


Figure 3- Write Cycle, Maximum Strobe Delay

For DDRII400BM support data is acquired on the rising and falling clock edges so only one sample point (illustrated by *S&H Sample Point 1* in Figures 3 and 4 need be set. It is recommended that the Write Data sample points be set at or near the transition points of the Strobes. The sample point for the WrMasks group should also be set to the transition point of the Strobes (DQS signals) for proper acquisition, again as shown by *S&H Sample Point 1*.



**Figure 4- Write Cycle, Minimum Strobe Delay**

## 5.4 DDR2M400 Support

To adjust the Read Data group sample points first make an appropriate acquisition of Read data by triggering on a Read Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2). A sample waveform display of MagniVu Read data is shown in Figure 5. To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (note arrows in Figure 5).

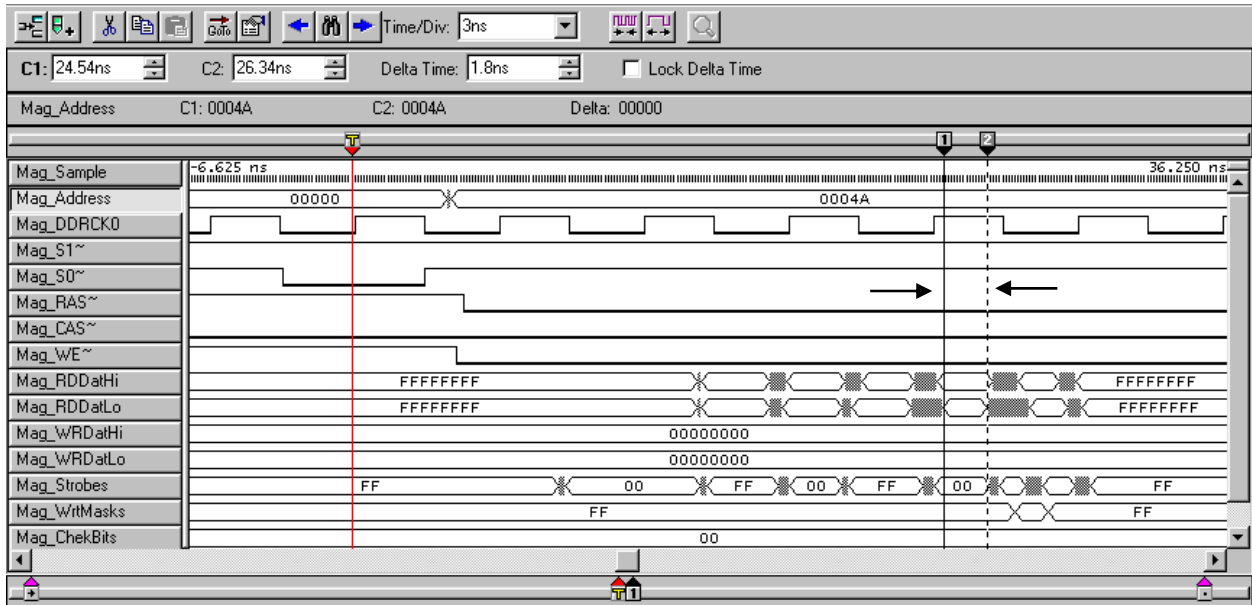


Figure 5- Locating Minimum Valid DDRII Read Data Window

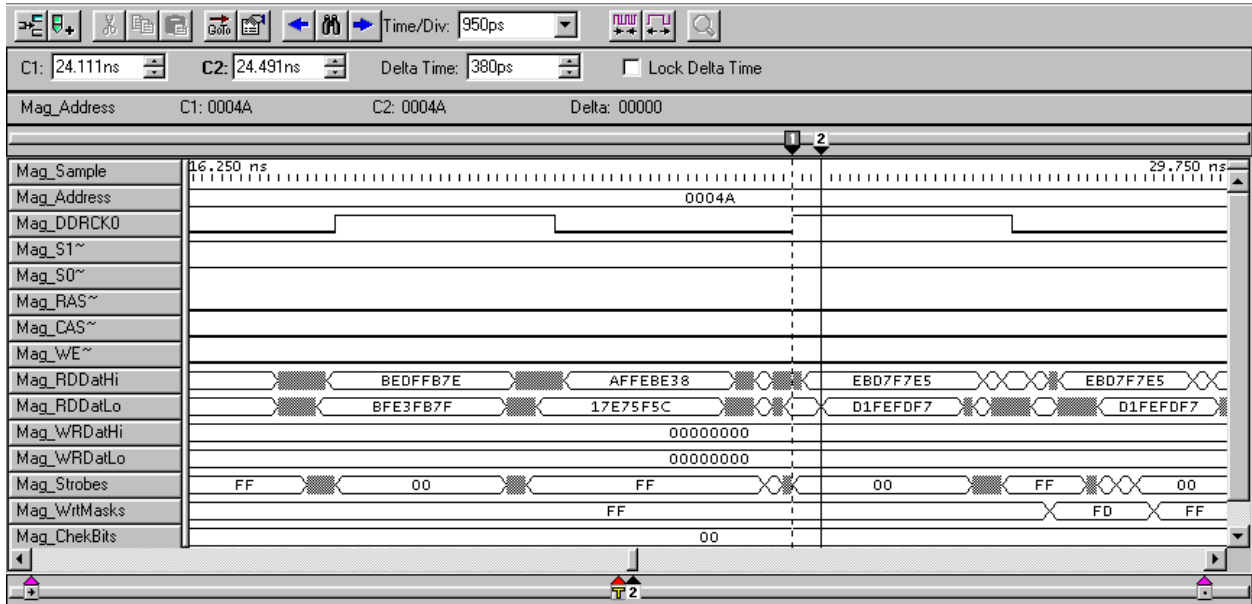
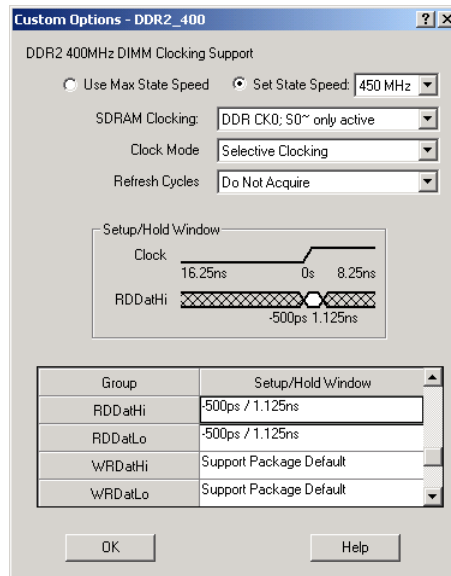


Figure 6- Measuring DDRII Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 6) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is ~380ps, meaning that a suitable Setup & Hold value would be -500ps/1.125ns. This sample point position must now be set for the RDDatHi and RDDatLo groups in the Setup window. This window is found by going to the LA Card's Setup window, then clicking on the **More** button to the right of the clock select field. The TLA acquisition cards require a valid data window of 625ps, and this window can be placed to begin from 16.25ns prior to the clock edge to 7.625ns after the edge in 125ps increments. Each 32-bit data group (RDDatHi and RDDatLo) will require its own value programmed from the measurements noted in the MagniVu window (Figure 7).



**Figure 7- Setting DDR2M400 Read Data Setup & Hold Sample Points**

Setting the Setup & Hold values for acquiring Write data is similar, but the valid data point now more closely aligns with the Strobe edges. To adjust the Write Data group sample points first make an appropriate acquisition of Write data by triggering on a Write Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2).

**Note:** Because of the method used to acquire Write Data using the DDR2M400 support, the Read Data group information must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A “How DDR Data is Clocked”.

A sample waveform display of MagniVu Write data is shown in Figure 8. To determine the sample point, locate the worst-case Setup & Hold timing of valid Write data during the acquired burst (note arrows in Figure 8). Refer to section 5.3 for important information on properly determining the Write data sample points.

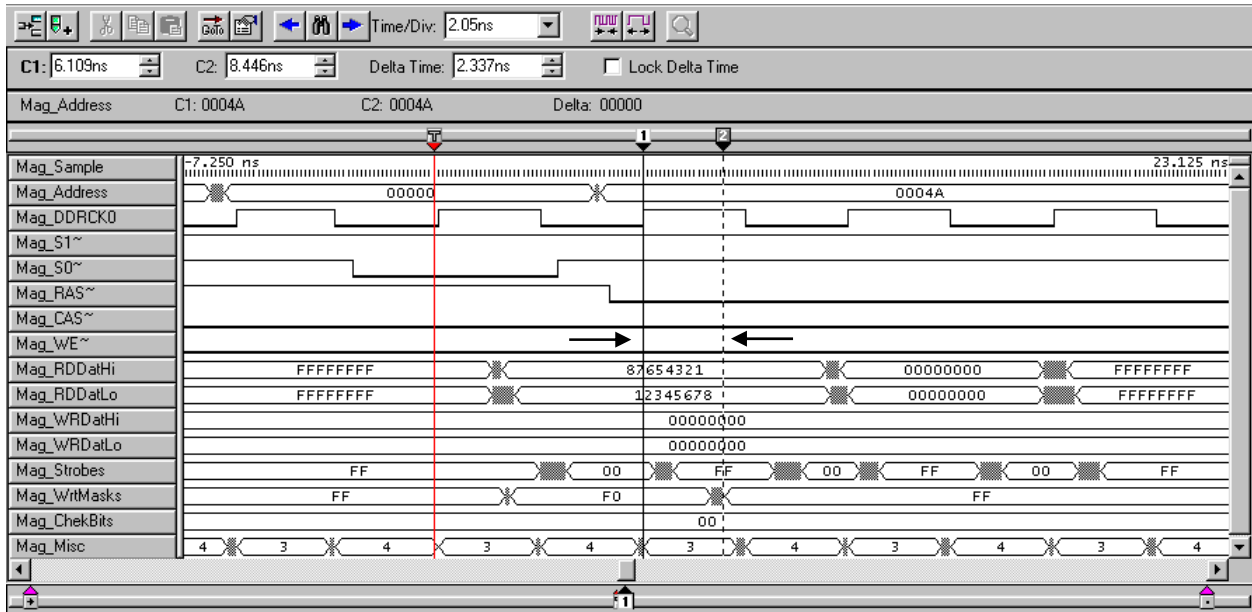


Figure 8- Locating Minimum Valid DDRII Write Data Window

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 9) and use the cursors to measure the time from the clock edge to the start of valid Write data. In this example the delay from edge to Strobe transition is  $\sim 875$ ps, meaning that a suitable Setup & Hold value would be  $-875$ ps/1.5ns. This sample point position must now be set for the WRDatHi and WRDatLo groups in the Setup window (Figure 10). Note that the WrtMasks group should have a Setup & Hold value that aligns with the transition of the Strobes.

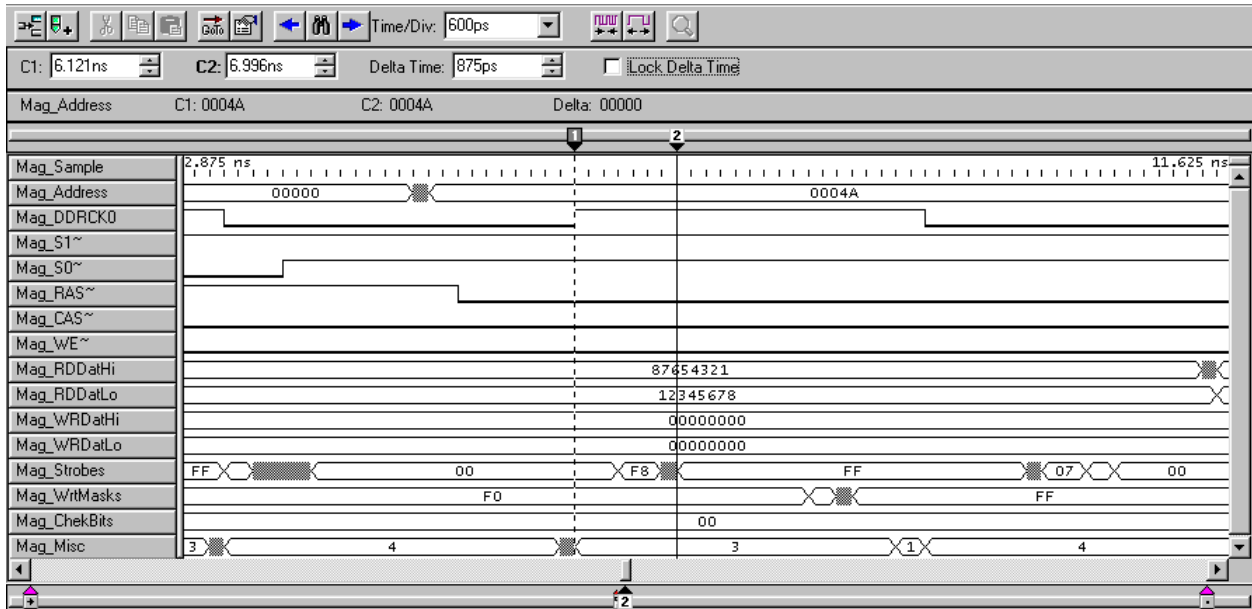
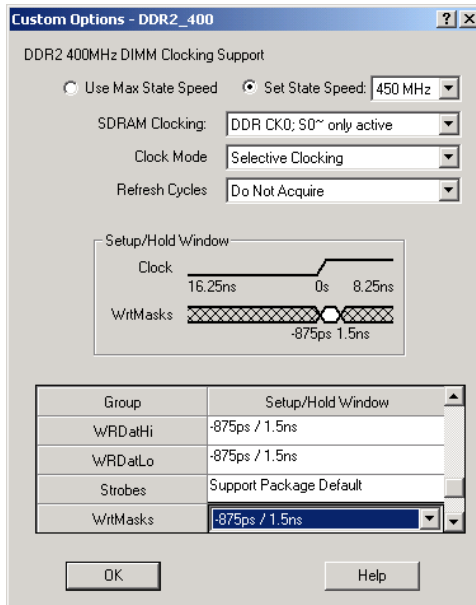


Figure 9- Measuring DDRII Write Data Setup & Hold



**Figure 10- Setting DDR2M400 Write Data Setup & Hold Sample Points**

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 11 shows these added data groups (DatByte7-0) added to the same Waveform display shown in Figure 8. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see Figure 12). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit or 4-bit groups make up a 32-bit group.

**Note:** Again, it is very important to remember that, because of the method used to acquire Write Data using the DDR2M400 support, the Read Data group information must be used to determine the Write Data sample points. For further explanation of this process refer to Appendix A “How DDR Data is Clocked”.

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (RDDatHi, RDDatLo, WRDatHi or WRDatLo) be reset to “Support Package Default”. This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values – 625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

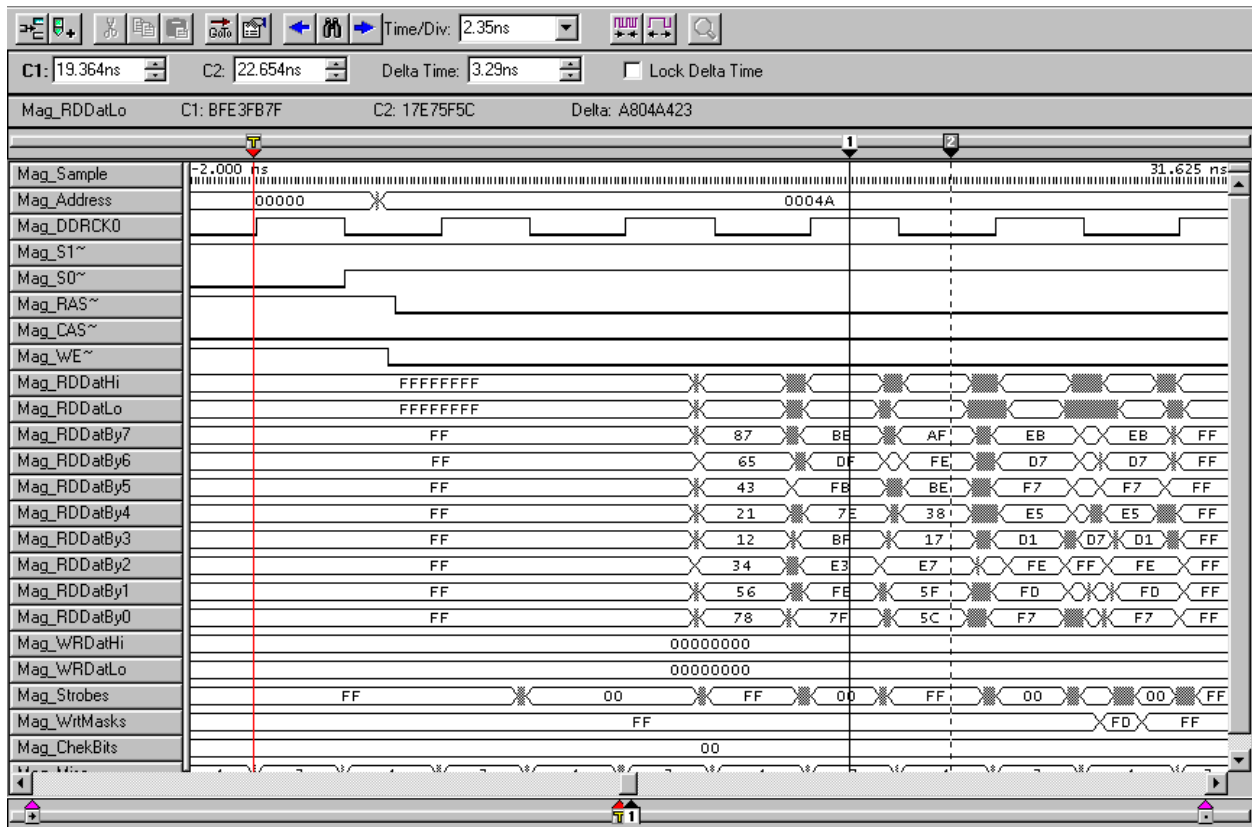


Figure 11- Viewing Individual 8-bit Read Data Groups

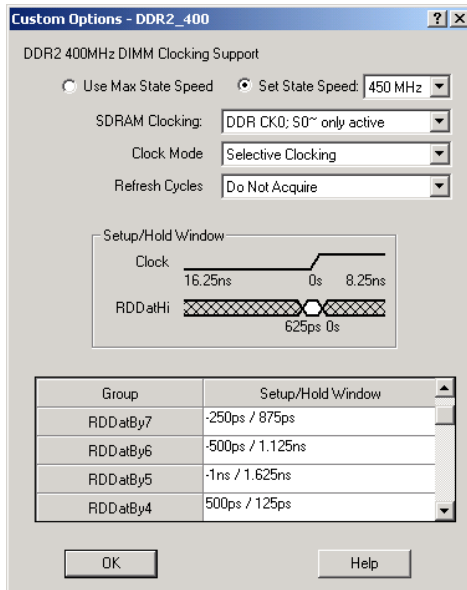


Figure 12- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

Note: Values shown are for illustration purposes only

## **6.0 VIEWING DATA**

### **6.1 Viewing State Data on the TLA - General**

After making an initial acquisition, the TLA will display the data in the Listing (State) format. A Symbol Table has been included in the support package for the Command data group (see Table 2). The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. The symbol file has been created to permit quickly showing the type of transaction that occurred on the DDR Bus - a Read, Write, Precharge, etc. This symbol information can also be used to trigger on a DDR cycle of interest.

It is important to note that changing the group, channel, or wiring of the Command group can result in incorrect symbol information being displayed.

Symbol	Definition
DESL--IGNORE_COMMAND--DATA?	11 xxx
NOP--NO_OPERATION_(S0~)	x0 111
NOP--NO_OPERATION_(S1~)	0x 111
BST--BURST_STOP_(S0~)	x0 110
BST--BURST_STOP_(S1~)	0x 110
READ--COL_ADDR_READ_(S0~)	x0 101
READ--COL_ADDR_READ_(S1~)	0x 101
WRITE--COL_ADDR_WRITE_(S0~)	x0 100
WRITE--COL_ADDR_WRITE_(S1~)	0x 100
ACTV--	x0 011
ROW_ADDRESS_STROBE_(S0~)	
ACTV--	0x 011
ROW_ADDRESS_STROBE_(S1~)	
PRE--	x0 010
PRECHARGE_SELECT_BANK_(S0~)	
PRE--	0x 010
PRECHARGE_SELECT_BANK_(S1~)	
PALL--	x0 010
PRECHARGE_ALL_BANK_(S0~)	
PALL--	0x 010
PRECHARGE_ALL_BANK_(S1~)	
REF--REFRESH_(S0~)	x0 001
REF--REFRESH_(S1~)	0x 001
MRS--MODE_REGISTER_SET_(S0~)	x0 000
MRS--MODE_REGISTER_SET_(S1~)	0x 000

**Table 2- DDR2M400 Command Symbol Table**

Signals, left-to-right: S1~, S0~, RAS~, CAS~, WE~

## 6.2 Viewing DDR2M400 Data

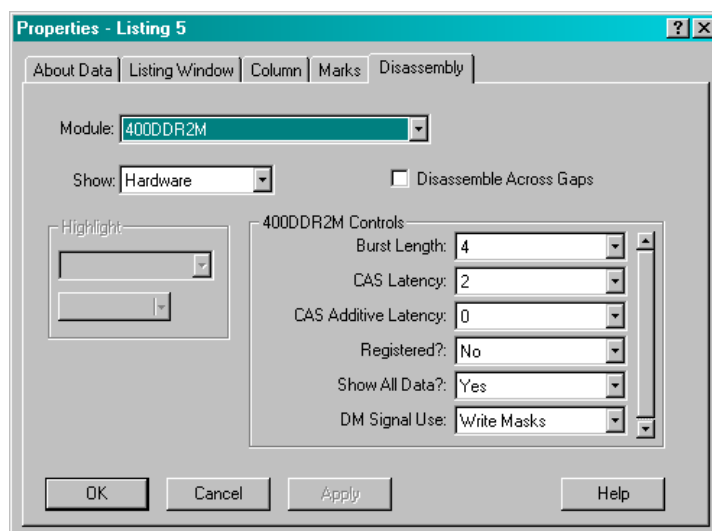
The DDR2M400 support package displays the Address, RDDatHi, RDDatLo, WRDatHi, WRDatLo, WrtMsk, and Strobes group data in hexadecimal format; Command, ChekBits, Misc, and the Data Byte (RDDatByx and WRDatByx) or Data Nibble (RDDatNibx and WRDatNibx) groups default to OFF.

The Command group is suppressed because its function is replaced with a column labeled “DDR2M400 Mnemonics”. The DDR2M400 support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 13 shows the default display where all DDR data is displayed.

Sample	DDRHS-RW Address	DDRHS-RW RDDatHi	DDRHS-RW RDDatLo	DDRHS-RW WRDatHi	DDRHS-RW WRDatLo	DDRHS-RW Mnemonics	DDRHS-RW Strobes	DDRHS-RW WrtMasks	Command	Timestamp
2015	003C8	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11100	2.875 ns
2016	003C8	FFFFFFE6	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11100	3.000 ns
2017	003C8	644F646E	65706544	6E4F646E	65706544	DESL - IGNORE COMMAND	FF	00	11100	3.000 ns
2018	0044A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	38.875 ns
2019	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	REF - REFRESH (S0~)	FF	FF	10001	17.875 ns
2020	00000	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	ACTV - ROW ADDRESS STROBE (S0~)	FF	FF	10011	395.000 ns
2021	003D0	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	READ - COL ADDR READ (S0~)	FF	FF	10101	18.000 ns
2022	003D0	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	(UNKNOWN)	FF	FF	10101	2.875 ns
2023	003D4	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11101	3.125 ns
2024	003D4	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11101	2.875 ns
2025	003D4	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	READ - COL ADDR READ (S0~)	00	FF	10101	3.125 ns
2026	003D4	00000000	00000000	FFFFFFFF	FFFFFFFF	READ DATA	00	FF	10101	2.875 ns
2027	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	F9	11010	3.000 ns
2028	0004A	00000000	00000000	00000000	00000000	READ DATA	00	FF	11010	3.000 ns
2029	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	FF	11010	3.000 ns
2030	0004A	00000000	00000000	00000000	00000000	READ DATA	00	FF	11010	3.000 ns
2031	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	FF	11010	3.000 ns
2032	0004A	00000000	00000000	00000000	00000000	READ DATA	00	FF	11010	3.000 ns
2033	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	FF	11010	3.000 ns
2034	0004A	FFFFFFFF	7E33FFF	FFFFFFFF	00000000	DESL - IGNORE COMMAND	00	FF	11010	3.000 ns
2035	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	08128C08	DESL - IGNORE COMMAND	02	FF	11010	3.000 ns
2036	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2037	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2038	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	2.875 ns
2039	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2040	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3.125 ns
2041	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	2.875 ns
2042	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2043	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	4.590,000 us
2044	0044A	00000000	00000000	00000000	00000000	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	731.625 ns
2045	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	3EC7DFF	REF - REFRESH (S0~)	FF	FF	10001	17.875 ns
2046	00000	FFFFFFFF	FFFFFFFF	FFFFFFFF	3E0320D5	ACTV - ROW ADDRESS STROBE (S0~)	FE	FF	10011	197.625 ns
2047	00088	006E0064	80FBFFFF	FFFFFFFF	FFFFFFFF	WRITE - COL ADDR WRITE (S0~)	FF	FF	10100	18.000 ns
2048	00088	006E0064	00690061	006E0064	00690061	(UNKNOWN)	FF	00	10100	3.000 ns
2049	00088	006E0064	00690061	006E0064	00690061	WRITE DATA	00	00	11100	3.000 ns
2050	0008C	00070000	00540000	00070000	00750061	WRITE DATA	FF	00	11100	2.875 ns
2051	0008C	000041B8	00070510	000041B8	00570510	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3.000 ns
2052	0008C	000041B8	00070510	000041B8	00570510	WRITE DATA	00	00	10100	3.000 ns
2053	00080	00003948	00003968	00003948	000079EC	WRITE DATA	00	00	11100	3.000 ns
2054	00080	00004478	000043C8	00004478	000073E8	WRITE DATA	FF	00	11100	3.000 ns
2055	00080	00003840	00003850	00003840	000078D8	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3.000 ns
2056	00080	00003840	00003850	00003840	000078D8	WRITE DATA	00	00	10100	3.000 ns
2057	00084	00003968	000043AC	00003968	000047EC	WRITE DATA	00	00	11100	3.000 ns
2058	00084	000043C8	00003948	000043C8	000038CC	WRITE DATA	FF	00	11100	3.000 ns
2059	00084	000039F4	000043F4	000039F4	000078FC	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3.000 ns
2060	00084	000039F4	000043F4	000039F4	000078FC	WRITE DATA	00	00	10100	3.000 ns
2061	0044C	0000441C	000039DC	0000441C	000078FC	WRITE DATA	FF	00	10100	3.000 ns
2062	0044A	0000384A	000038B4	0000384A	000038FC	WRITE DATA	00	00	11010	3.000 ns
2063	0044A	00420076	00000053	00420076	000038F7	WRITE DATA	FF	00	11010	2.875 ns
2064	0004A	00070528	00080002	00070568	00080053	WRITE DATA	00	00	11010	3.000 ns
2065	0004A	00720073	00070528	00720073	000F052A	WRITE DATA	FF	00	11010	3.125 ns
2066	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	00720178	DESL - IGNORE COMMAND	00	00	11010	3.000 ns
2067	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	2.875 ns
2068	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2069	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	3.000 ns
2070	0004A	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	(UNKNOWN)	FF	FF	10010	3.000 ns

Figure 13- 400DDR2M State Display- Show All Data? = Yes

To change the display it is necessary to bring up the window’s Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in Figure 14.



**Figure 14- DDR2M400 Disassembly Properties**

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

**Burst Length** – permits setting the burst length for Read and Write data. Valid choices are 4 (the default) and 8. This value must be set properly for all valid Read and Write data to be displayed.

**CAS Latency** – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 2 (default), 3, 4, or 5 cycles.

**CAS Additive Latency** – additional latency for data cycles. This value must also be set properly for valid Read and Write Data to be displayed. Valid choices are 0 (default), 1, 2, 3, or 4 cycles.

**Registered?** – must be set to reflect whether or not Registered DDR memory is used. Default is No. When set to Yes an additional clock cycle delay is added to CAS Latency and to valid Read and Write Data tagging.

**Show All Data?** – permits choosing between displaying all DDR data (default), including Invalid Read / Write and Command data, and showing only valid Data and Command data.

**DM Signal Use** – permits setting Data Mask functionality to Write Masks (default) or Strobes. When set to Write Mask the DM signals will be used to mask Write Data to show which data bytes were valid in the cycle.

When setting **Show All Data?** to No, the display in Figure 13 then becomes the display in Figure 15. This allows the user to see at a glance the valid information on the bus.

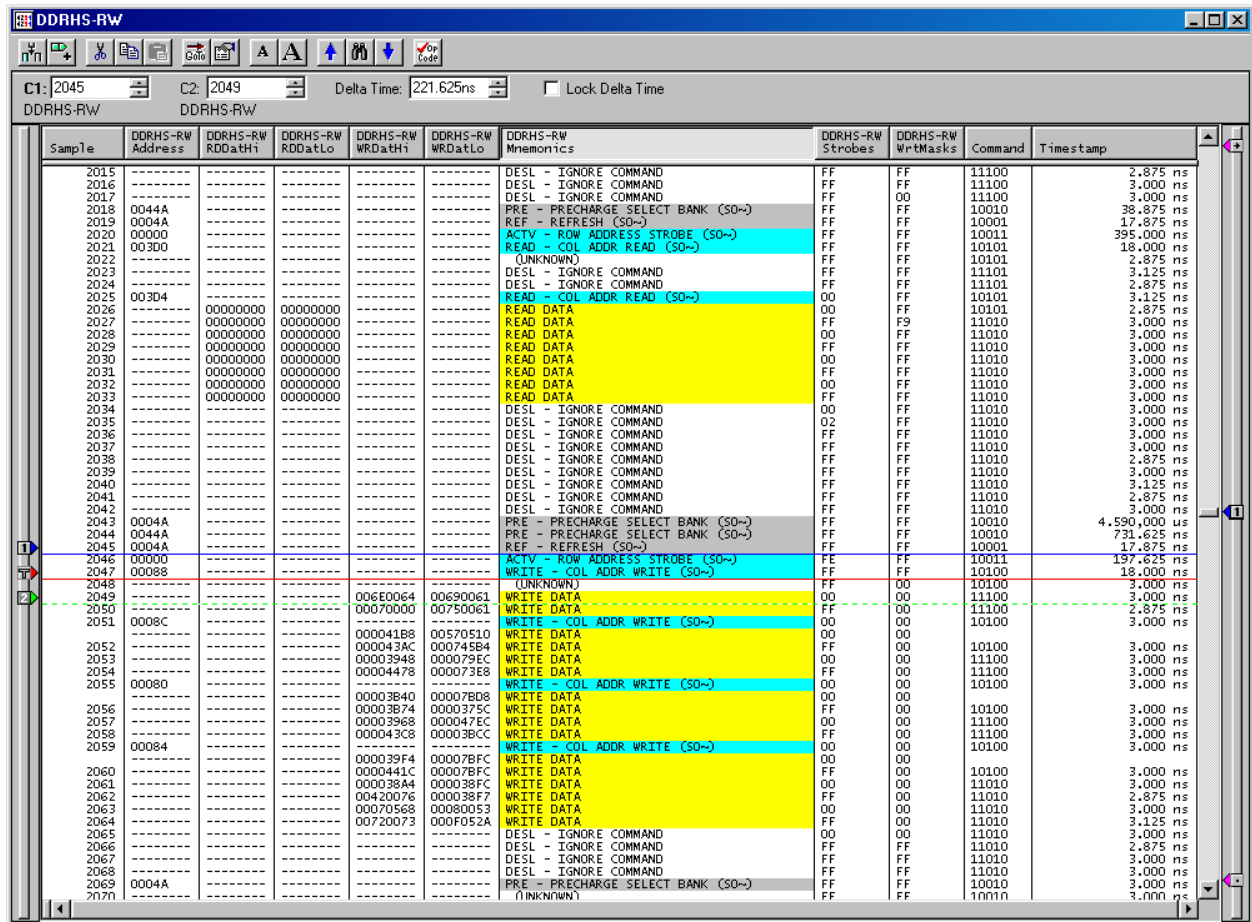


Figure 15- DDR2M400 State Display- Show All Data? = No

In addition to the Disassembly Properties selections discussed earlier, changing the settings in the **Show** field result in display changes as well:

- Hardware** – displays all acquired cycles
- Software** – suppresses all idle or wait cycles
- Control Flow** – shows Address Command and valid Read / Write data cycles
- Subroutine** – shows valid Read / Write data cycles only

Changing the Show field setting in the display of Figure 15 from Hardware-RW to Control Flow results in the display of Figure 16 where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

Sample	DDRHS-RW Address	DDRHS-RW R0DatH	DDRHS-RW R0DatLo	DDRHS-RW WRDatH	DDRHS-RW WRDatLo	DDRHS-RW Mmemorics	DDRHS-RW Strobes	DDRHS-RW WrMasks	Command	Timestamp
1993	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10101	3,000 ns
1994	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11101	3,000 ns
1995	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11101	3,000 ns
1996	003C8	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	FF	FF	10101	3,000 ns
1997	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10101	3,000 ns
1998	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11101	3,000 ns
1999	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11101	3,000 ns
2000	003CC	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	FF	FF	10101	3,000 ns
2001	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10101	2,875 ns
2002	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2003	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11010	3,000 ns
2004	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10010	3,000 ns
2005	-----	00000000	00000000	-----	-----	READ DATA	00	FF	10010	3,000 ns
2006	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11011	3,000 ns
2007	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11011	3,000 ns
2008	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11011	3,000 ns
2020	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	FF	FF	10011	478,500 ns
2021	00300	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	FF	FF	10101	18,000 ns
2025	003D4	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	00	FF	10101	12,000 ns
2026	-----	00000000	00000000	-----	-----	READ DATA	00	FF	10101	2,875 ns
2027	-----	00000000	00000000	-----	-----	READ DATA	FF	F9	11010	3,000 ns
2028	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2029	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2030	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11010	3,000 ns
2031	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2032	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11010	3,000 ns
2033	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2046	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	FF	FF	10011	5,564,000 ns
2047	00088	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	FF	FF	10100	18,000 ns
2049	-----	-----	-----	006E0064	00690061	WRITE DATA	00	00	11100	6,000 ns
2050	-----	-----	00070000	00750061	-----	WRITE DATA	FF	00	11100	2,875 ns
2051	0008C	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3,000 ns
2052	-----	000041B8	00570510	-----	-----	WRITE DATA	00	00	10100	3,000 ns
2053	-----	000043AC	000745B4	-----	-----	WRITE DATA	FF	00	10100	3,000 ns
2054	-----	00003948	000079EC	-----	-----	WRITE DATA	00	00	11100	3,000 ns
2055	00080	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	00	00	11100	3,000 ns
2056	-----	00003B40	00007B08	-----	-----	WRITE DATA	00	00	10100	3,000 ns
2057	-----	00003B74	0000375C	-----	-----	WRITE DATA	FF	00	10100	3,000 ns
2058	-----	00003968	000047EC	-----	-----	WRITE DATA	00	00	11100	3,000 ns
2059	00084	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	FF	00	11100	3,000 ns
2060	-----	000039F4	00007BFC	-----	-----	WRITE DATA	00	00	10100	3,000 ns
2061	-----	0000441C	00007BFC	-----	-----	WRITE DATA	00	00	10100	3,000 ns
2062	-----	000038A4	000038FC	-----	-----	WRITE DATA	FF	00	11010	2,875 ns
2063	-----	00420076	000038F7	-----	-----	WRITE DATA	FF	00	11010	3,000 ns
2064	-----	00070568	00080053	-----	-----	WRITE DATA	00	00	11010	3,125 ns
2064	-----	00720073	000F052A	-----	-----	WRITE DATA	FF	00	11010	3,125 ns
2077	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	7F	FF	10011	116,750 ns
2078	00088	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	FF	FF	10100	18,000 ns
2080	-----	00000000	005D0050	-----	-----	WRITE DATA	00	00	11100	6,000 ns
2081	-----	00000000	005D0050	-----	-----	WRITE DATA	FF	00	11100	3,000 ns
2082	0008C	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3,000 ns
2083	-----	00000000	00000000	-----	-----	WRITE DATA	00	00	10100	3,000 ns
2084	-----	00000000	00000000	-----	-----	WRITE DATA	FF	00	11100	3,000 ns

Figure 16- DDR2M400 State Display- Show Control Flow

### 6.3 DDR2M400 Mnemonics Description

Table 3 gives a brief description of each of the text lines displayed in the post-processing software display.

Mnemonic	Description
ACTV - ROW ADDRESS STROBE (S0~)	Active command – activate a row in a bank for subsequent access (chip select 0)
ACTV - ROW ADDRESS STROBE (S1~)	Active command – activate a row in a bank for subsequent access (chip select 1)
BST - BURST STOP (S0~)	Burst Terminate command – truncate current Read burst (chip select 0)
BST - BURST STOP (S1~)	Burst Terminate command – truncate current Read burst (chip select 1)
DESL - IGNORE COMMAND	Deselect function – no new command
MRS - MODE REGISTER SET (S0~)	Mode Register Set command – mode register load (chip select 0)
MRS - MODE REGISTER SET (S1~)	Mode Register Set command – mode register load (chip select 1)
NOP - NO OPERATION (S0~)	No Operation command (chip select 0)
NOP - NO OPERATION (S1~)	No Operation command (chip select 1)
PRE - PRECHARGE SELECT BANK (S0~)	Precharge command (chip select 0)
PRE - PRECHARGE SELECT BANK (S1~)	Precharge command (chip select 1)
READ - COL ADDR READ (S0~)	Read command – initiates a burst read access to active row (chip select 0)
READ - COL ADDR READ (S1~)	Read command – initiates a burst read access to active row (chip select 1)
READ DATA	Valid Read data on the bus
REF - REFRESH (S0~)	Self Refresh command (chip select 0)
REF - REFRESH (S1~)	Self Refresh command (chip select 1)
WRITE - COL ADDR WRITE (S0~)	Write command – initiates a burst write access to active row (chip select 0)
WRITE - COL ADDR WRITE (S1~)	Write command – initiates a burst write access to active row (chip select 1)
WRITE DATA	Valid Write data on the bus
DDRCK0, DDRCK1, & DDRCK2 INACTIVE	No active clock detected by software
(UNKNOWN)	Command Cycle on falling edge of clock

**Table 3- DDR2M400 Mnemonics Definition**

## 6.4 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: DDR2M400 and DDR2M400-MagniVu. The first (DDR2M400) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, DDR2M400-MagniVu, will show all of the channels in 8GHz MagniVu mode, so that edge relationships can be examined around the MagniVu trigger point. MagniVu is very useful and in some cases necessary to see/resolve DDR data. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

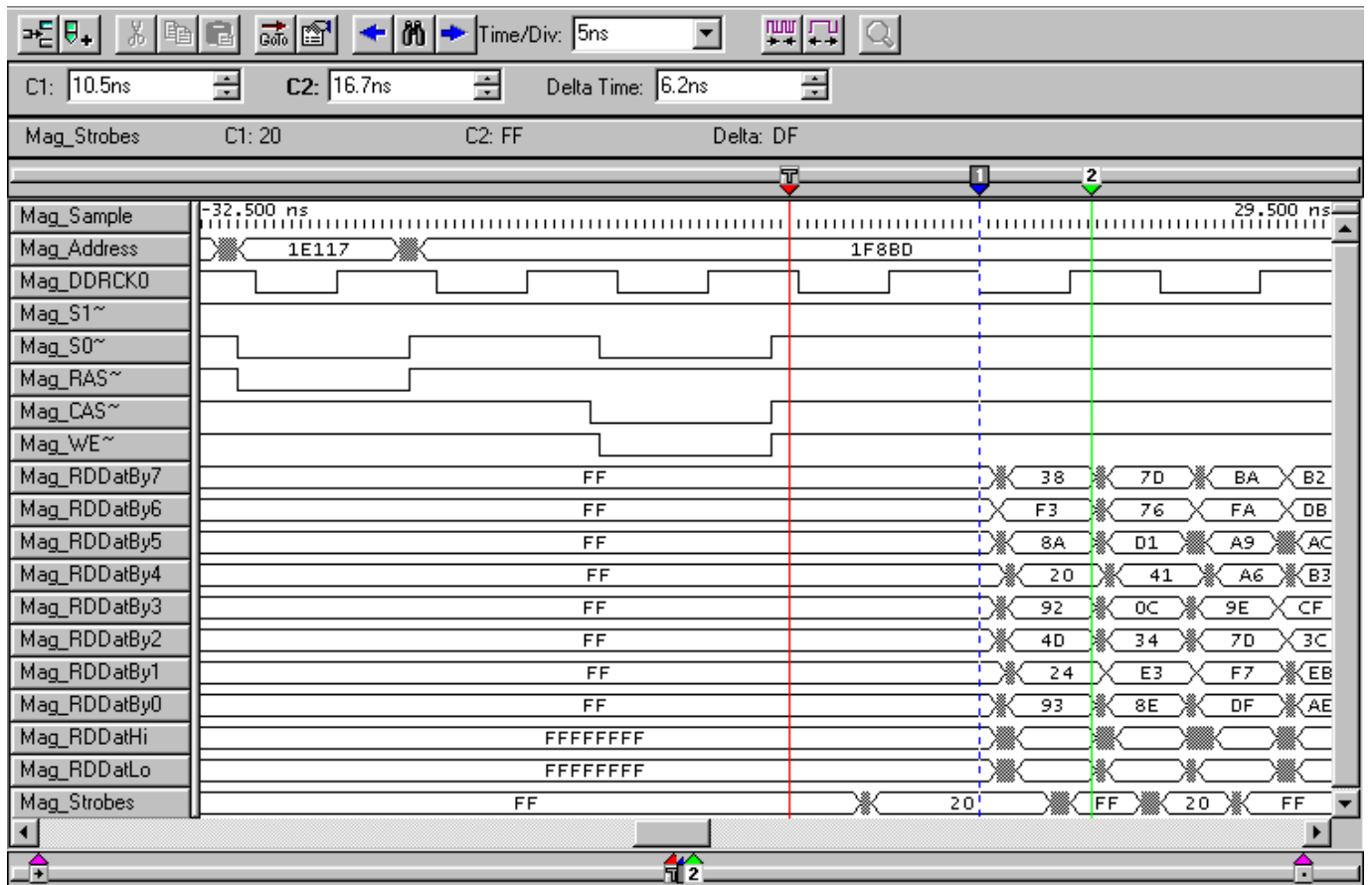


Figure 17- DDR2M400 MagniVu Display on TLA

## 7.0 HINTS & TIPS

### 7.1 Triggering on a Command

The DDR2M400 support package clocks data into the logic analyzer on both the rising and falling edges of the selected DDR Clock. Command information is only valid on the rising edge of the clock, but it is very possible (even likely) that valid information is also available on the falling edge of the clock preceding the Command's valid rising edge. This can result in a false trigger of the TLA. With the DDR2M400 post-processing software such a cycle (falling edge of DDR Clock with valid Command data) is labeled as an Unknown cycle. These cycles would be filtered out (suppressed) when changing the Disassembly Properties display mode to something other than Hardware, resulting in a Trigger position that is hidden from the user.

To eliminate this problem it is suggested that a trigger condition be defined that ANDs the desired Command with the DDR Clock channel being used for acquisition in a LOW state (see Figure 18). (Since the data stored by the TLA reflects its state before the acquisition clock occurs the DDR Clock is stored as a LOW for a rising clock edge and as a HIGH for a falling clock edge.) Figure 19 shows the actual Trigger Clause definition used in the trigger program shown in Figure 18.

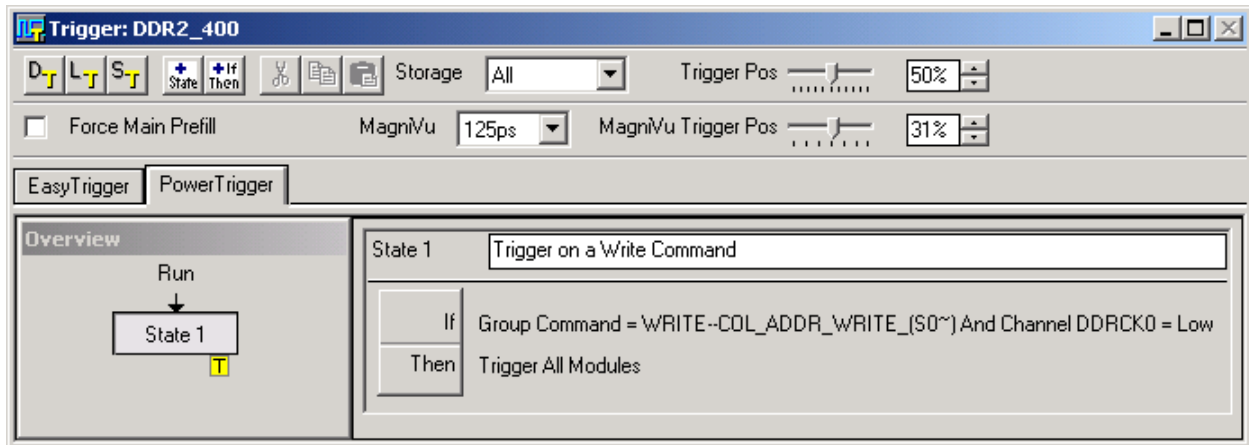


Figure 18- Recommended DDR2M400 Command Trigger

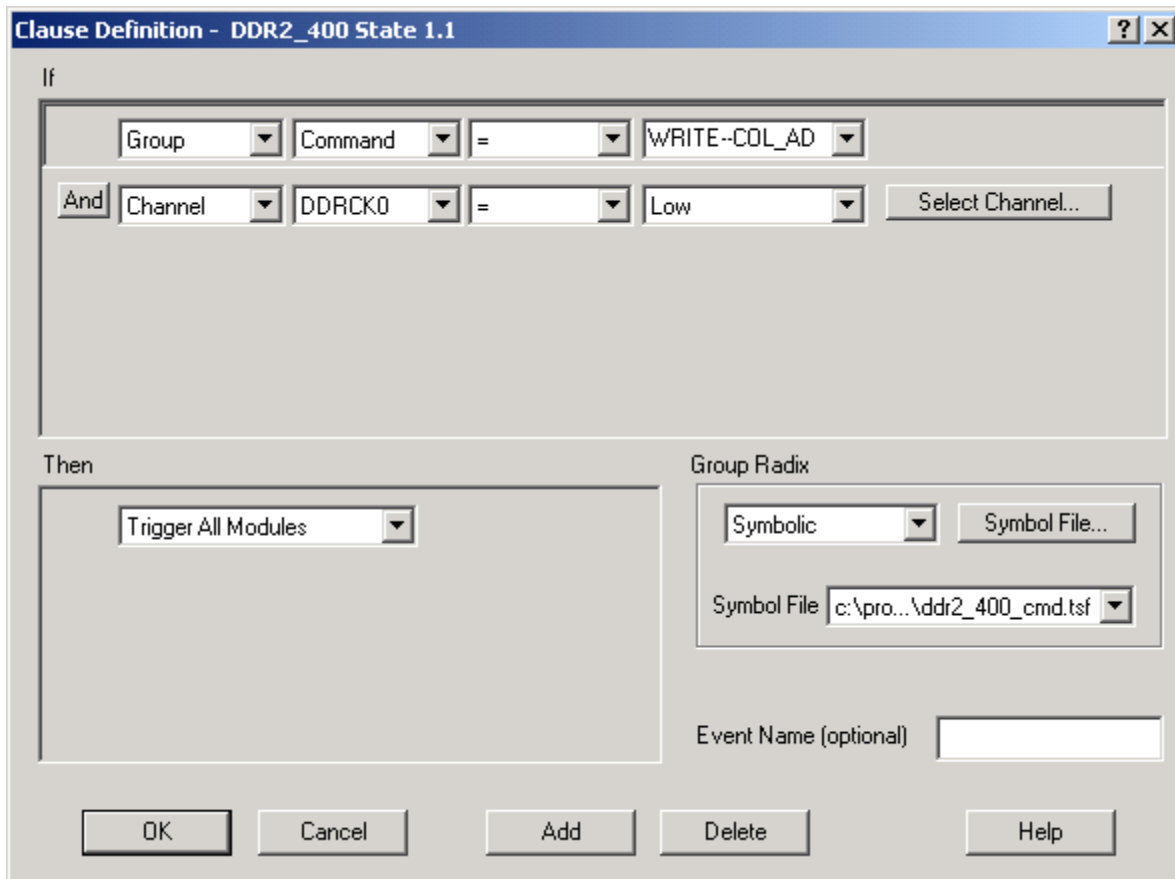


Figure 19- Recommended DDR2M400 Command Trigger - Detail

## 7.2 Capturing MRS (Mode Register Set) Data

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the DDR2M400 support for the post-processing software to properly decode the acquisitions. The TLA trigger shown in Figure 20 can be used to acquire the MRS cycles when using either of these supports.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

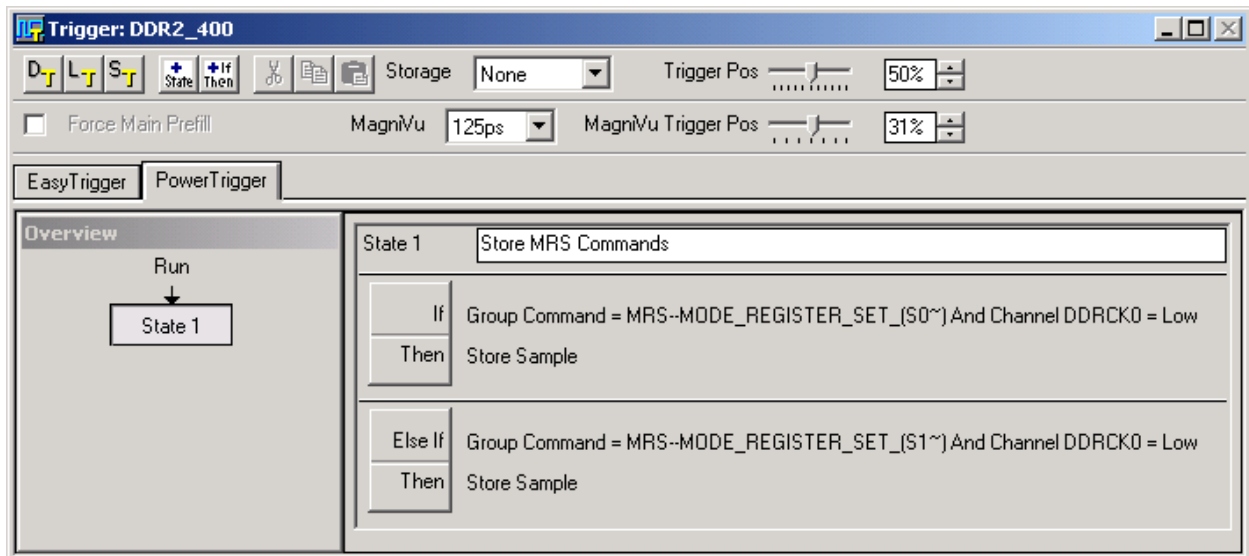


Figure 20- DDR2M400 MRS Trigger

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in Figure 21. The last acquired MRS cycle will reflect the settings used in the DDR target – in this case, a CAS latency of 2 cycles with a Burst length of 8.

Sample	DDRHS-RW Address	DDRHS-RW R0DatHi	DDRHS-RW R0DatLo	DDRHS-RW WRDatHi	DDRHS-RW WRDatLo	DDRHS-RW Mnemonics	DDRHS-RW Struc
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Normal MRS	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Normal Operation	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Latency = 2	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Burst Type = Interleaved	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Burst Length = 8	FF
35	04000	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	MRS - MODE REGISTER SET (S0~)	FF
	04000	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Reserved	FF
36	00400	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	MRS - MODE REGISTER SET (S0~)	FF
	00400	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Normal MRS	FF
	00400	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Operating Mode = Reserved	FF
	00400	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Latency = Reserved	FF
	00400	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Burst Type = Sequential	FF
	00400	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Burst Length = Reserved	FF
37	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	MRS - MODE REGISTER SET (S0~)	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Normal MRS	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Normal Operation	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Latency = 2	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Burst Type = Interleaved	FF
	0002B	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	Burst Length = 8	FF

Figure 21- MRS Cycle Acquisition Disassembly

## **APPENDIX A - How DDRII Data is Clocked**

### **A.1 Background**

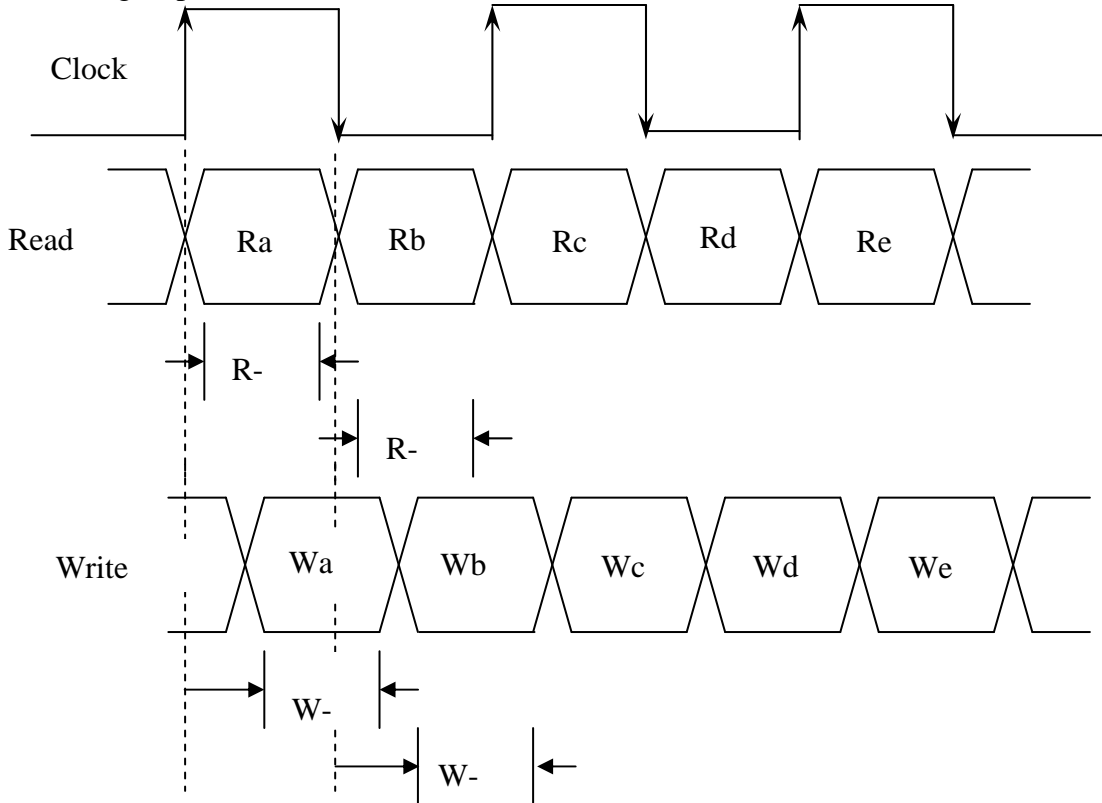
Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section *and* the D3 section. Through the User Interface of the TLA, demux can be performed by connecting the A0-A3 sections and storing the data in both the A0-A3 and D0-D3 data sections. More extensive demux capabilities are possible using the software tools that were used to create the various DDR packages. A very useful side benefit of using demux is that, since only one set of TLA data channels have to be connected, only one probe load is added to the target, even though data is stored in two different locations of the acquisition card.

### **A.2 DDR Acquisition - General**

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. The speeds of DDRII (400MHz and higher) require different setups to enable proper data acquisition. In addition, instead of trying to use the Data Strobes to acquire data our solution uses one of the DDRII SDRAM Clocks (DDRCK0, DDRCK1, or DDRCK2 user selectable) and all data acquisition is adjusted in relation to the clock edges. The 8 or 16 Data Strobes cannot be easily used to acquire data as some TLA configurations only support that number of Clock Inputs. Also, the Strobes cannot be used to acquire Address and Command information.

### A.3 DDR2M400 Support

This support requires two (2) merged 136-channel 450MHz TLA7AA4 or TLA7AB4 acquisition cards used in a TLA7XX. The merged cards enable both Read and Write data to be acquired simultaneously from a DDR system. Data is acquired using both edges of the DDR clock, and demultiplexing is done to permit acquiring both Read and Write data on every clock edge. One Sample Point must be adjusted to acquire valid Read data in reference to the clock edge; a second Sample Point must be set to acquire valid Write data in relation to the edge. Again, different Sample Points must be set for each of the Read / Write data groups (RDDatHi, RDDatLo, WRDatHi, and WRDatLo), and if necessary, sample points can be set for any of the 8-bit data groups.



Sample	Address	RDDatHi	RDDatLo	WRDatHi	WRDatLo	Command	Strobes	Timestamp
19	10011	20528000	008E0000	20528000	00070000	DESL--IGNORE_COMMAND--DATA?	20	-25,000 ns
20	142F3	20528004	00CE0000	20528000	00CE0000	ACTV--ROW_ADDRESS_STROBE_(S0~)	2C	-19,500 ns
21	142F3	20528004	0C460000	20528004	00CE0000	ACTV--ROW_ADDRESS_STROBE_(S0~)	2C	-15,000 ns
22	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	-9,500 ns
23	10011	20528000	010C0000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	-5,000 ns
24	14031	2052800C	050C0000	20528000	050C0000	READ--COL_ADDR_READ_(S0~)	20	0 ps
25	14031	20528008	040C0000	2052800C	050C0000	READ--COL_ADDR_READ_(S0~)	28	5,000 ns
26	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	10,500 ns
27	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	15,000 ns
28	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	20,000 ns
29	10011	20038C30	C30C20A2	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	25,000 ns
30	10011	2C528082	08248208	20D38C30	C30C20A2	DESL--IGNORE_COMMAND--DATA?	B4	30,500 ns
31	10011	7D77F7DF	FFDF3C7	2C528082	08248208	DESL--IGNORE_COMMAND--DATA?	60	35,500 ns
32	10011	BA739659	65155555	7D77F7DF	FFDF3C7	DESL--IGNORE_COMMAND--DATA?	FF	40,000 ns
33	10011	2EFAEBBE	FBAE39E7	BA739659	65155555	DESL--IGNORE_COMMAND--DATA?	20	45,000 ns
34	10011	E3DE84D3	4D3492C8	2EFAEBBE	FBAE39E7	DESL--IGNORE_COMMAND--DATA?	FF	50,500 ns
35	10011	FBFFBCF7	DF6D9618	E3DE84D3	4D3492C8	DESL--IGNORE_COMMAND--DATA?	20	55,500 ns
36	10011	A6DBEDB4	D75D65B6	FBFFBCF7	DF6D9618	DESL--IGNORE_COMMAND--DATA?	3C	60,500 ns
37	10011	A252A1B4	00044482	A6DBEDB4	D75D65B6	DESL--IGNORE_COMMAND--DATA?	20	65,000 ns
38	10011	A6DBEDB4	0E0761B6	A6DBEDB4	D75D65B6	DESL--IGNORE_COMMAND--DATA?	20	70,500 ns
39	10011	A802AC30	08040010	A6DBEDB4	0E0761B6	DESL--IGNORE_COMMAND--DATA?	21	75,000 ns
40	10011	2652A024	00054010	A0D2A030	00040010	PRE--PRECHARGE_SELECT_BANK_(S0~)	20	80,000 ns
41	14411	24528004	08044010	2652A024	08054010	PRE--PRECHARGE_SELECT_BANK_(S0~)	20	85,000 ns
42	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	90,500 ns
43	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	95,000 ns
44	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	22	100,500 ns

## **APPENDIX B - Considerations**

### **B.1 DDRII Bus Loading**

It must be noted that the NEX-DDRII400BM Bus Adapter does not provide any buffering of the DDRII memory signals. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using this adapter, to see the exact timing relationships and signal waveforms from the system. It is important to note that the NEX-DDRII400BM is an impedance controlled, matched trace length design. This adds greatly to its ability to maintain signal integrity and timing relationships of the DDRII bus.

## APPENDIX C - DDRII DIMM 240-pin Pinout

Front Side (left 1-60)			Back Side (right 121-180)			Front Side (left 61-120)			Back Side (right 181-240)		
Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC
1	VREF	VREF	121	VSS	VSS	61	A4	A4	181	VDDQ	VDDQ
2	VSS	VSS	122	DQ4	DQ4	62	VDDQ	VDDQ	182	A3	A3
3	DQ0	DQ0	123	DQ5	DQ5	63	A2	A2	183	A1	A1
4	DQ1	DQ1	124	VSS	VSS	64	VDD	VDD	184	VDD	VDD
5	VSS	VSS	125	DM0 DQS9	DM0 DQS9	KEY			KEY		
6	DQS0#	DQS0#	126	NC DQS9#	NC DQS9#	65	VSS	VSS	185	CK0	CK0
7	DQS0	DQS0	127	VSS	VSS	66	VSS	VSS	186	CK0#	CK0#
8	VSS	VSS	128	DQ6	DQ6	67	VDD	VDD	187	VDD	VDD
9	DQ2	DQ2	129	DQ7	DQ7	68	NC	NC	188	A0	A0
10	DQ3	DQ3	130	VSS	VSS	69	VDD	VDD	189	VDD	VDD
11	VSS	VSS	131	DQ12	DQ12	70	A10/AP	A10/AP	190	BA1	BA1
12	DQ8	DQ8	132	DQ13	DQ13	71	BA0	BA0	191	VDDQ	VDDQ
13	DQ9	DQ9	133	VSS	VSS	72	VDDQ	VDDQ	192	RAS#	RAS#
14	VSS	VSS	134	DM1 DQS10	DM1 DQS10	73	WE#	WE#	193	S0#	S0#
15	DQS1#	DQS1#	135	NC DQS10#	NC DQS10#	74	CAS#	CAS#	194	VDDQ	VDDQ
16	DQS1	DQS1	136	VSS	VSS	75	VDDQ	VDDQ	195	ODT0	ODT0
17	VSS	VSS	137	CK1,RFU	CK1,RFU	76	S1#	S1#	196	A13	A13
18	RC1	RC1	138	CK1#,RFU	CK1#,RFU	77	ODT1	ODT1	197	VDD	VDD
19	NC	NC	139	VSS	VSS	78	VDDQ	VDDQ	198	VSS	VSS
20	VSS	VSS	140	DQ14	DQ14	79	VSS	VSS	199	DQ36	DQ36
21	DQ10	DQ10	141	DQ15	DQ15	80	DQ32	DQ32	200	DQ37	DQ37
22	DQ11	DQ11	142	VSS	VSS	81	DQ33	DQ33	201	VSS	VSS
23	VSS	VSS	143	DQ20	DQ20	82	VSS	VSS	202	DM4 DQS13	DM4 DQS13
24	DQ16	DQ16	144	DQ21	DQ21	83	DQS4#	DQS4#	203	NC DQS13#	NC DQS13#
25	DQ17	DQ17	145	VSS	VSS	84	DQS4	DQS4	204	VSS	VSS
26	VSS	VSS	146	DM2 DQS11	DM2 DQS11	85	VSS	VSS	205	DQ38	DQ38
27	DQS2#	DQS2#	147	NC DQS11#	NC DQS11#	86	DQ34	DQ34	206	DQ39	DQ39
28	DQS2	DQS2	148	VSS	VSS	87	DQ35	DQ35	207	VSS	VSS
29	VSS	VSS	149	DQ22	DQ22	88	VSS	VSS	208	DQ44	DQ44
30	DQ18	DQ18	150	DQ23	DQ23	89	DQ40	DQ40	209	DQ45	DQ45
31	DQ19	DQ19	151	VSS	VSS	90	DQ41	DQ41	210	VSS	VSS

32	VSS	VSS	152	DQ28	DQ28	91	VSS	VSS	211	DM5 DQS14	DM5 DQS14
33	DQ24	DQ24	153	DQ29	DQ29	92	DQS5#	DQS5#	212	NC DQS14#	NC DQS14#
34	DQ25	DQ25	154	VSS	VSS	93	DQS5	DQS5	213	VSS	VSS
35	VSS	VSS	155	DM3 DQS12	DM3 DQS12	94	VSS	VSS	214	DQ46	DQ46
36	DQS3#	DQS3#	156	NC DQS12#	NC DQS12#	95	DQ42	DQ42	215	DQ47	DQ47
37	DQS3	DQS3	157	VSS	VSS	96	DQ43	DQ43	216	VSS	VSS
38	VSS	VSS	158	DQ30	DQ30	97	VSS	VSS	217	DQ52	DQ52
39	DQ26	DQ26	159	DQ31	DQ31	98	DQ48	DQ48	218	DQ53	DQ53
40	DQ27	DQ27	160	VSS	VSS	99	DQ49	DQ49	219	VSS	VSS

NC = No Connect; NU = Not Useable; RFU = Reserved Future Use

## APPENDIX C - DDRII DIMM 240-pin Pinout (cont'd.)

Front Side (left 1-60)			Back Side (right 121-180)			Front Side (left 61-120)			Back Side (right 181-240)		
Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC
41	VSS	VSS	161	NC	CB4	100	VSS	VSS	220	CK2 RFU	CK2 RFU
42	NC	CB0	162	NC	CN5	101	SA2	SA2	221	CK2# RFU	CK2# RFU
43	NC	CB1	163	VSS	VSS	102	NC TEST	NC TEST	222	VSS	VSS
44	VSS	VSS	164	NC	DM8 DQS17	103	VSS	VSS	223	DM6 DQS15	DM6 DQS15
45	NC	DQS8#	165	NC	NC DQS17#	104	DQS6#	DQS6#	224	NC DQS15#	NC DQS15#
46	NC	DQS8	166	VSS	VSS	105	DQS6	DQS6	225	VSS	VSS
47	VSS	VSS	167	NC	CB6	106	VSS	VSS	226	DQ54	DQ54
48	NC	CB2	168	NC	CB7	107	DQ50	DQ50	227	DQ55	DQ55
49	NC	CB3	169	VSS	VSS	108	DQ51	DQ51	228	VSS	VSS
50	VSS	VSS	170	VDDQ	VDDQ	109	VSS	VSS	229	DQ60	DQ60
51	VDDQ	VDDQ	171	CKE1	CKE1	110	DQ56	DQ56	230	DQ61	DQ61
52	CKE0	CKE0	172	VDD	VDD	111	DQ57	DQ57	231	VSS	VSS
53	VDD	VDD	173	A15	A15	112	VSS	VSS	232	DM7 DQS16	DM7 DQS16
54	A16,BA2	A16,BA2	174	A14	A14	113	DQS7#	DQS7#	233	NC DQS16#	NC DQS16#
55	RC0	RC0	175	VDDQ	VDDQ	114	DQS7	DQS7	234	VSS	VSS
56	VDDQ	VDDQ	176	A12	A12	115	VSS	VSS	235	DQ62	DQ62
57	A11	A11	177	A9	A9	116	DQ58	DQ58	236	DQ63	DQ63
58	A7	A7	178	VDD	VDD	117	DQ59	DQ59	237	VSS	VSS
59	VDD	VDD	179	A8	A8	118	VSS	VSS	238	VDDSPD	VDDSPD
60	A5	A5	180	A6	A6	119	SDA	SDA	239	SA0	SA0
						120	SCL	SCL	240	SA1	SA1

NC = No Connect; NU = Not Useable; RFU = Reserved Future Use

## **APPENDIX D- NEX-DDR2400BM P6860 Compression Pinouts**

For further information on the P6860 Connectorless probe compression footprint please refer to the “P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

Pad #	TLA Channel	DDR2 Pin #	DDR2 Signal
A15	Q3-		GND
A13	Q3+		GND
B12	E3:7	122	DQ4
B10	E3:6	3	DQ0
A12	E3:5	123	DQ5
A10	E3:4	4	DQ1
B9	E3:3	128	DQ6
B7	E3:2	9	DQ2
A9	E3:1	129	DQ7
A7	E3:0	10	DQ3
B6	E2:7	131	DQ12
B4	E2:6	12	DQ8
A6	E2:5	132	DQ13
A4	E2:4	13	DQ9
B3	E2:3		GND
B1	E2:2		GND
A3	E2:1		GND
A1	E2:0		GND

P6860 Probe Connection MA - E2 / E3

Pad #	TLA Channel	DDR2 Pin #	DDR2 Signal
A15	CK1-	138	CK1#_RFU
A13	CK1+	137	CK1_RFU
B12	A1:7	146	DM2_DQS11
B10	A1:6	28	DQS2
A12	A1:5	147	NC_DQS11#
A10	A1:4	27	DQS2#
B9	A1:3		GND
B7	A1:2		GND
A9	A1:1	19	NC19
A7	A1:0	18	RC1_RESET#
B6	A0:7	16	DQS1
B4	A0:6	135	NC_DQS10#
A6	A0:5	15	DQS1#
A4	A0:4	134	DM1_DQS10
B3	A0:3	7	DQS0
B1	A0:2	126	NC_DQS9#
A3	A0:1	6	DQS0#
A1	A0:0	125	DM0_DQS9

P6860 Probe Connection MA - A0 / A1

## APPENDIX D- NEX-DDRII400BM P6860 Compression Pinouts (cont'd.)

Pad #	TLA Channel	DDRII Pin #	DDRII Signal
A15	CK3-		GND
A13	CK3+	76	S1#
B12	C3:7	102	NC_TEST
B10	C3:6	101	SA2
A12	C3:5	93	DQS5
A10	C3:4	212	NC_DQS14#
B9	C3:3	92	DQS5#
B7	C3:2	211	DM5_DQS14
A9	C3:1	84	DQS4
A7	C3:0	203	NC_DQS13#
B6	C2:7	83	DQS4#
B4	C2:6	202	DM4_DQS13
A6	C2:5	196	A13
A4	C2:4	195	ODT0
B3	C2:3	74	CAS#
B1	C2:2	193	S0#
A3	C2:1	73	WE#
A1	C2:0	192	RAS#

P6860 Probe Connection MA - C2 / C3

Pad #	TLA Channel	DDRII Pin #	DDRII Signal
A15	CK0-	221	CK2#_RFU
A13	CK0+	220	CK2_RFU
B12	A3:7	223	DM6_DQS15
B10	A3:6	104	DQS6#
A12	A3:5	224	NC_DQS15#
A10	A3:4	105	DQS6
B9	A3:3	232	DM7_DQS16
B7	A3:2	113	DQS7#
A9	A3:1	233	NC_DQS16#
A7	A3:0	114	DQS7
B6	A2:7	119	SDA
B4	A2:6	239	SA0
A6	A2:5	120	SCL
A4	A2:4	240	SA1
B3	A2:3		GND
B1	A2:2		GND
A3	A2:1		GND
A1	A2:0		GND

P6860 Probe Connection MA – A2 / A3

## APPENDIX D- NEX-DDR2400BM P6860 Compression Pinouts (cont'd.)

Pad #	TLA Channel	DDR2 Pin #	DDR2 Signal
A15	CK0-		GND
A13	CK0+		GND
B12	A3:7	199	DQ36
B10	A3:6	80	DQ32
A12	A3:5	200	DQ37
A10	A3:4	81	DQ33
B9	A3:3	205	DQ38
B7	A3:2	86	DQ34
A9	A3:1	206	DQ39
A7	A3:0	87	DQ35
B6	A2:7	208	DQ44
B4	A2:6	89	DQ40
A6	A2:5	209	DQ45
A4	A2:4	90	DQ41
B3	A2:3	214	DQ46
B1	A2:2	95	DQ42
A3	A2:1	215	DQ47
A1	A2:0	96	DQ43

P6860 Probe Connection SL - A2 / A3

Pad #	TLA Channel	DDR2 Pin #	DDR2 Signal
A15	CK2-	186	CK0#
A13	CK2+	185	CK0
B12	D1:7	177	A9
B10	D1:6	58	A7
A12	D1:5	179	A8
A10	D1:4	60	A5
B9	D1:3	180	A6
B7	D1:2	61	A4
A9	D1:1	182	A3
A7	D1:0	63	A2
B6	D0:7	183	A1
B4	D0:6	68	NC68
A6	D0:5	188	A0
A4	D0:4	70	A10/AP
B3	D0:3	190	BA1
B1	D0:2	71	BA0
A3	D0:1	77	ODT1
A1	D0:0		GND

P6860 Probe Connection MA -D1 / D0

## APPENDIX D- NEX-DDRII400BM P6860 Compression Pinouts (cont'd.)

Pad #	TLA Channel	DDRII Pin #	DDRII Signal
A15	Q1-		GND
A13	Q1+		GND
B12	C1:7	155	DM3_DQS12
B10	C1:6	36	DQS3#
A12	C1:5	156	NC_DQS12#
A10	C1:4	37	DQS3
B9	C1:3	164	NC_DM8_DQS17
B7	C1:2	45	NC_DQS8#
A9	C1:1	165	NC_DQS17#
A7	C1:0	46	NC_DQS8
B6	C0:7	171	CKE1
B4	C0:6	52	CKE0
A6	C0:5	173	A15
A4	C0:4	54	A16_BA2
B3	C0:3	174	A14
B1	C0:2	55	RC0
A3	C0:1	176	A12
A1	C0:0	57	A11

P6860 Probe Connection MA – C0 / C1

Pad #	TLA Channel	DDRII Pin #	DDRII Signal
A15	Q3-		GND
A13	Q3+		GND
B12	E3:7	217	DQ52
B10	E3:6	98	DQ48
A12	E3:5	218	DQ53
A10	E3:4	99	DQ49
B9	E3:3	226	DQ54
B7	E3:2	107	DQ50
A9	E3:1	227	DQ55
A7	E3:0	108	DQ51
B6	E2:7	229	DQ60
B4	E2:6	110	DQ56
A6	E2:5	230	DQ61
A4	E2:4	111	DQ57
B3	E2:3	235	DQ62
B1	E2:2	116	DQ58
A3	E2:1	236	DQ63
A1	E2:0	117	DQ59

P6860 Probe Connection SL – E2 / E3

## APPENDIX D- NEX-DDRII400BM P6860 Compression Pinouts (cont'd.)

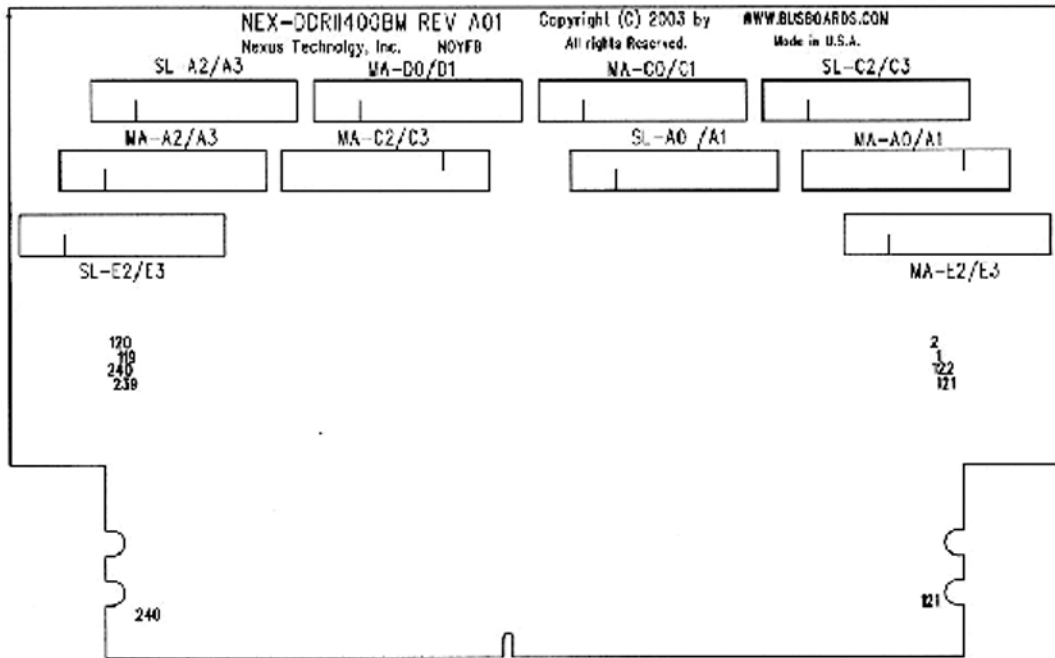
Pad #	TLA Channel	DDRII Pin #	DDRII Signal
A15	CK1-		GND
A13	CK1+		GND
B12	A1:7	158	DQ30
B10	A1:6	39	DQ26
A12	A1:5	159	DQ31
A10	A1:4	40	DQ27
B9	A1:3	161	NC_CB4
B7	A1:2	42	NC_CB0
A9	A1:1	162	NC_CB5
A7	A1:0	43	NC_CB1
B6	A0:7	167	NC_CB6
B4	A0:6	48	NC_CB2
A6	A0:5	168	NC_CB7
A4	A0:4	49	NC_CB3
B3	A0:3		GND
B1	A0:2		GND
A3	A0:1		GND
A1	A0:0		GND

P6860 Probe Connection SL – A1 / A0

Pad #	TLA Channel	DDRII Pin #	DDRII Signal
A15	CK3-		GND
A13	CK3+		GND
B12	C3:7	140	DQ14
B10	C3:6	21	DQ10
A12	C3:5	141	DQ15
A10	C3:4	22	DQ11
B9	C3:3	143	DQ20
B7	C3:2	24	DQ16
A9	C3:1	144	DQ21
A7	C3:0	25	DQ17
B6	C2:7	149	DQ22
B4	C2:6	30	DQ18
A6	C2:5	150	DQ23
A4	C2:4	31	DQ19
B3	C2:3	152	DQ28
B1	C2:2	33	DQ24
A3	C2:1	153	DQ29
A1	C2:0	34	DQ25

P6860 Probe Connection SL – C2/C3

# APPENDIX E - NEX-DDR2400BM Silkscreen



Backside (Mirror Image Interposer)

## **APPENDIX F – Data Group / Data Byte / Strobe Cross-Reference**

32-bit Data Group	4-bit Data Group	Strobe	Data Bits
RDDatHi	RDDatNib16	DQS16	63,62,61,60
	RDDatNib7	DQS7	59,58,57,56
	RDDatNib15	DQS15	55,54,53,52
	RDDatNib6	DQS6	51,50,49,48
	RDDatNib14	DQS14	47,46,45,44
	RDDatNib5	DQS5	43,42,41,40
	RDDatNib13	DQS13	39,38,37,36
	RDDatNib4	DQS4	35,34,33,32
RDDatLo	RDDatNib12	DQS12	31,30,29,28
	RDDatNib3	DQS3	27,26,25,24
	RDDatNib11	DQS11	23,22,21,20
	RDDatNib2	DQS2	19,18,17,16
	RDDatNib10	DQS10	15,14,13,12
	RDDatNib1	DQS1	11,10,9,8
	RDDatNib9	DQS9	7,6,5,4
	RDDatNib0	DQS0	3,2,1,0
WRDatHi	WRDatNib16	DQS16	63,62,61,60
	WRDatNib7	DQS7	59,58,57,56
	WRDatNib15	DQS15	55,54,53,52
	WRDatNib6	DQS6	51,50,49,48
	WRDatNib14	DQS14	47,46,45,44
	WRDatNib5	DQS5	43,42,41,40
	WRDatNib13	DQS13	39,38,37,36
	WRDatNib4	DQS4	35,34,33,32
WRDatLo	WRDatNib12	DQS12	31,30,29,28
	WRDatNib3	DQS3	27,26,25,24
	WRDatNib11	DQS11	23,22,21,20
	WRDatNib2	DQS2	19,18,17,16
	WRDatNib10	DQS10	15,14,13,12
	WRDatNib1	DQS1	11,10,9,8
	WRDatNib9	DQS9	7,6,5,4
	WRDatNib0	DQS0	3,2,1,0

DDR2 Groups/Bytes/Strobes Cross Reference

## **APPENDIX F – Data Group / Data Byte / Strobe Cross-Reference (cont'd)**

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
RdDatHi	RDDatBy7	DQS7	63,62,61,60,59,58,57,56
	RDDatBy6	DQS6	55,54,53,52,51,50,49,48
	RDDatBy5	DQS5	47,46,45,44,43,42,41,40
	RDDatBy4	DQS4	39,38,37,36,35,34,33,32
RdDatLo	RDDatBy3	DQS3	31,30,29,28,27,26,25,24
	RDDatBy2	DQS2	23,22,21,20,19,18,17,16
	RDDatBy1	DQS1	15,14,13,12,11,10,9,8
	RDDatBy0	DQS0	7,6,5,4,3,2,1,0
WrDatHi	WRDatBy7	DQS7	63,62,61,60,59,58,57,56
	WRDatBy6	DQS6	55,54,53,52,51,50,49,48
	WRDatBy5	DQS5	47,46,45,44,43,42,41,40
	WRDatBy4	DQS4	39,38,37,36,35,34,33,32
WrDatLo	WRDatBy3	DQS3	31,30,29,28,27,26,25,24
	WRDatBy2	DQS2	23,22,21,20,19,18,17,16
	WRDatBy1	DQS1	15,14,13,12,11,10,9,8
	WRDatBy0	DQS0	7,6,5,4,3,2,1,0

DDRII Groups/Bytes/Strobes Cross Reference

## **APPENDIX G - References**

Tektronix TLA700 System User's Manual

Tektronix TLA700 Logic Analyzer User's Manual

P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual  
Tektronix part number 071-1059-00

Elpida 1GB Unbuffered DDR2 SDRAM DIMM  
Document #E0365E10, March 2003

Elpida 1GB Registered DDR2 SDRAM DIMM  
Document #E0366E20, April 2003

## **APPENDIX H - Support**

### **About Nexus Technology, Inc.**



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.  
78 Northeastern Blvd. #2  
Nashua, NH 03062

TEL: 877-595-8116  
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

### **Support Contact Information**

Technical Support	<b><a href="mailto:techsupport@nexustechnology.com">techsupport@nexustechnology.com</a></b>
General Information	<b><a href="mailto:support@nexustechnology.com">support@nexustechnology.com</a></b>
Quote Requests	<b><a href="mailto:quotes@nexustechnology.com">quotes@nexustechnology.com</a></b>

We will try to respond within one business day.

### **If Problems Are Found**

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Please do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.