NEX-DDRII400DC

DDRII 400 Synchronous DRAM Interposer Support

Including these Software Support packages:

DDR2DC2A DDRSPA

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1.0 OVERVIEW

1.1 General Information

The NEX-DDRII400DC adapter is an extender design and does not require a dedicated DDRII DIMM slot. It provides quick and easy connections to interface a TLA700 Logic Analyzer to a 240-pin DIMM socket to support DDRII SDRAM. Connections to the Logic Analyzer are made through built in coax cable to help minimize the size of the adapter board, thus reducing trace length and keeping signal loading to a minimum. This design technique also produces a very narrow adapter.

A software support package has been included with the NEX-DDRII400DC adapter to support 400MT/s DDRII DIMM:

> **DDR2DC2A** allows the user to acquire DDRII 400 Read **AND** Write data from a target. This support requires two merged TLA7AA4 or TLA7AB4 136-channel 450MHz state speed acquisition cards and no addition Tektronix probes.

The NEX-DDRII400DC software also post-processes the acquisition to display valid cycle information to the user.

The NEX-DDRII400DC support is usable with a TLA7XX-series Logic Analyzer only, and the TLA must be running V4.2 or later of the TLA Application Software.

Note that this manual uses some terms generically. For instance, references to the TLA700 apply to all suitable TLA700 Logic Analyzers. DDR400DC refers to the DDR2DC2A software support packages.

Appendix E has a silk-screened print of the NEX-DDRII400DC DIMM adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the DDRII SDRAM DIMM Specification and the Tektronix TLA700 Logic Analyzers. It is also expected that the user is familiar with the Windows environment used on the TLA.

2.0 SOFTWARE INSTALLATION

The NEX-DDRII400DC software is installed using the same method as other Windows programs. Place the DDR2DC2A Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer module in the Setup window, select Load Support Package from the File pull-down, then choose either DDR2DC2A and click on **Okay**. Note that the selected support will require two merged modules and that the TLA acquisition cards must be configured properly for the software to load.

3.0 CONNECTING to the NEX-DDRII400DC Adapter

3.1 General

Care should be taken to support the weight of the acquisition probes so that the Logic Analyzer adapter board and/or target DIMM socket are not damaged

To acquire DDRII Read and Write data at speeds up to 400MT/s will require two merged TLA7Ax4 136-channel 450MHz state speed acquisition cards and the use of the **DDR2DC2A** support software. The Master acquisition card will be in the lower-numbered mainframe slots while the Slave card will be in the adjacent higher-numbered slots. The NEX-DDRII400DC Logic Analyzer DIMM adapter should be connected to the TLA acquisition cards as follows using the eight (8) attached coax cables:

NEX-DDRII400DC Adapter M_A3/A2 cable to TLA Master A3/A2 probe connection
NEX-DDRII400DC Adapter M_A1/A0 cable to TLA Master A1/A0 probe connection
NEX-DDRII400DC Adapter M_C3/C2 cable to TLA Master C3/C2 probe connection
NEX-DDRII400DC Adapter M_C1/C0 cable to TLA Master C1/C0 probe connection
NEX-DDRII400DC Adapter M_E3/E2 cable to TLA Master E3/E2 probe connection
NEX-DDRII400DC Adapter M_E1/E0 cable to TLA Master E1/E0 probe connection
NEX-DDRII400DC Adapter S_A3/A2 cable to TLA Slave A3/A2 probe connection
NEX-DDRII400DC Adapter S_A1/A0 cable to TLA Slave A1/A0 probe connection
NEX-DDRII400DC Adapter S_C3/C2 cable to TLA Slave C3/C2 probe connection
NEX-DDRII400DC Adapter S_E3/E2 cable to TLA Slave E3/E2 probe connection

This support requires NO Tektronix probes.

The below is a photo of the support:

3.2 Channel Grouping

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RDDatHi	RD_DQ63	236	M_E3:3	RDDatLo	RD_DQ31	159	S_C3:2
(Hex)	RD_DQ62	235	M_E3:6	(Hex)	RD_DQ30	158	S_CK3+
	RD_DQ61	230	M_E1:1		RD_DQ29	153	S_C3:1
	RD_DQ60	229	M_E1:0		RD_DQ28	152	S_C3:6
	RD_DQ59	117	M_E3:4		RD_DQ27	40	S_CK1+
	RD_DQ58	116	M_E3:5		RD_DQ26	39	S_A1:0
	RD_DQ57	111	M_E0:6		RD_DQ25	34	S_A1:6
	RD_DQ56	110	M_E0:3		RD_DQ24	33	S_A1:4
	RD_DQ55	227	M_E0:5		RD_DQ23	150	S_C3:4
	RD_DQ54	226	M_ E0:0		RD_DQ22	149	S_C3:7
	RD_DQ53	218	M_ A0:3		RD_DQ21	144	M_A2:3
	RD_DQ52	217	M_ A0:1		RD_DQ20	143	M_A2:1
	RD_DQ51	108	M_E0:2		RD_DQ19	31	S_A1:7
	RD_DQ50	107	S_E2:2		RD_DQ18	30	S_ A1:5
	RD_DQ49	99	S_E2:4		RD_DQ17	25	S_ A2:3
	RD_DQ48	98	S_E2:7		RD_DQ16	24	S_ A2:1
	RD_DQ47	215	M_ A0:6		RD_DQ15	141	M_A2:6
	RD_DQ46	214	M_ A0:4		RD_DQ14	140	M_A2:4
	RD_DQ45	209	M_A1:2		RD_DQ13	132	M_A3:2
	RD_DQ44	208	M_A1:0		RD_DQ12	131	M_A3:0
	RD_DQ43	96	M_A2:5		RD_DQ11	22	S_A2:6
	RD_DQ42	95	S_E3:2		RD_DQ10	21	S_A2:4
	RD_DQ41	90	S_ E3:3		RD_DQ9	13	S_CK0+
	RD_DQ40	89	S_ E3:1		RD_DQ8	12	S_A3:0
	RD_DQ39	206	M_A1:3		RD_DQ7	129	M_A3:3
	RD_DQ38	205	M_ A1:1		RD_DQ6	128	M_A3:1
	RD_DQ37	200	M_A1:7		RD_DQ5	123	M_A3:7
	RD_DQ36	199	M_A1:5		RD_DQ4	122	M_A3:5
	RD_DQ35	87	S_ E3:6		RD_DQ3	10	S_A3:3
	RD_DQ34	86	S_ E3:4		RD_DQ2	9	S_A3:1
	RD_DQ33	81	S_ E3:7		RD_DQ1	4	S_A3:7
	RD_DQ32	80	S_ E3:5		RD_DQ0	3	S_A3:5

Table 1- DDR2DC2A (400MT/s Read and Write) TLA Channel Grouping

Notes:

1. All signals are required for accurate post-processing of acquired data
2. The ‘S’ in front of a TLA channel denotes the Slave card of the merged pair
3. The ‘M’ in front of a TLA channel denotes the Master card of the merged pair

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
WRDatHi	WR_DQ63	236	M_E1:3	WRDatLo	WR_DQ31	159	S_C1:2
(Hex)	WR_DQ62	235	M_E1:4	(Hex)	WR_DQ30	158	S_Q3+
	WR_DQ61	230	M_E3:1		WR_DQ29	153	S_C1:1
	WR_DQ60	229	M_ E3:0		WR_DQ28	152	S_C1:6
	WR_DQ59	117	M_E1:6		WR_DQ27	40	S_Q1+
	WR_DQ58	116	M_E1:7		WR_DQ26	39	S_D1:0
	WR_DQ57	111	M_ E2:6		WR_DQ25	34	S_D1:6
	WR_DQ56	110	M_E2:3		WR_DQ24	33	S_D1:4
	WR_DQ55	227	M_ E2:5		WR_DQ23	150	S_C1:4
	WR_DQ54	226	M_E2:2		WR_DQ22	149	S_C1:7
	WR_DQ53	218	M_ D0:3		WR_DQ21	144	M_D2:3
	WR_DQ52	217	M_ D0:1		WR_DQ20	143	M_D2:1
	WR_DQ51	108	M_ E2:0		WR_DQ19	31	S_A3:7
	WR_DQ50	107	S_E0:2		WR_DQ18	30	S_ A3:5
	WR_DQ49	99	S_E0:4		WR_DQ17	25	S_ A0:3
	WR_DQ48	98	S_E0:7		WR_DQ16	24	S_ A0:1
	WR_DQ47	215	M_ D0:6		WR_DQ15	141	M_D2:6
	WR_DQ46	214	M_ D0:4		WR_DQ14	140	M_D2:4
	WR_DQ45	209	M_D1:2		WR_DQ13	132	M_D3:2
	WR_DQ44	208	M_D1:0		WR_DQ12	131	M_D3:0
	WR_DQ43	96	M_D2:5		WR_DQ11	22	S_A0:6
	WR_DQ42	95	S_E1:2		WR_DQ10	21	S_A0:4
	WR_DQ41	90	S_ E1:3		WR_DQ9	13	S_Q0+
	WR_DQ40	89	S_ E1:1		WR_DQ8	12	S_A1:0
	WR_DQ39	206	M_D1:3		WR_DQ7	129	M_A1:3
	WR_DQ38	205	M_ D1:1		WR_DQ6	128	M_A1:1
	WR_DQ37	200	M_D1:7		WR_DQ5	123	M_A1:7
	WR_DQ36	199	M_D1:5		WR_DQ4	122	M_A1:5
	WR_DQ35	87	S_ E1:6		WR_DQ3	10	S_A1:3
	WR_DQ34	86	S_ E1:4		WR_DQ2	9	S_A1:1
	WR_DQ32	81	S_ E1:7		WR_DQ1	4	S_A1:7
	WR_DQ33	80	S_ E1:5		WR_DQ0	3	S_A1:5

Table 1 – DDR2DC2A (400MT/s Read and Write) TLA Channel Grouping (cont'd)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
3. The 'M' in front of a TLA channel denotes the Master card of the merged pair
4. All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
DataMsks	DM7_DQS16	232	S_Q3+	Strobes	DQS7	114	M_E1:2
(BIN)	DM6_DQS15	223	M_E0:1	(HEX)	DQS6	105	S_E2:0
	DM5_DQS14	211	M_A0:5		DQS5	93	S_Q3+
	DM4_DQS13	202	M_A1:6		DQS4	84	M_C2:6
	DM3_DQS12	155	S_C3:3		DQS3	37	S_A1:3
	DM2_DQS11	146	M_A2:0		DQS2	28	S_A2:1
	DM1_DQS10	134	M_A2:5		DQS1	16	S_A2:5
	DM0_DQS9	125	M_A3:4		DQS0	7	S_A3:6
Address	BA1	190	M_C3:6	Hi_Strobes	DM7_DQS16	232	S_Q3+
(Hex)	BA0	71	M_C1:6	(BIN)	DM6_DQS15	223	M_E0:1
	A13	196	M_C2:6		DM5_DQS14	211	M_A0:5
	A12	176	M_C0:1		DM4_DQS13	202	M_A1:6
	A11	57	M_C0:2		DM3_DQS12	155	S_C3:3
	A10/AP	70	M_C1:3		DM2_DQS11	146	M_A2:0
	A9	177	M_C0:4		DM1_DQS10	134	M_A2:5
	A8	179	M_C0:5		DM0_DQS9	125	M_A3:4
	A7	58	M_C0:3	Misc	DDRCK2+/-	220/221	M_CK1
	A6	180	M_C1:0	(OFF)	DDRCK1+/-	137/138	M_CK0
	A5	60	M_C0:6		DDRCK0+/-	185/186	M_CK3
	A4	61	M_ C0:7	Cmd	S1#	76	M_C2:0
	A3	182	M_ C1:1	(Sym)	S0#	193	M_C2:2
	A2	63	M_ C1:2		RAS#	192	M_C2:3
	A1	183	M_ C1:4		CAS#	74	M_C2:1
	A0	188	M_ C3:7		WE#	73	M_Q1+

Table 1 – DDR2DC2A (400MT/s Read and Write) TLA Channel Grouping (cont'd)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. ' # ' denotes a low-true signal
3. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
4. The 'M' in front of a TLA channel denotes the Master card of the merged pair

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RDChkBits	RD _CB7	168	S_C2:3	Ungrouped	CKE1	171	S_C2:0
	RD _CB6	167	S_C2:1		CKE0	52	S_A0:3
	RD _CB5	162	S_C2:7		A15	173	S_C2:2
	RD _CB4	161	S_C2:5		A14	174	M_C0:2
	RD _CB3	49	S_A0:1		ODT1	77	M_C3:4
	RD _CB2	48	S_ A0:6		ODT0	195	M_C2:7
	RD _CB1	43	S_ A0:5		SCL	120	M_E2:1
	RD _CB0	42	S_ A1:2		SDA	119	M_E2:4
WRChkBits	WR _CB7 [3]	168	S_C0:3		SA1	240	M_E2:7
	WR _CB6 [3]	167	S_C0:1		SA0	239	M_E3:2
	WR _CB5 [3]	162	S_C0:7		NC_TEST	102	S_E2:1
	WR _CB4 [3]	161	S_C0:5		DM8	164	S_C2:4
	WR _CB3 [3]	49	S_D0:1		BA2	54	S_A0:0
	WR _CB2 [3]	48	S_ D0:6		NC_DQS8	46	S_A0:4
	WR _CB1 [3]	43	S_ D0:5				
	WR _CB0 [3]	42	S_ D1:2				

Table 1 – DDR2DC2A (400MT/s Read and Write) TLA Channel Grouping (cont'd)

Notes:

1. These signals are not required for data acquisition or post-processing data display
2. These signals are acquired using the TLA's demux capability and will not have a MagniVu display value

3.3 Display Groups not in Table 1

There are several groups in the List window that are not documented in the table as these groups are used only by the post-processing display software. To ensure correct data display these groups must not be modified. These groups are:

- DataHi
- DataLo
- DataMasks
- MRSAddr

4.0 CLOCK SELECTION

There are three clocking option fields available when using the support packages. These select fields permit the user to setup the TLA acquisition as follows:

SDRAM Clocking: – Permits selecting the DDR Clock to be used to acquire data. Also allows user to use only Chip Select S0# or Chip Selects S0# and S1# for acquisition. The field choices are:

DDR CK0; S0~ only active (default)
DDR CK0; S0~ & S1~ active
DDR CK1; S0~ only active
DDR CK1; S0~ & S1~ active

Clock Mode – Allows the user to choose the kind of data acquisition that will be made:

Selective Clocking (default) - This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS# or CAS# is asserted low along with S0# or S1#. After every assertion of CAS# (with either S0# or S1#) a samples are taken during the next 17 DDR Clock cycles to ensure that all valid memory cycles have been acquired, then acquisition pauses and waits for the next Command. If CAS# and a Chip Select are asserted during these 17 clock cycles the count is reset. The 17-clock cycle value was determined by adding the maximum Burst Length, CAS Latency, Additive Latency and Registered Delay values together to determine worst case delay from Command to the last cycle containing valid data.

Every SDRAM Clock Edge – As the name implies this will cause the acquisition card to store data on every Rising and Falling edge of the selected SDRAM clock.

Refresh Cycles: – Permits choosing whether Refresh Cycles will be stored or not. The field choices are:

Do Not Acquire (default) **–** This mode will reduce the number of Refresh cycles stored by the acquisition card to provide optimum use of the acquisition memory.

Acquire – Refresh Cycles will be stored.

5.0 CONFIGURING FOR READ / WRITE DATA ACQUISITION

IMPORTANT !

Prior to configuring your NEX-DDRII400DC support package it is ***strongly*** recommended that Appendix A ("How DDR Data is Clocked"), section 5.2 ("Selecting DDR Read Sample Points") and section 5.3 ("Selecting DDR Write Sample Points") be read. This background information is very helpful in properly configuring the support.

5.1 Adjusting Input Thresholds for Proper Data Acquisition

The voltage threshold must be properly set on the TLA for proper acquisition of the DDR bus.

IMPORTANT!
Because of the design of the adapter and probing interface the suggested threshold voltages for the TLA will be twice what they would be normally. This threshold voltage value (set to 1.89v as a default value) should be applied to the DDR Clock inputs as well as all of the other DDRII signals.

It is recommended that this be verified as correct by taking a TLA acquisition and verifying a 50% duty cycle on the clock by looking at the DDRCK0, DDRCK1 or DDRCK2 signals in a MagniVu trace.

5.2 Selecting DDRII Read Sample Points

For the NEX-DDRII400DC post-processing software packages to accurately show valid data it is necessary to choose the proper sample point to ensure that valid data is acquired when the software expects it. Since valid DDR2 Read data is straddled by the Strobes (see Figure 1) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Reads is determined by adding the Additive Latency value to the CAS Latency value, resulting in the total number of clock cycles from the Read Command to the first valid Read Data. (If these values are not known the technique described in Section 7.3 can be used to determine them.) In Figure 1 the total Read latency is 5 cycles.

DDR2DC2A support clocks data from both the rising and falling edge of the DDR2 clock, so only Sample Pt. #1 needs to be used to set the sample point for the RDDatHi/Lo groups.

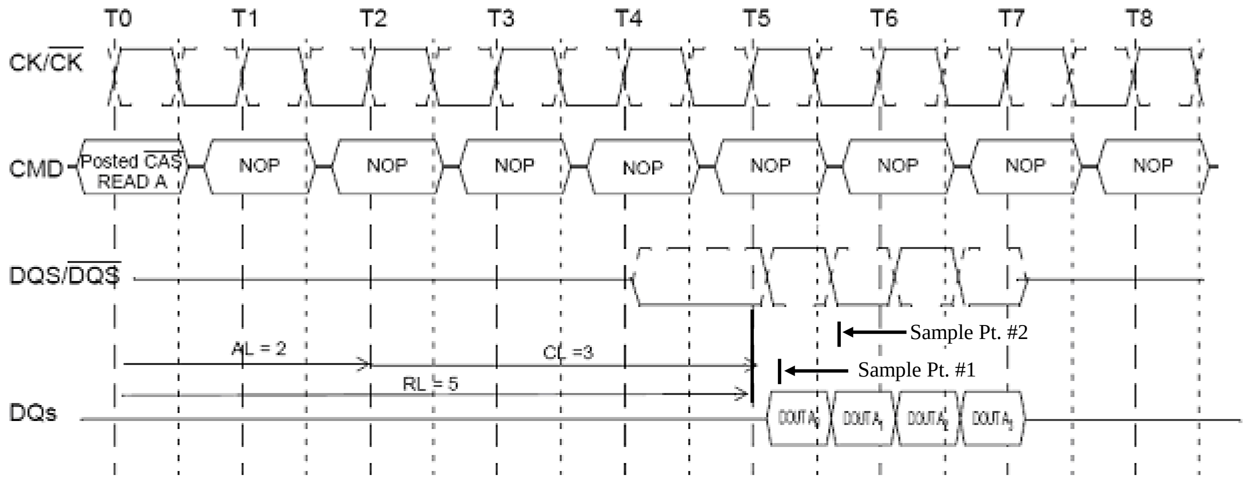


Figure 1- Read Cycle Latency = CAS Latency + Additive Latency (3+2=5 cycles)

5.3 Selecting DDRII Write Sample Points

Unlike valid DDR Read data, valid Write data is bisected by the Strobes. Since valid DDR2 Write data is bisected by the Strobes (see Figure 2) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Writes is determined by adding the Additive Latency value to the CAS Latency value and then subtracting one, resulting in the total number of clock cycles from the Write Command to the first valid Write Data. (If these values are not known the technique described in Section 7.3 can be used to determine them.) In Figure 2 the total Write latency is 4 cycles.

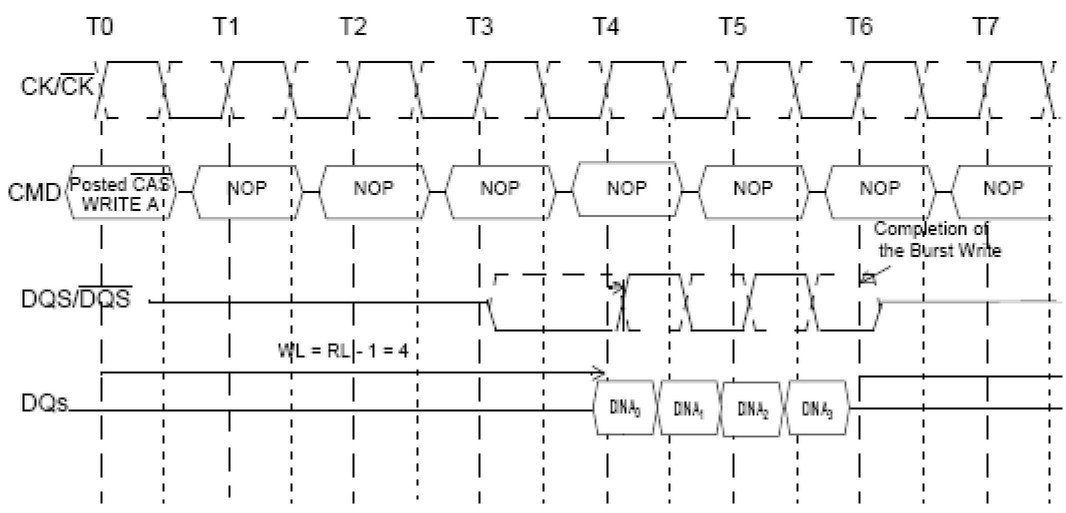


Figure 2- Write Cycle Latency = CAS Latency + Additive Latency-1 (3+2-1=4 cycles)

DDR2DC2A support clocks data from both the rising and falling edge of the DDR2 clock, so only Sample Pt. #1 needs to be used to set the sample point for the WRDatHi/Lo groups.

5.4 DDR2DC2A Support

The DDR2DC2A support will acquire both Read and Write data on DDR2 targets running at up to 400MT/s. It is necessary to program the sample windows for four 32-bit data groups because Read and Write data are acquired on both the rising and falling edges of the DDR Clock.

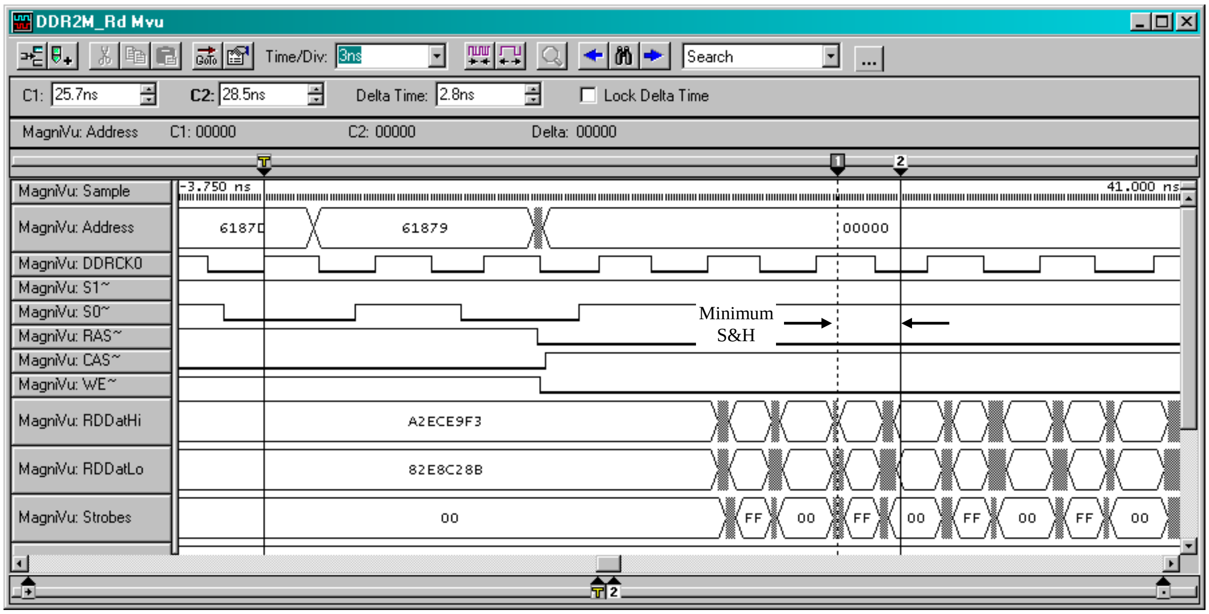


Figure 3- Locating Minimum Valid DDR2DC2A Read Data Window

To adjust the Read Data group sample points first make an appropriate acquisition of Read data by triggering on a Read Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0 or DDRCK1). A sample waveform display of MagniVu Read data is shown in Figure 3. To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (note arrows in Figure 3).

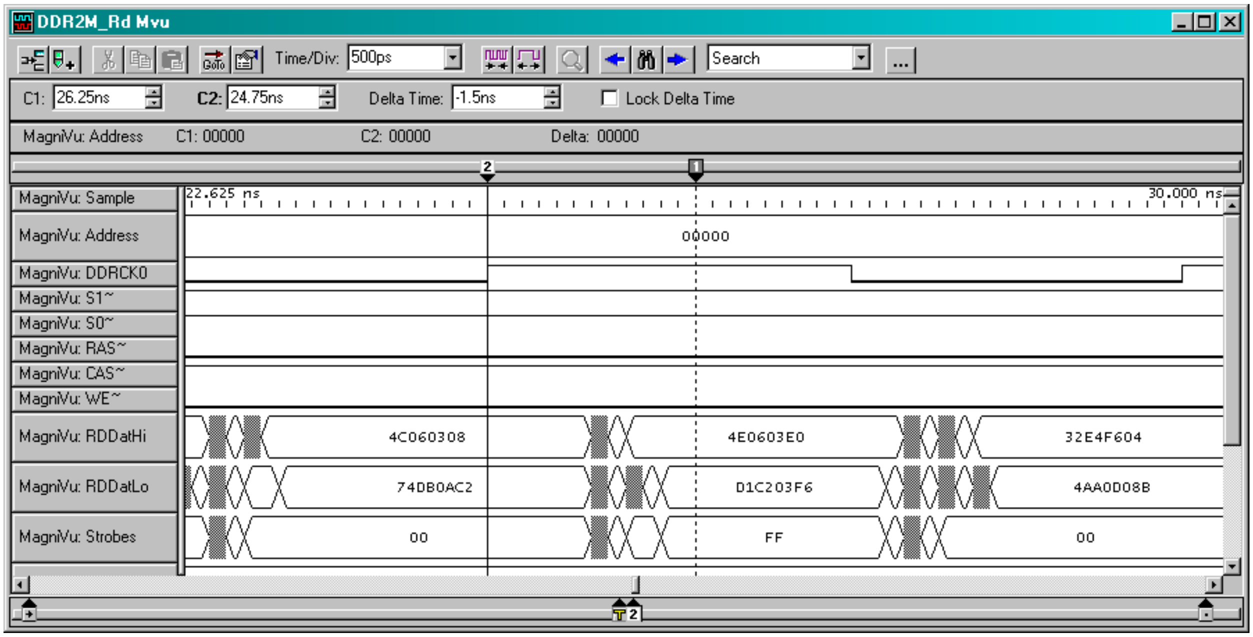


Figure 4- Measuring DDR2DC2A Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 4) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is ~1.5ns, meaning that a suitable Setup & Hold value would be –1.5ns/2.125ns. This sample point position must now be set for the RDDatHi and RDDatLo groups in the Setup window. This window is found by going to the LA Card's Setup window, then clicking on the **More** button to the right of the clock select field. The TLA acquisition cards require a valid data window of 625ps, and this window can be placed to begin from 16.25ns prior to the clock edge to 7.625ns after the edge in 125ps increments. Each 32-bit data group (RDDatHi and RDDataLo) will require its own value programmed from the measurements noted in the MagniVu window (Figure 5).

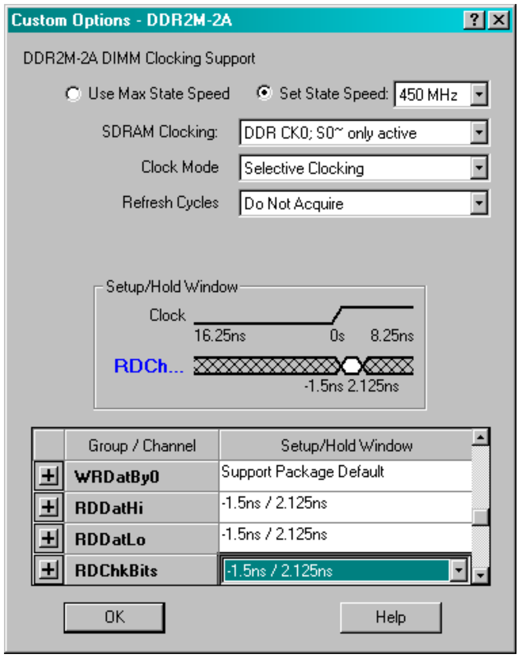


Figure 5- Setting DDR2DC2A Read Data Setup & Hold Sample Points

Setting the Setup & Hold values for acquiring Write data is similar, but the valid sample point now more closely aligns with the Strobe edges. To adjust the Write Data group sample points first make an appropriate acquisition of Write data by triggering on a Write Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0 or DDRCK1).

Note: Because of the method used to acquire Write Data using the DDR2DC2A support the MagniVu data from the RDDatHi/Lo data groups must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A “How DDR Data is Clocked”.

A sample waveform display of MagniVu Write data is shown in Figure 6. To determine the sample point, locate the worst-case Setup & Hold timing of valid Write data during the acquired burst (note arrows in Figure 6). Refer to section 5.3 for important information on properly determining the Write data sample points.

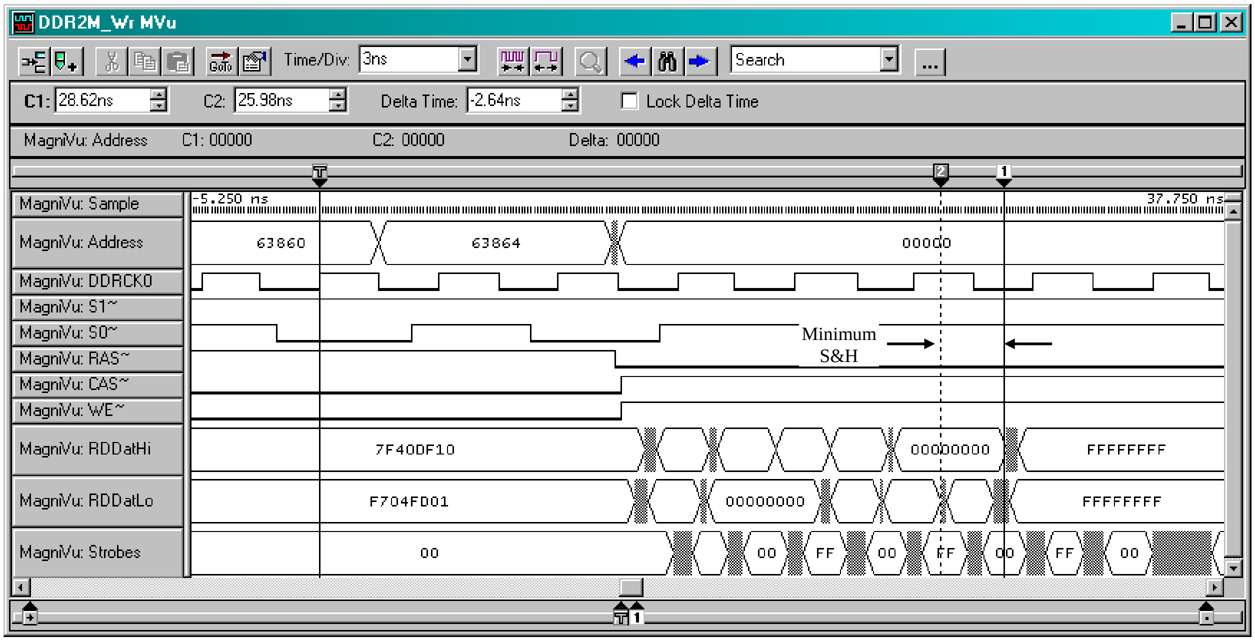


Figure 6- Locating Minimum Valid DDR2DC2A Write Data Window

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 7) and use the cursors to measure the time from the clock edge to the start of valid Write data. In this example the delay from edge to Strobe transition is ~1ns, meaning that a suitable Setup & Hold value would be 1ns/-375ps. This sample point position must now be set for the WRDatHi and WRDatLo groups in the Setup window (Figure 8). Note that the WrtMasks group should have a Setup & Hold value that aligns with the transition of the Strobes.

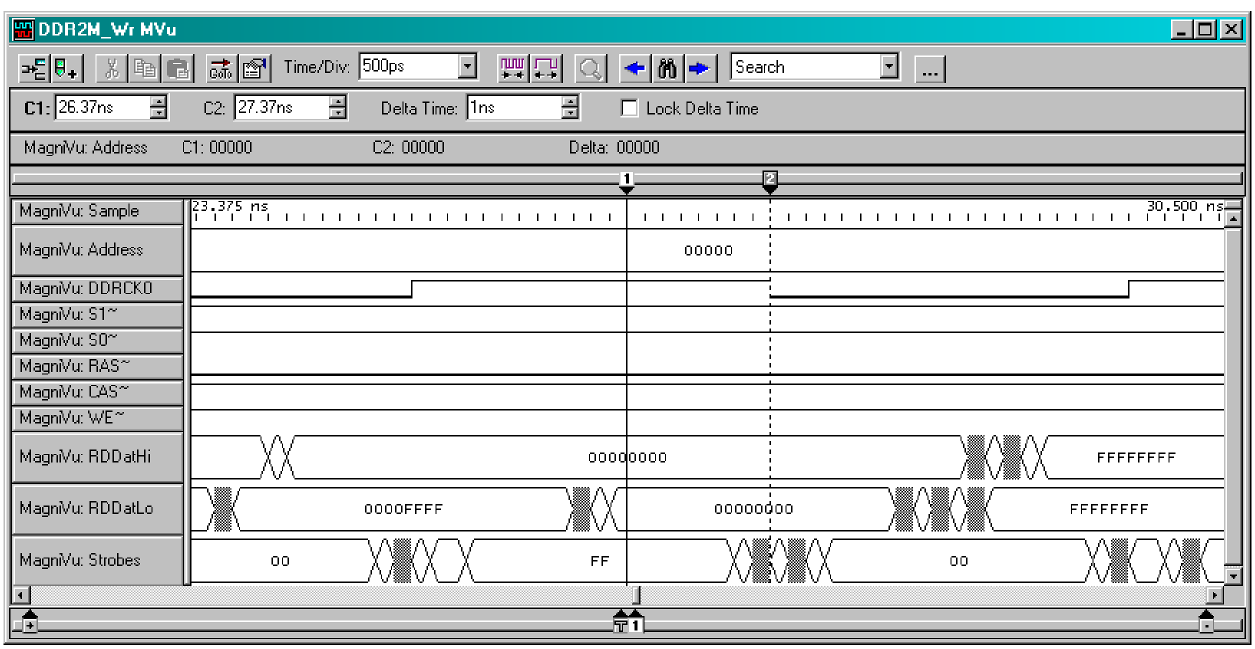


Figure 7- Measuring DDR2DC2A Write Data Setup & Hold

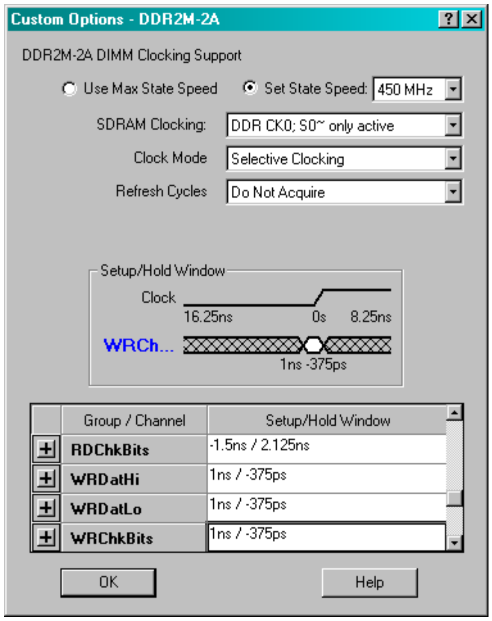


Figure 8- Setting DDR2DC2A Write Data Setup & Hold Sample Points

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 9 shows these added data groups (DatByte7-0) added to the same Waveform display shown in Figure 6. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see Figure 10). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit groups make up a 32-bit group.

Note: Again, it is very important to remember that, because of the method used to acquire Write Data using the DDR2DC2A support, the Read Data group information must be used to determine the Write Data sample points. For further explanation of this process refer to Appendix A "How DDR Data is Clocked".

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (RDDatHi, RDDatLo, WRDatHi or WRDatLo) be reset to "Support Package Default". This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values: 625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

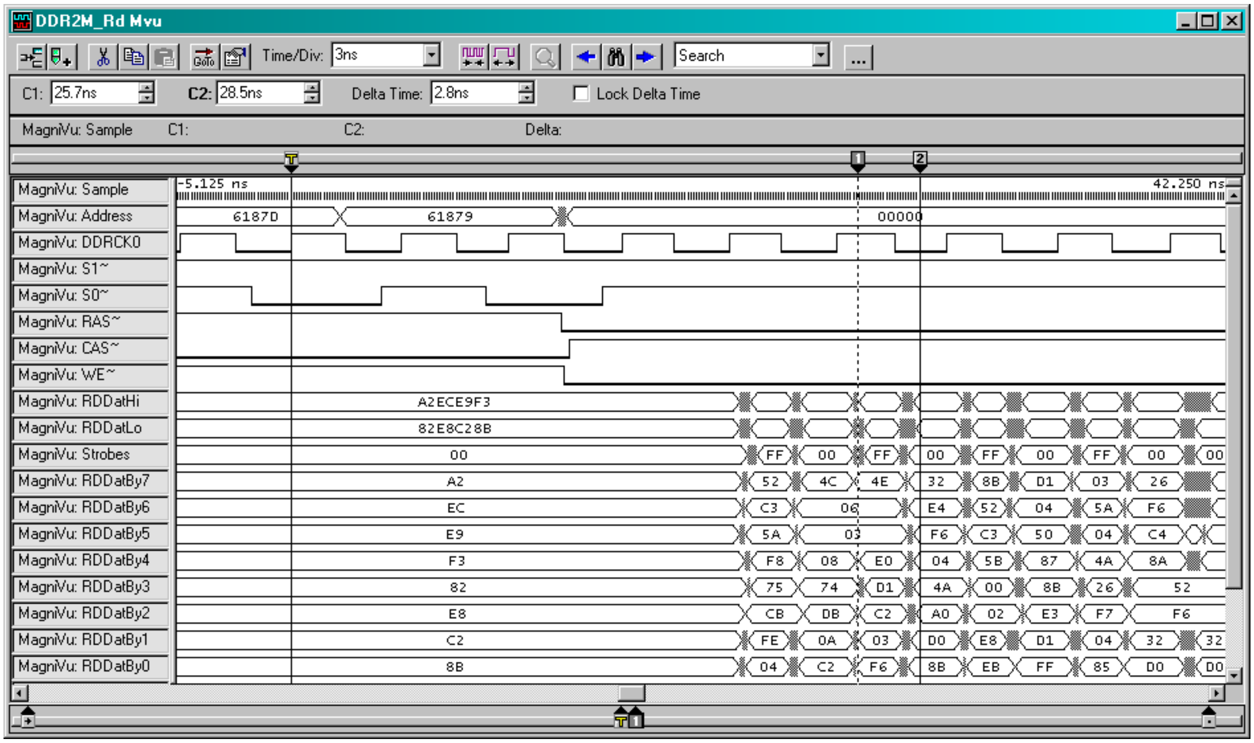


Figure 9- Viewing Individual 8-bit Read Data Groups

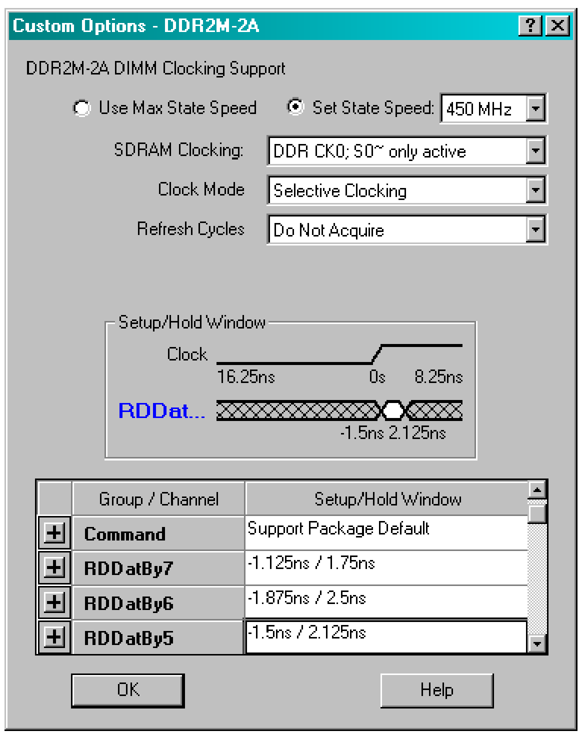


Figure 10- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

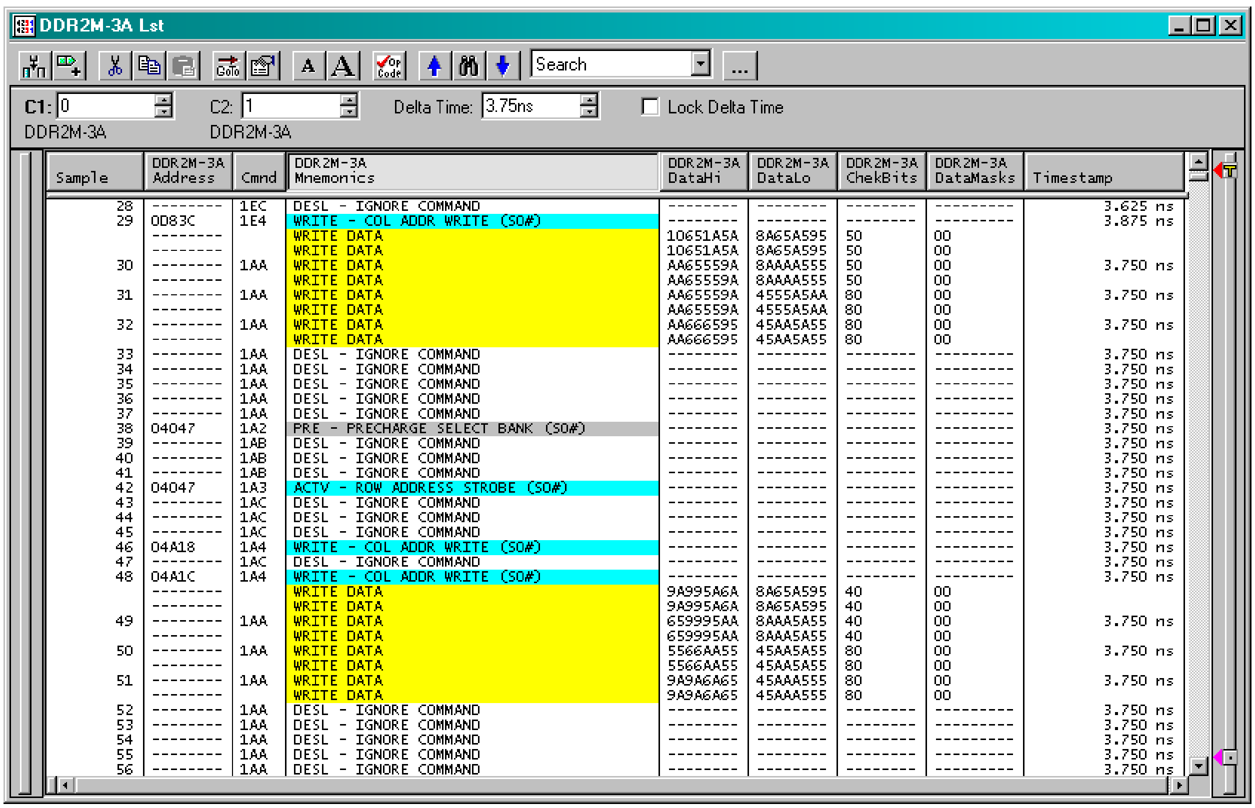
Note: Values shown are for illustration purposes only

6.0 VIEWING DATA

6.1 Viewing NEX-DDRII400DC Data

When using the NEX-DDRII400DC support packages the raw Address and Data groups are suppressed and are replaced with post-processed data in new groups. This data is displayed in new groups that have the support package name preceding it (i.e., DDR2DC2A Address, etc.). The raw data groups are suppressed so that the display of data can be done in a more user-friendly fashion.

The Command group is suppressed because its function is replaced with a column labeled “DDR2DC2A Mnemonics”. The NEX-DDRII400DC support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 11 shows the default display where all DDR data is displayed.



Sample	DDR2M-3A Address	Cmnd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChekBits	DDR2M-3A DataMasks	Timestamp
28	--------	1EC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.625 ns
29	0D83C	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	3.875 ns
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
30	--------	1AA	WRITE DATA	AA65559A	8AAAA555	50	00	3.750 ns
	--------		WRITE DATA	AA65559A	8AAAA555	50	00	
31	--------	1AA	WRITE DATA	AA65559A	4555A5AA	80	00	3.750 ns
	--------		WRITE DATA	AA65559A	4555A5AA	80	00	
32	--------	1AA	WRITE DATA	AA666595	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	AA666595	45AA5A55	80	00	
33	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
34	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
35	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
36	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
37	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
38	04047	1A2	PRE - PRECHARGE SELECT BANK (S0#)	--------	--------	--------	---------	3.750 ns
39	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
40	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
41	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
42	04047	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	3.750 ns
43	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
44	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
45	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	3.750 ns
47	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	3.750 ns
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
49	--------	1AA	WRITE DATA	659995AA	8AAA5A55	40	00	3.750 ns
	--------		WRITE DATA	659995AA	8AAA5A55	40	00	
50	--------	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	5566AA55	45AA5A55	80	00	
51	--------	1AA	WRITE DATA	9A9A6A65	45AAA555	80	00	3.750 ns
	--------		WRITE DATA	9A9A6A65	45AAA555	80	00	
52	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
53	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
54	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
55	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
56	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns

Figure 11- DDR2DC2A State Display

To change the display it is necessary to bring up the window’s Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in Figure 12.

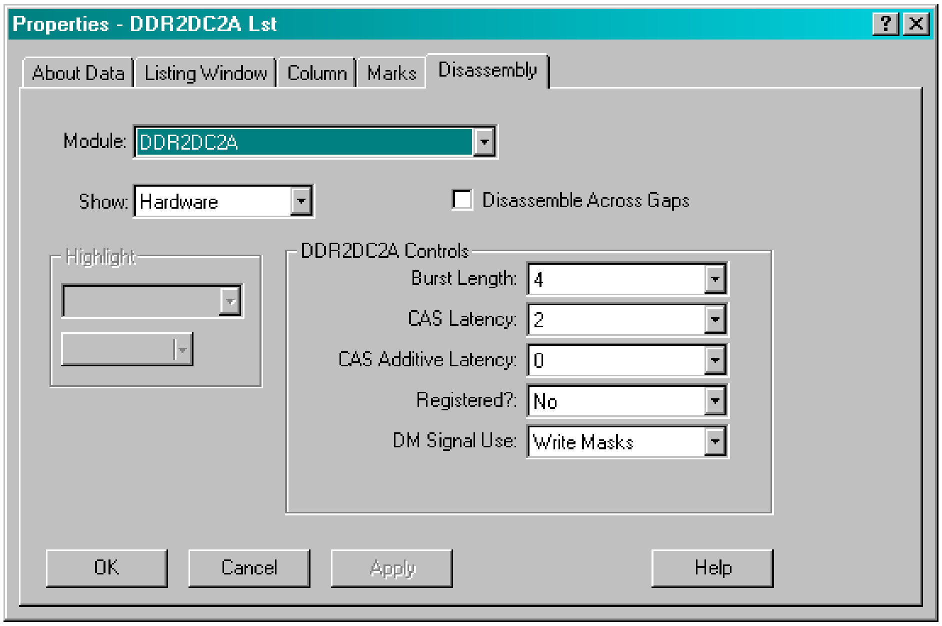


Figure 12- Disassembly Properties

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

Burst Length – permits setting the burst length for Read and Write data. Valid choices are 4 (the default) and 8. This value must be set properly for all valid Read and Write data to be displayed.

CAS Latency – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 2 (default), 3, 4, or 5 cycles.

CAS Additive Latency – additional latency for data cycles. This value must also be set properly for valid Read and Write Data to be displayed. Valid choices are 0 (default), 1, 2, 3, or 4 cycles.

Registered? – must be set to reflect whether or not Registered DDR memory is used. Default is No. When set to Yes an additional clock cycle delay is added to CAS Latency and to valid Read and Write Data tagging.

DM Signal Use – permits setting Data Mask functionality to Write Masks (default) or Strobes. When set to Write Mask the DM signals will be used to mask Write Data to show which data bytes were valid in the cycle.

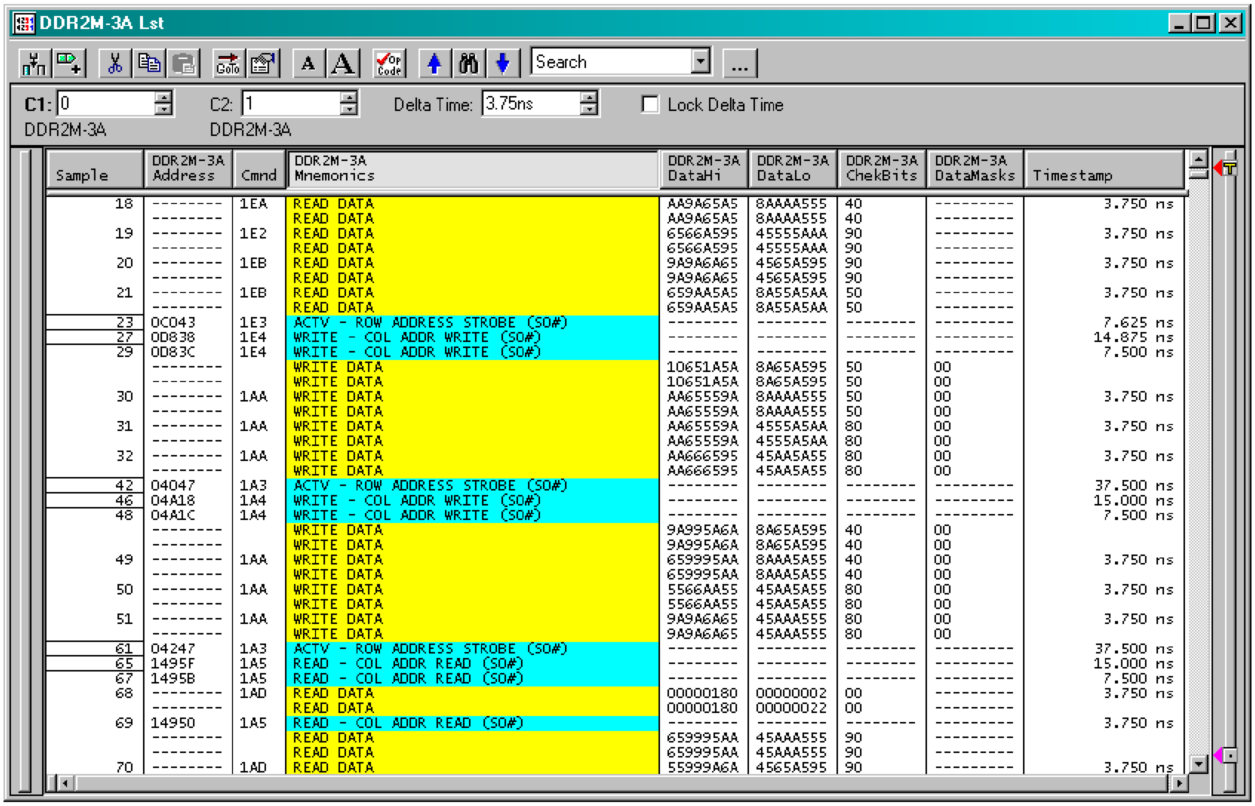
In addition to these Disassembly Properties selections, changing the settings in the **Show** field results in display changes as well:

Hardware – (default) displays all acquired cycles

Software – suppresses all idle or wait cycles

Control Flow – shows Address Command and valid Read / Write data cycles

Subroutine – shows valid Read / Write data cycles only



Sample	DDR2M-3A Address	Cmnd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChekBits	DDR2M-3A DataMasks	Timestamp
18	--------	1EA	READ DATA	AA9A65A5	8AAAA555	40	---------	3.750 ns
	--------		READ DATA	AA9A65A5	8AAAA555	40	---------	
19	--------	1E2	READ DATA	6566A595	45555AAA	90	---------	3.750 ns
	--------		READ DATA	6566A595	45555AAA	90	---------	
20	--------	1EB	READ DATA	9A9A6A65	4565A595	90	---------	3.750 ns
	--------		READ DATA	9A9A6A65	4565A595	90	---------	
21	--------	1EB	READ DATA	659AA5A5	8A55A5AA	50	---------	3.750 ns
	--------		READ DATA	659AA5A5	8A55A5AA	50	---------	
23	0C043	1E3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	7.625 ns
27	0D838	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	14.875 ns
29	0D83C	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	7.500 ns
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
30	--------	1AA	WRITE DATA	AA65559A	8AAAA555	50	00	3.750 ns
	--------		WRITE DATA	AA65559A	8AAAA555	50	00	
31	--------	1AA	WRITE DATA	AA65559A	4555A5AA	80	00	3.750 ns
	--------		WRITE DATA	AA65559A	4555A5AA	80	00	
32	--------	1AA	WRITE DATA	AA666595	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	AA666595	45AA5A55	80	00	
42	04047	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	37.500 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	15.000 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	7.500 ns
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
49	--------	1AA	WRITE DATA	659995AA	8AAA5A55	40	00	3.750 ns
	--------		WRITE DATA	659995AA	8AAA5A55	40	00	
50	--------	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	5566AA55	45AA5A55	80	00	
51	--------	1AA	WRITE DATA	9A9A6A65	45AAA555	80	00	3.750 ns
	--------		WRITE DATA	9A9A6A65	45AAA555	80	00	
61	04247	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	37.500 ns
65	1495F	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	15.000 ns
67	1495B	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	7.500 ns
68	--------	1AD	READ DATA	00000180	00000002	00	---------	3.750 ns
	--------		READ DATA	00000180	00000022	00	---------	
69	14950	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	3.750 ns
	--------		READ DATA	659995AA	45AAA555	90	---------	
	--------		READ DATA	659995AA	45AAA555	90	---------	
70	--------	1AD	READ DATA	55999A6A	4565A595	90	---------	3.750 ns

Figure 13- DDR2DC3A State Display - Control Flow

Changing the Show field setting in the display of Figure 11 from Hardware to Control Flow results in the display of Figure 13 where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

6.2 Viewing Raw DDR2 Data

In order to make the display of DDR2 data more user-friendly the raw data from the Address, all Data and other groups is suppressed in the Listing display. Instead the post-processing display software formats and reorders the data to tag and display valid DDR2 Address, Commands and Data.

To see the raw data using any of the NEX-DDRII400DC support packages perform a right mouse click in the Listing window, select **Add Column…** then click on the group to be added. Refer to the TLA User's Manual or online help for further information on added or deleting data groups.

6.3 DDR2DC2A Mnemonics Description

Table 2 gives a brief description of each of the text lines displayed in the post-processing software display.

Mnemonic	Description
ACTV - ROW ADDRESS STROBE (S0~)	Active command – activate a row in a bank for subsequent access (chip select 0)
ACTV - ROW ADDRESS STROBE (S1~)	Active command – activate a row in a bank for subsequent access (chip select 1)
BST - BURST STOP (S0~)	Burst Terminate command – truncate current Read burst (chip select 0)
BST - BURST STOP (S1~)	Burst Terminate command – truncate current Read burst (chip select 1)
DESL - IGNORE COMMAND	Deselect function – no new command
MRS - MODE REGISTER SET (S0~)	Mode Register Set command – mode register load (chip select 0)
MRS - MODE REGISTER SET (S1~)	Mode Register Set command – mode register load (chip select 1)
NOP - NO OPERATION (S0~)	No Operation command (chip select 0)
NOP - NO OPERATION (S1~)	No Operation command (chip select 1)
PRE - PRECHARGE SELECT BANK (S0~)	Precharge command (chip select 0)
PRE - PRECHARGE SELECT BANK (S1~)	Precharge command (chip select 1)
READ - COL ADDR READ (S0~)	Read command – initiates a burst read access to active row (chip select 0)
READ - COL ADDR READ (S1~)	Read command – initiates a burst read access to active row (chip select 1)
READ DATA	Valid Read data on the bus
REF - REFRESH (S0~)	Self Refresh command (chip select 0)
REF - REFRESH (S1~)	Self Refresh command (chip select 1)
WRITE - COL ADDR WRITE (S0~)	Write command – initiates a burst write access to active row (chip select 0)
WRITE - COL ADDR WRITE (S1~)	Write command – initiates a burst write access to active row (chip select 1)
WRITE DATA	Valid Write data on the bus
(UNKNOWN)	Command Cycle on falling edge of clock

Table 2- DDR2DC2A Mnemonics Definition

6.4 Viewing data at the output of Logic Analyzer Module scope outputs

A critical design goal of the NEX-DDRII400DC is to insure correct acquisition of State data with the logic analyzer. With this goal in mind the probe adapter front end was designed to present a comfortable voltage swing to the logic analyzer for acquisition. This provides margin for data acquisition. It is important to note that this causes the DDR data that is presented to an oscilloscope using the TLA Analog MUX capability to be increased in magnitude. The Analog MUX output of the TLA is twice the magnitude of the actual DDR signal. For example a DDR signal with a voltage swing of 0.5V-1.5V will be represented as a 1V-3V signal.

6.5 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: DDR2DC2A and DDR2DC2A: MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, DDR2DC2A: MagniVu, will show all of the channels in 8GHz MagniVu mode, so that edge relationships can be examined around the MagniVu trigger point. MagniVu is very useful and in some cases necessary to see/resolve DDR data. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

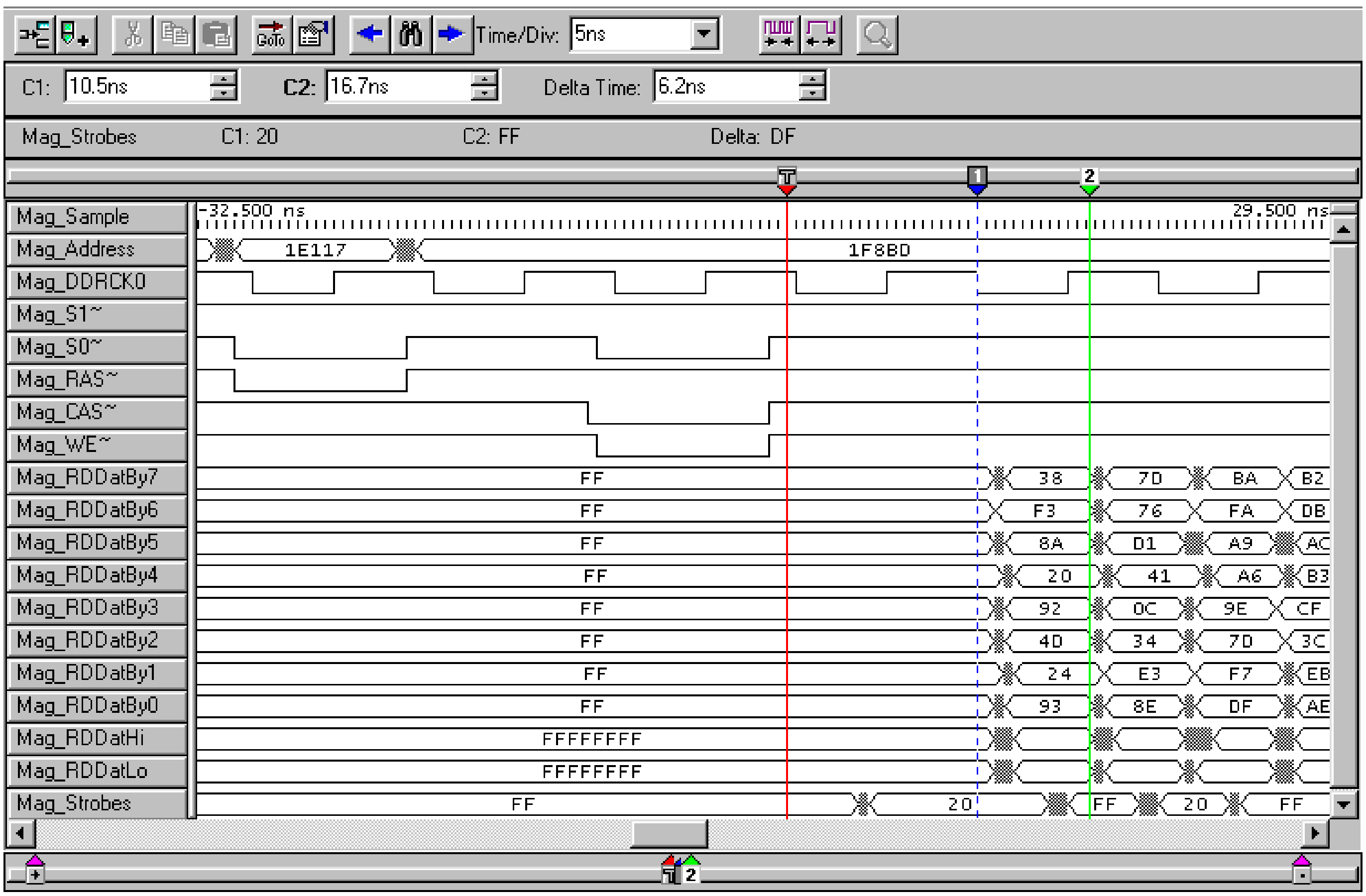


Figure 14- DDR2DC2A MagniVu Display on TLA

7.0 HINTS & TIPS

7.1 Symbolic Triggering on a Command using the NEX-DDRII400DC Supports

A Symbol Table has been included in the support packages for the Command data group (see Table 3). The use of Symbol Tables when triggering makes it easier for the user to define a given cycle to be triggered on. Rather than trying to remember what signals make up the Command group, the Symbol Table has the appropriate bits already set for the given cycle.

It is important to note that changing the group, channel, or wiring of the Command group can result in incorrect symbol information being displayed.

Symbol	Definition
DESL--IGNORE_COMMAND--DATA?	11 xxx
NOP--NO_OPERATION_(S0~)	x0 111
NOP--NO_OPERATION_(S1~)	0x 111
BST--BURST_STOP_(S0~)	x0 110
BST--BURST_STOP_(S1~)	0x 110
READ--COL_ADDR_READ_(S0~)	x0 101
READ--COL_ADDR_READ_(S1~)	0x 101
WRITE--COL_ADDR_WRITE_(S0~)	x0 100
WRITE--COL_ADDR_WRITE_(S1~)	0x 100
ACTV--ROW_ADDRESS_STROBE_(S0~)	x0 011
ACTV--ROW_ADDRESS_STROBE_(S1~)	0x 011
PRE--PRECHARGE_SELECT_BANK_(S0~)	x0 010
PRE--PRECHARGE_SELECT_BANK_(S1~)	0x 010
PALL--PRECHARGE_ALL_BANK_(S0~)	x0 010
PALL--PRECHARGE_ALL_BANK_(S1~)	0x 010
REF--REFRESH_(S0~)	x0 001
REF--REFRESH_(S1~)	0x 001
MRS--MODE_REGISTER_SET_(S0~)	x0 000
MRS--MODE_REGISTER_SET_(S1~)	0x 000

Table 3- DDR2DC2A Command Symbol Table
Signals, left-to-right: S1#, S0#, RAS#, CAS#, WE#

7.2 Triggering on a Command using the NEX-DDRII400DC Supports

The DDR2DC2A support package clocks data into the logic analyzer on both the rising and falling edges of the selected DDR Clock. Command information is only valid on the rising edge of the clock, but it is very possible (even likely) that valid information is also available on the falling edge of the clock preceding the Command's valid rising edge. This can result in a false trigger of the TLA. With the DDR2DC2A post-processing software such a cycle (falling edge of DDR Clock with valid Command data) is labeled as an Unknown cycle. These cycles would be filtered out (suppressed) when changing the Disassembly Properties display mode to something other than Hardware, resulting in a Trigger position that is hidden from the user.

To eliminate this problem it is suggested that a trigger condition be defined that ANDs the desired Command with the DDR Clock channel being used for acquisition in a LOW state (see Figure 15). (Since the data stored by the TLA reflects its state before the acquisition clock occurs the DDR Clock is stored as a LOW for a rising clock edge and as a HIGH for a falling clock edge.) Figure 16 shows the actual Trigger Clause definition used in the trigger program shown in Figure 15.

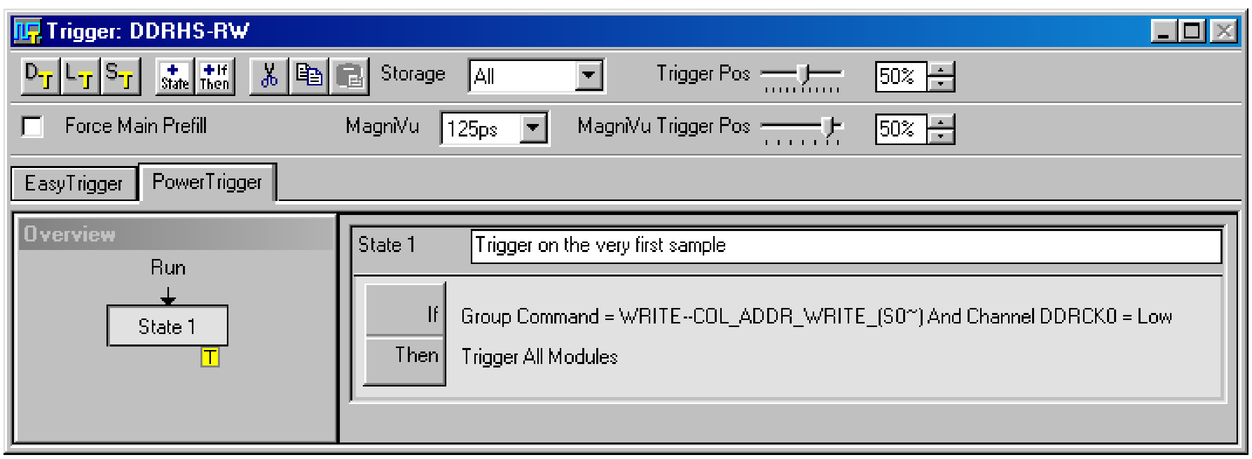


Figure 15- Recommended DDR2DC2A Command Trigger

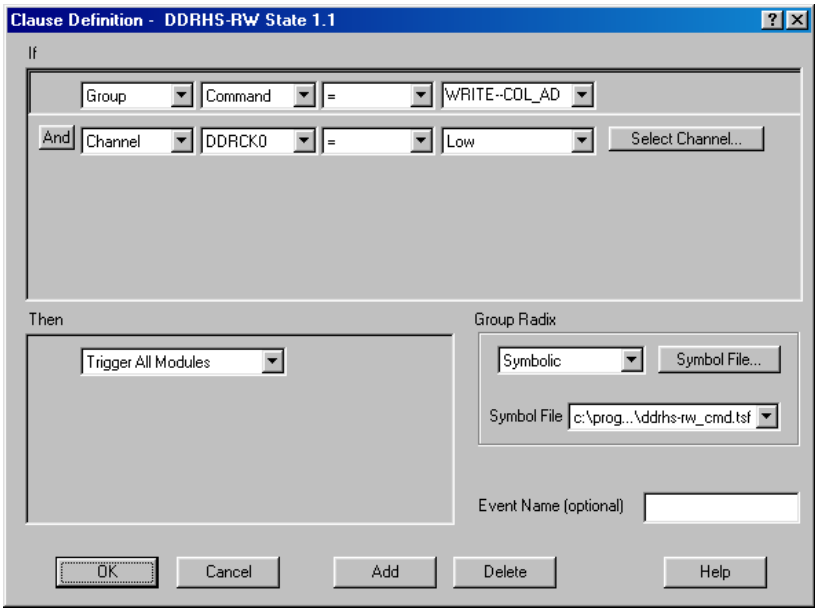


Figure 16- Recommended DDR2DC2A Command Trigger - Detail

7.3 Capturing MRS (Mode Register Set) Data

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the NEX-DDRII400DC supports for the post-processing software to properly decode the acquisitions. The TLA trigger shown in Figure 17 can be used to acquire the MRS cycles when using either of these supports.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

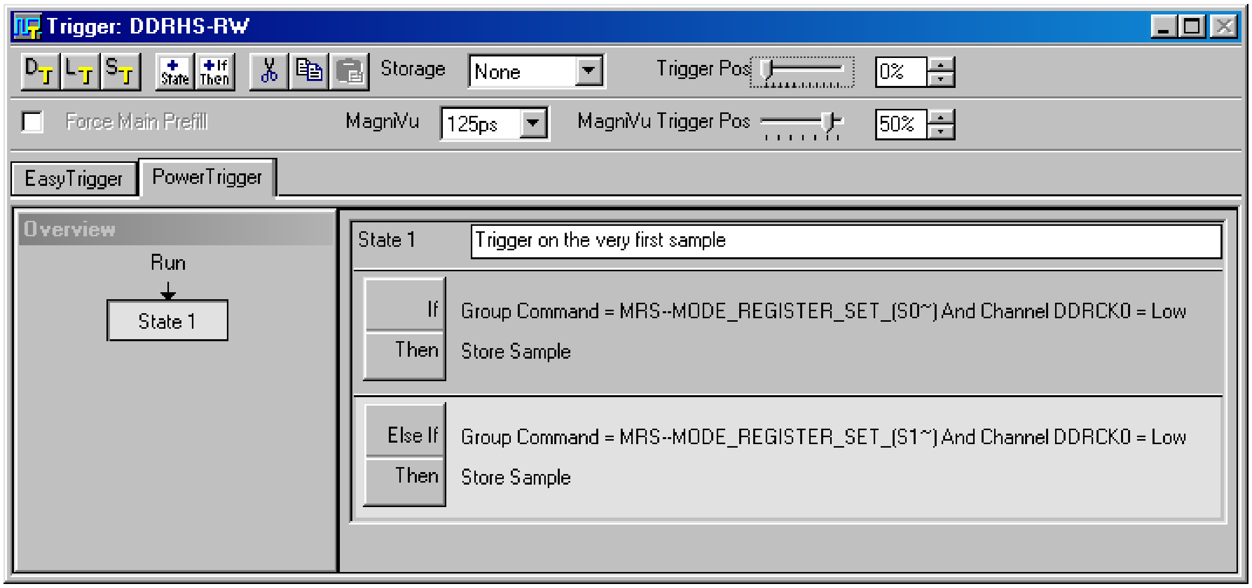


Figure 17- DDR2DC2A MRS Trigger

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in Figure 18. The last acquired MRS cycle will reflect the settings used in the DDR target – in this case, a CAS latency of 2 cycles with a Burst length of 8.

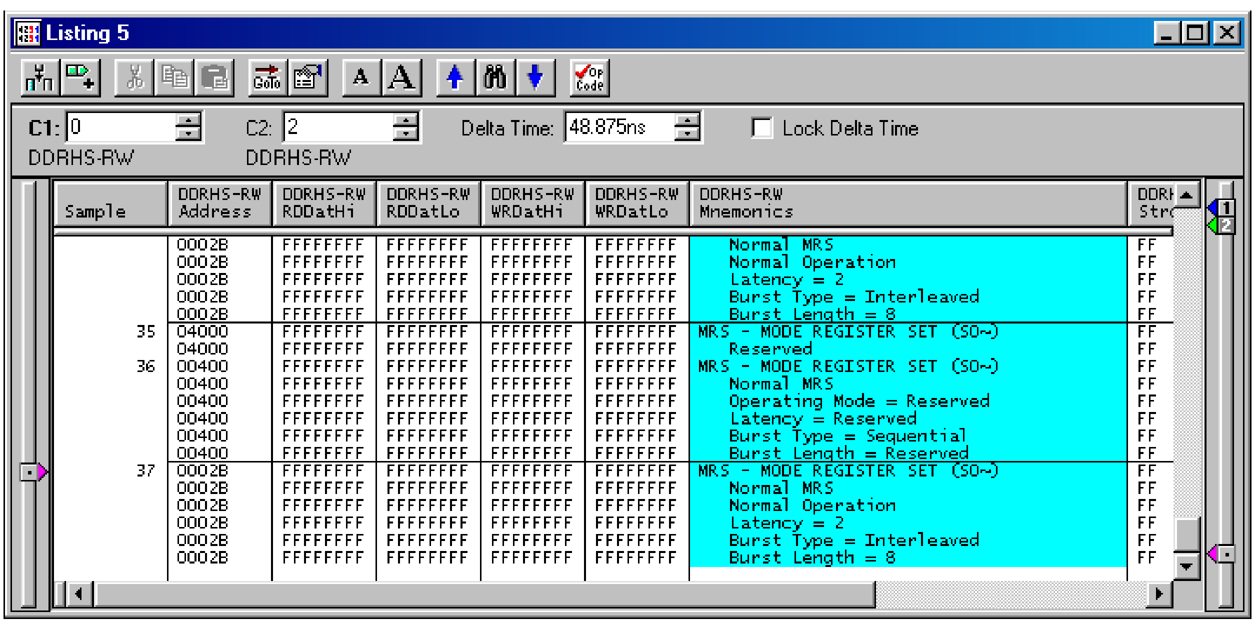


Figure 18- MRS Cycle Acquisition Disassembly

APPENDIX A - How DDR Data is Clocked

A.1 Background

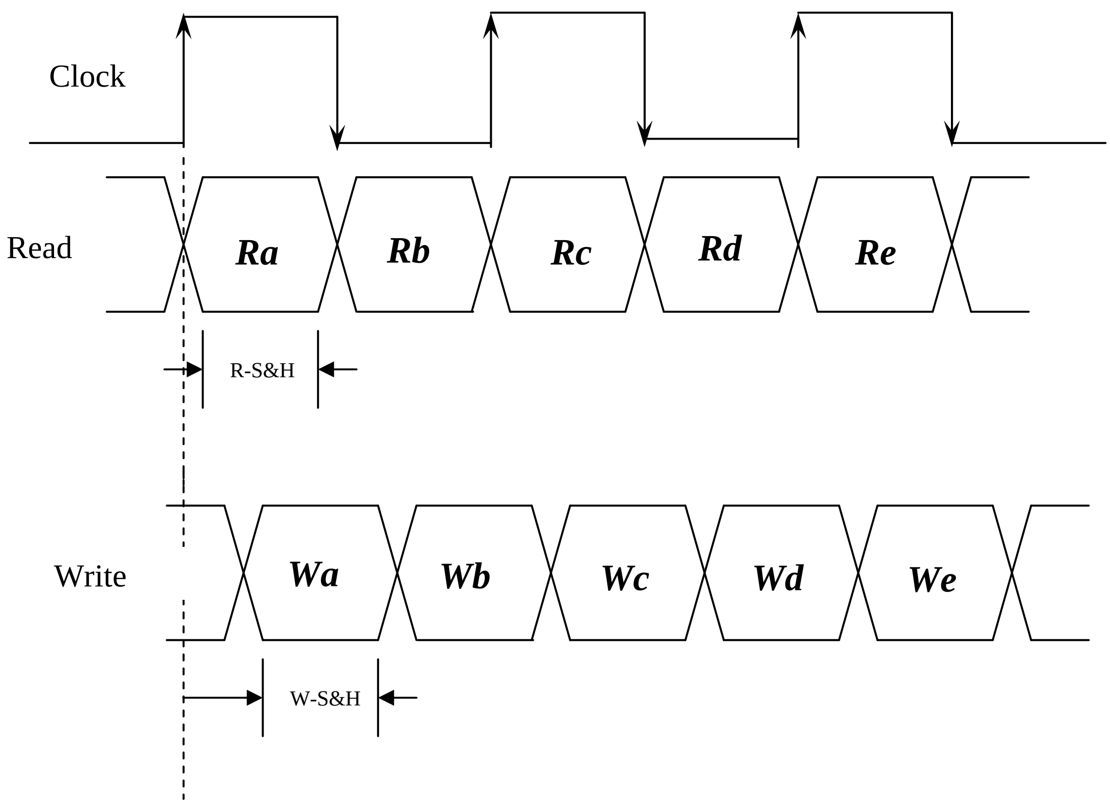
Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two or four separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section ***and*** the D3 section. Using 4X demux, connections made to the A3 channels permit data to be stored in the A3, A2, D3 and D2 sections. A very useful side benefit of using demux is that, since only one set of TLA data channels has to be connected, only one probe load is added to the target, even though data is stored in two or four different locations of the acquisition card.

A.2 DDR Acquisition - General

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. In addition, instead of trying to use the 8 Data Strobes to acquire data our solution uses one of the DDR SDRAM Clocks (either CK0 or CK1, user selectable) and all data acquisition is adjusted in relation to the clock edges. The 8 Data Strobes cannot be easily used to acquire data as some TLA configurations only support 4 Clock Inputs. Also, the Strobes cannot be used to acquire Address and Command information.

A.3 DDR2DC2A Support

This support requires two (2) merged 136-channel 450MHz TLA7Ax4 acquisition cards used in a TLA7XX. The merged cards enable 400MT/s Read and Write data to be acquired simultaneously from a DDR system. Data is acquired using both edges of the DDR clock, and 2X demultiplexing is done to permit acquiring both Read and Write data on every clock edge. One Sample Point must be set to acquire valid Read data in reference to the clock edge; a second Sample Point must be set to acquire valid Write data in relation to that edge. Again, different Sample Points must be set for each of the Read / Write data groups, and if necessary, sample points can be set for any of the 8-bit data groups.



APPENDIX B - Considerations

B.1 NEX-DDRII400DC Bus Loading

It must be noted that the NEX-DDRII400DC Bus Adapter does not provide any buffering of the DDR memory signals. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using this adapter, to see the exact timing relationships and signal waveforms from the system. It is important to note that the NEX- DDRII400DC is an impedance controlled, matched trace length design. This adds greatly to its ability to maintain signal integrity and timing relationships of the DDR bus.

APPENDIX C - DDRII DIMM 240-pin Pinout

Front Side (left 1-60)			Back Side (right 121-180)			Front Side (left 61-120)			Back Side (right 181-240)		
Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC
1	VREF	VREF	121	VSS	VSS	61	A4	A4	181	VDDQ	VDDQ
2	VSS	VSS	122	DQ4	DQ4	62	VDDQ	VDDQ	182	A3	A3
3	DQ0	DQ0	123	DQ5	DQ5	63	A2	A2	183	A1	A1
4	DQ1	DQ1	124	VSS	VSS	64	VDD	VDD	184	VDD	VDD
5	VSS	VSS	125	DM0 DQS9	DM0 DQS9	KEY			KEY		
6	DQS0#	DQS0#	126	NC DQS9#	NC DQS9#	65	VSS	VSS	185	CK0	CK0
7	DQS0	DQS0	127	VSS	VSS	66	VSS	VSS	186	CK0#	CK0#
8	VSS	VSS	128	DQ6	DQ6	67	VDD	VDD	187	VDD	VDD
9	DQ2	DQ2	129	DQ7	DQ7	68	NC	NC	188	A0	A0
10	DQ3	DQ3	130	VSS	VSS	69	VDD	VDD	189	VDD	VDD
11	VSS	VSS	131	DQ12	DQ12	70	A10/AP	A10/AP	190	BA1	BA1
12	DQ8	DQ8	132	DQ13	DQ13	71	BA0	BA0	191	VDDQ	VDDQ
13	DQ9	DQ9	133	VSS	VSS	72	VDDQ	VDDQ	192	RAS#	RAS#
14	VSS	VSS	134	DM1 DQS10	DM1 DQS10	73	WE#	WE#	193	S0#	S0#
15	DQS1#	DQS1#	135	NC DQS10#	NC DQS10#	74	CAS#	CAS#	194	VDDQ	VDDQ
16	DQS1	DQS1	136	VSS	VSS	75	VDDQ	VDDQ	195	ODT0	ODT0
17	VSS	VSS	137	CK1,RFU	CK1,RFU	76	S1#	S1#	196	A13	A13
18	RC1	RC1	138	CK1#,RFU	CK1#,RFU	77	ODT1	ODT1	197	VDD	VDD
19	NC	NC	139	VSS	VSS	78	VDDQ	VDDQ	198	VSS	VSS
20	VSS	VSS	140	DQ14	DQ14	79	VSS	VSS	199	DQ36	DQ36
21	DQ10	DQ10	141	DQ15	DQ15	80	DQ32	DQ32	200	DQ37	DQ37
22	DQ11	DQ11	142	VSS	VSS	81	DQ33	DQ33	201	VSS	VSS
23	VSS	VSS	143	DQ20	DQ20	82	VSS	VSS	202	DM4 DQS13	DM4 DQS13
24	DQ16	DQ16	144	DQ21	DQ21	83	DQS4#	DQS4#	203	NC DQS13#	NC DQS13#
25	DQ17	DQ17	145	VSS	VSS	84	DQS4	DQS4	204	VSS	VSS
26	VSS	VSS	146	DM2 DQS11	DM2 DQS11	85	VSS	VSS	205	DQ38	DQ38
27	DQS2#	DQS2#	147	NC DQS11#	NC DQS11#	86	DQ34	DQ34	206	DQ39	DQ39
28	DQS2	DQS2	148	VSS	VSS	87	DQ35	DQ35	207	VSS	VSS
29	VSS	VSS	149	DQ22	DQ22	88	VSS	VSS	208	DQ44	DQ44
30	DQ18	DQ18	150	DQ23	DQ23	89	DQ40	DQ40	209	DQ45	DQ45
31	DQ19	DQ19	151	VSS	VSS	90	DQ41	DQ41	210	VSS	VSS
32	VSS	VSS	152	DQ28	DQ28	91	VSS	VSS	211	DM5 DQS14	DM5 DQS14
33	DQ24	DQ24	153	DQ29	DQ29	92	DQS5#	DQS5#	212	NC DQS14#	NC DQS14#
34	DQ25	DQ25	154	VSS	VSS	93	DQS5	DQS5	213	VSS	VSS
35	VSS	VSS	155	DM3 DQS12	DM3 DQS12	94	VSS	VSS	214	DQ46	DQ46
36	DQS3#	DQS3#	156	NC DQS12#	NC DQS12#	95	DQ42	DQ42	215	DQ47	DQ47
37	DQS3	DQS3	157	VSS	VSS	96	DQ43	DQ43	216	VSS	VSS
38	VSS	VSS	158	DQ30	DQ30	97	VSS	VSS	217	DQ52	DQ52
39	DQ26	DQ26	159	DQ31	DQ31	98	DQ48	DQ48	218	DQ53	DQ53
40	DQ27	DQ27	160	VSS	VSS	99	DQ49	DQ49	219	VSS	VSS

NC = No Connect; NU = Not Useable; RFU = Reserved Future Use

APPENDIX C - DDRII DIMM 240-pin Pinout (cont'd.)

Front Side (left 1-60)			Back Side (right 121-180			Front Side (left 61-120)			Back Side (right 181-240)		
Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC
41	VSS	VSS	161	NC	CB4	100	VSS	VSS	220	CK2 RFU	CK2 RFU
42	NC	CB0	162	NC	CN5	101	SA2	SA2	221	CK2# RFU	CK2# RFU
43	NC	CB1	163	VSS	VSS	102	NC TEST	NC TEST	222	VSS	VSS
44	VSS	VSS	164	NC	DM8 DQS17	103	VSS	VSS	223	DM6 DQS15	DM6 DQS15
45	NC	DQS8#	165	NC	NC DQS17#	104	DQS6#	DQS6#	224	NC DQS15#	NC DQS15#
46	NC	DQS8	166	VSS	VSS	105	DQS6	DQS6	225	VSS	VSS
47	VSS	VSS	167	NC	CB6	106	VSS	VSS	226	DQ54	DQ54
48	NC	CB2	168	NC	CB7	107	DQ50	DQ50	227	DQ55	DQ55
49	NC	CB3	169	VSS	VSS	108	DQ51	DQ51	228	VSS	VSS
50	VSS	VSS	170	VDDQ	VDDQ	109	VSS	VSS	229	DQ60	DQ60
51	VDDQ	VDDQ	171	CKE1	CKE1	110	DQ56	DQ56	230	DQ61	DQ61
52	CKE0	CKE0	172	VDD	VDD	111	DQ57	DQ57	231	VSS	VSS
53	VDD	VDD	173	A15	A15	112	VSS	VSS	232	DM7 DQS16	DM7 DQS16
54	A16,BA2	A16,BA2	174	A14	A14	113	DQS7#	DQS7#	233	NC DQS16#	NC DQS16#
55	RC0	RC0	175	VDDQ	VDDQ	114	DQS7	DQS7	234	VSS	VSS
56	VDDQ	VDDQ	176	A12	A12	115	VSS	VSS	235	DQ62	DQ62
57	A11	A11	177	A9	A9	116	DQ58	DQ58	236	DQ63	DQ63
58	A7	A7	178	VDD	VDD	117	DQ59	DQ59	237	VSS	VSS
59	VDD	VDD	179	A8	A8	118	VSS	VSS	238	VDDSPD	VDDSPD
60	A5	A5	180	A6	A6	119	SDA	SDA	239	SA0	SA0
						120	SCL	SCL	240	SA1	SA1

NC = No Connect; NU = Not Useable; RFU = Reserved Future Use

APPENDIX D - NEX-DDRII400DC Coax Cable Pinouts

Refer to the Silkscreen front and back in Appendix E for the location of the Coax cables. P100 pins 1-120 indicate the front side.

Coax #	Samtec #	TLA Channel	DDR Signal
2	50	A3:5	DQ4
3	49	A3:7	DQ5
4	54	A3:4	DM0_DQS9
5	53	A3:6	NC_DQS9#
6	58	A3:1	DQ6
7	57	A3:3	DQ7
8	62	A3:0	DQ12
9	46	CK0+	CLK1
10	61	A3:2	DQ13
11	66	A2:5	DM1_DQS10
12	65	A2:7	NC_DQS10#
13	70	A2:4	DQ14
14	69	A2:6	DQ15
15	74	A2:1	DQ20
16	73	A2:3	DQ21
17	78	A2:0	DM2_DQS11
18	77	A2:2	NC_DQS11#

Coax Cable Connection
M - A3 /A2

Coax #	Samtec #	TLA Channel	DDR Signal
2	50	A1:5	DQ36
3	49	A1:7	DQ37
4	54	A1:4	DM4_DQS13
5	53	A1:6	NC_DQS13#
6	58	A1:1	DQ38
7	57	A1:3	DQ39
8	62	A1:0	DQ44
9	46	CK1+	CK2+
10	61	A1:2	DQ45
11	66	A0:5	DM5_DQS14
12	65	A0:7	NC_DQS14#
13	70	A0:4	DQ46
14	69	A0:6	DQ47
15	74	A0:1	DQ52
16	73	A0:3	DQ53
17	78	A0:0	GND
18	77	A0:2	GND

Coax Cable Connection
M - A1 / A0

Coax #	Samtec #	TLA Channel	DDR Signal
2	3	C0:0	A14
3	7	C0:1	A12
4	11	C0:4	A9
5	15	C0:5	A8
6	19	C1:0	A6
7	23	C1:1	A3
8	27	C1:4	A1
9	31	C1:5	GND
10	46	CK3+	CK0+
11	49	C3:7	A0
12	53	C3:6	BA1
13	57	C3:3	GND
14	61	C3:2	GND
15	65	C2:7	ODT0
16	69	C2:6	A13
17	73	C2:3	RAS#
18	77	C2:2	S0#

Coax Cable Connection
M_C Back (Interposer)
(Front of Paddle board)

Coax #	Samtec #	TLA Channel	DDR Signal
2	4	C0:2	A11
3	8	C0:3	A7
4	12	C0:6	A5
5	16	C0:7	A4
6	20	C1:2	A2
7	24	C1:3	A10/AP
8	28	C1:6	BA0
9	32	C1:7	GND
10	35	Q1+	WE#
11	50	C3:5	GND
12	54	C3:4	ODT1
13	58	C3:1	GND
14	62	C3:0	GND
15	66	C2:5	DQS4#
16	70	C2:4	DQS4
17	74	C2:1	CAS#
18	78	C2:0	S1#

Coax Cable Connection
M_C Front (Interposer)
(Back of Paddle board)

APPENDIX D - NEX-DDRII400DC Coax Cable Pinouts (cont'd.)

Refer to the Silkscreen front and back in Appendix E for the location of the Coax cables. P100 pins 1-120 indicate the front side.

Coax #	Samtec #	TLA Channel	DDR Signal
2	3	E0:0	DQ54
3	7	E0:1	DM6_DQS15
4	11	E0:4	NC_DQS15#
5	15	E0:5	DQ55
6	19	E1:0	DQ60
7	23	E1:1	DQ61
8	27	E1:4	GND
9	31	E1:5	GND
10	46	Q3+	DM7_DQS16
11	49	E3:7	NC_DQS16#
12	53	E3:6	DQ62
13	57	E3:3	DQ63
14	61	E3:2	SA0
15	65	E2:7	SA1
16	69	E2:6	GND
17	73	E2:3	GND
18	77	E2:2	GND

Coax Cable Connection
M_E Back (Interposer)
(Front of Paddle board)

Coax #	Samtec #	TLA Channel	DDR Signal
2	4	E0:2	DQ51
3	8	E0:3	DQ56
4	12	E0:6	DQ57
5	16	E0:7	DQS7#
6	20	E1:2	DQS7
7	24	E1:3	GND
8	28	E1:6	GND
9	32	E1:7	GND
10	35	Q2+	GND
11	50	E3:5	DQ58
12	54	E3:4	DQ59
13	58	E3:1	GND
14	62	E3:0	GND
15	66	E2:5	GND
16	70	E2:4	SDA
17	74	E2:1	SCL
18	78	E2:0	GND

Coax Cable Connection
M_E Front (Interposer)
(Back of Paddle board)

APPENDIX D - NEX-DDRII400DC Coax Cable Pinouts (cont'd.)

Refer to the Silkscreen front and back in Appendix E for the location of the Coax cables. P100 pins 1-120 indicate the front side.

Coax #	Samtec #	TLA Channel	DDR Signal
2	50	E3:5	DQ32
3	49	E3:7	DQ33
4	54	E3:4	DQ34
5	53	E3:6	DQ35
6	58	E3:1	DQ40
7	57	E3:3	DQ41
8	62	E3:0	DQS5#
9	46	Q3+	DQS5
10	61	E3:2	DQ42
11	66	E2:5	DQ43
12	65	E2:7	DQ48
13	70	E2:4	DQ49
14	69	E2:6	SA2
15	74	E2:1	NC_TEST
16	73	E2:3	DQS6#
17	78	E2:0	DQS6
18	77	E2:2	DQ50

Coax Cable Connection
S – E2 / E3

Coax #	Samtec #	TLA Channel	DDR Signal
2	50	A3:5	DQ0
3	49	A3:7	DQ1
4	54	A3:4	DQS0#
5	53	A3:6	DQS0
6	58	A3:1	DQ2
7	57	A3:3	DQ3
8	62	A3:0	DQ8
9	46	CK0+	DQ9
10	61	A3:2	DQS1#
11	66	A2:5	DQS1
12	65	A2:7	RC1
13	70	A2:4	DQ10
14	69	A2:6	DQ11
15	74	A2:1	DQ16
16	73	A2:3	DQ17
17	78	A2:0	DQS2#
18	77	A2:2	DQS2

Coax Cable Connection
S – A2 / A3

Coax #	Samtec #	TLA Channel	DDR Signal
2	50	A1:5	DQ18
3	49	A1:7	DQ19
4	54	A1:4	DQ24
5	53	A1:6	DQ25
6	58	A1:1	DQS3#
7	57	A1:3	DQS3
8	62	A1:0	DQ26
9	46	CK1+	DQ27
10	61	A1:2	CB0
11	66	A0:5	CB1
12	65	A0:7	DQS8#
13	70	A0:4	DQS8
14	69	A0:6	CB2
15	74	A0:1	CB3
16	73	A0:3	CKE0
17	78	A0:0	A16_BA2
18	77	A0:2	RC0

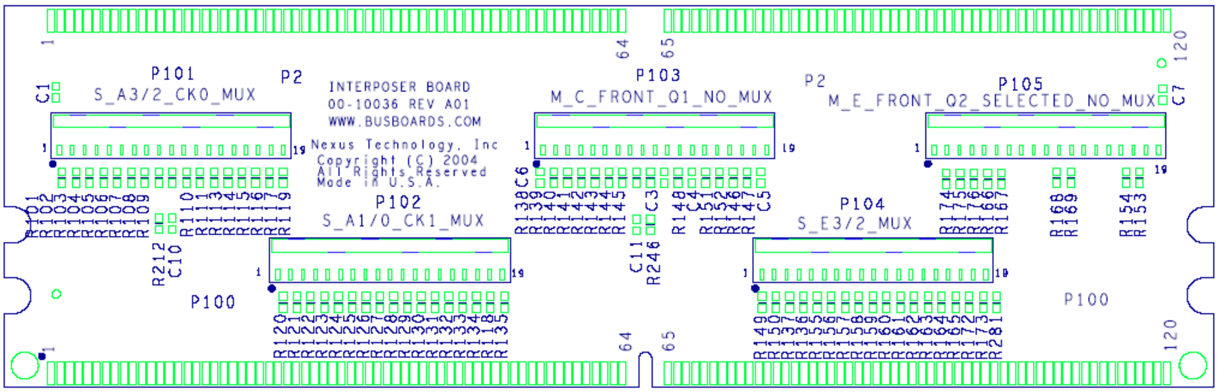
Coax Cable Connection
S – A0/A1

Coax #	Samtec #	TLA Channel	DDR Signal
2	50	C3:5	GND
3	49	C3:7	DQ22
4	54	C3:4	DQ23
5	53	C3:6	DQ28
6	58	C3:1	DQ29
7	57	C3:3	DM3_DQS12
8	62	C3:0	NC_DQS12#
9	46	CK3+	DQ30
10	61	C3:2	DQ31
11	66	C2:5	CB4
12	65	C2:7	CB5
13	70	C2:4	DM8_DQS17
14	69	C2:6	NC_DQS17#
15	74	C2:1	CB6
16	73	C2:3	CB7
17	78	C2:0	CKE1
18	77	C2:2	A15

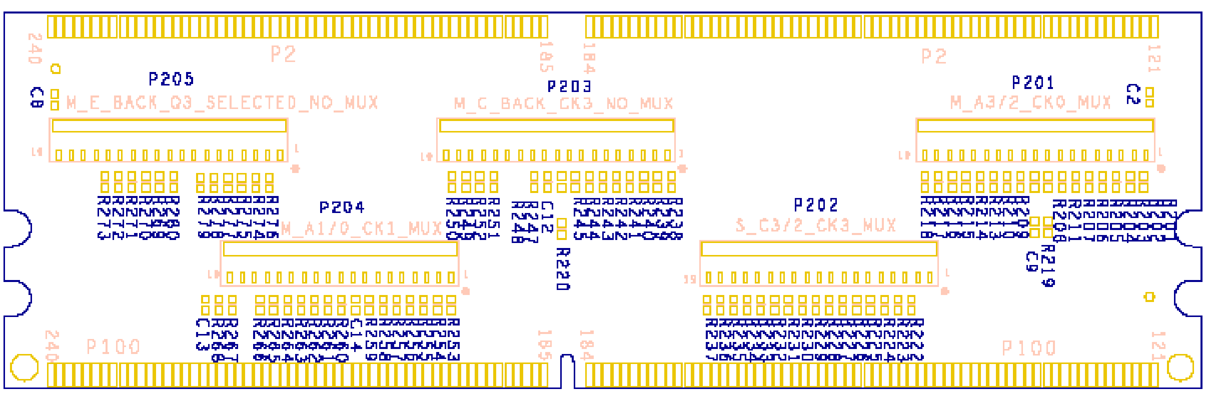
Coax Cable Connection
S – C2/C3

APPENDIX E – NEX-DDRII400DC Silkscreen

Silkscreen Front



Silkscreen Back



APPENDIX F – Data Group / Data Byte / Strobe Cross-Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
RDDatHi	RDDatB7	DQS7	63,62,61,60,59,58,57,56
	RDDatB6	DQS6	55,54,53,52,51,50,49,48
	RDDatB5	DQS5	47,46,45,44,43,42,41,40
	RDDatB4	DQS4	39,38,37,36,35,34,33,32
RDDatLo	RDDatB3	DQS3	31,30,29,28,27,26,25,24
	RDDatB2	DQS2	23,22,21,20,19,18,17,16
	RDDatB1	DQS1	15,14,13,12,11,10,9,8
	RDDatB0	DQS0	7,6,5,4,3,2,1,0
WRDatHi	WRDatB7	DQS7	63,62,61,60,59,58,57,56
	WRDatB6	DQS6	55,54,53,52,51,50,49,48
	WRDatB5	DQS5	47,46,45,44,43,42,41,40
	WRDatB4	DQS4	39,38,37,36,35,34,33,32
WRDatLo	WRDatB3	DQS3	31,30,29,28,27,26,25,24
	WRDatB2	DQS2	23,22,21,20,19,18,17,16
	WRDatB1	DQS1	15,14,13,12,11,10,9,8
	WRDatB0	DQS0	7,6,5,4,3,2,1,0

DDR2DC2A Groups/Bytes/Strobes Cross Reference

APPENDIX G - References

JEDEC PC2-4300/PC2-3200 DDR2 Unbuffered Reference Design Specification Revision 0.12

Tektronix TLA700 System User's Manual

Tektronix TLA700 Logic Analyzer User's Manual

P6810, P6860, and P6864 Logic Analyzer Probes Instruction Manual
Tektronix part number 071-1059-00

APPENDIX H - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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Support Contact Information

Technical Support	**techsupport@nexustechnology.com**
General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.