



NEX-DDRHSM

DDR (Double Data Rate)

Synchronous DRAM DIMM Support

Including these Software Support packages:
DDRHSM DDRHSM-RW DDRSPA

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1.0 OVERVIEW

1.1 General Information

The NEX-DDRHSM adapter has been designed to provide a quick and easy connection to interface a Tektronix TLA700 Logic Analyzer to a 184-pin 2.5volt PC1600/PC2100/PC2700/PC3200 72-bit wide Unbuffered or Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Module (DDR SDRAM DIMM) socket. Analyzer connections are made through P6860 High-Density Connectorless probes to help minimize the size of the adapter board, thus reducing trace length and keeping signal loading to a minimum.

Two software support packages have been included with the NEX-DDRHSM adapter to support up to 400MHz DDR:

DDRHSM offers the ability to synchronously acquire up to 400Mhz DDR Address and Command signals on every edge of DDR CK0, CK1 or CK2. Read Data or Write Data can also be acquired - the acquisition of DDR Data requires a valid data window of approximately 625ps. This support requires one TLA7AA4 or TLA7AB4 136-channel acquisition card with the 450MHz state clocking option. Refer to Section 5.0 for further information. The DDRHSM support is usable with a TLA7XX-series Logic Analyzer only, and must be running V4.2 or later of the TLA Application Software.

DDRHSMRW requires two merged TLA7AA4 or TLA7AB4 136-channel acquisition cards. This support is designed to give the user the ability to acquire up to 400MHz DDR Read and Write data. For this support to work, both merged cards must have the 450MHz state clocking option. Again, refer to Section 5.0 for further information. The DDRHSMRW support is usable with a TLA7XX-series Logic Analyzer only, and must be running V4.2 or later of the TLA Application Software. This software also post-processes the acquisition to display valid cycle information to the user.

Note that this manual uses some terms generically. For instance, references to the TLA700 apply to all suitable TLA700 Logic Analyzers. References to the “Adapter” apply to the NEX-DDRHSM adapter.

This manual assumes that the user is familiar with the Double Data Rate (DDR) SDRAM Specification (JEDEC Standard 79, Release 2) and the Tektronix TLA700 Logic Analyzers. It is also expected that the user is familiar with the Windows environment used on the TLA (Windows 2000).

2.0 SOFTWARE INSTALLATION

The NEX-DDRHSM software is loaded in the same method as other Windows programs. Place the DDRHSM or DDRHSMRW Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer module in the Setup window, select Load Support Package from the File pull-down, then choose DDRHSM or DDRHSMRW and click on **Okay**. Note that for the support requiring two merged modules that the TLA acquisition cards must be configured properly for the software to load.

3.0 CONNECTING to the NEX-DDRHSM ADAPTER

3.1 General

Care should be taken to support the weight of the acquisition probes so that the adapter board and/or target socket are not damaged

The NEX-DDRHSM adapter is larger than a standard DDR DIMM module, and is designed to function as an extender card while providing easy connections to acquire DDR data by the Logic Analyzer. It is entirely possible that placing a target card onto the NEX-DDRHSM adapter may result in improper operation of the target card or system.

Care should be used when removing a DIMM under test from the Adapter. The extraction tabs will break if excessive force is used.

When using the **DDRHSM** support, connect the TLA to the Adapter as follows:

- TLA A2/A3 probe head to DDRHSM MA-A2/A3 position
- TLA A0/A1 probe head to DDRHSM MA-A0/A1 position
- TLA D2/D3 probe head to DDRHSM SL-C2/C3 position
- TLA D0/D1 probe head to DDRHSM SL-E2/E3 position
- TLA C2/C3 probe head to DDRHSM MA-C2/C3 position
- TLA C0/C1 probe head to DDRHSM SL-A0/A1 position
- TLA E2/E3 probe head to DDRHSM MA-E2/E3 position
- TLA E0/E1 probe head to DDRHSM SL-A2/A3 position

Table 1 shows the Channel Grouping for the DDRHSM support.

When using **DDRHSMRW** support, two merged TLA7Axx acquisition cards are required. The Master card is the card in the lower-numbered slots; the Slave card is the card in the higher-numbered slots. The cards must be connected to the NEX-DDRHSM adapter as follows:

TLA Master A2/A3 probe head to DDRHSM MA-A2/A3 position
TLA Master A0/A1 probe head to DDRHSM MA-A0/A1 position
TLA Master C2/C3 probe head to DDRHSM MA-C2/C3 position
TLA Master E2/E3 probe head to DDRHSM MA-E2/E3 position
TLA Slave A2/A3 probe head to DDRHSM SL-A2/A3 position
TLA Slave A0/A1 probe head to DDRHSM SL-A0/A1 position
TLA Slave C2/C3 probe head to DDRHSM SL-C2/C3 position
TLA Slave E2/E3 probe head to DDRHSM SL-E2/E3 position

Table 2 shows the Channel Grouping / Wiring for use with the DDRHSMRW support.

Group Name	Signal Name	DDR Pin #	TLA70 0 Input	Group Name	Signal Name	DDR Pin #	TLA70 0 Input
DataHi (Hex)	DQ63	179	C3:7	DataLo (Hex)	DQ31	133	D3:3
	DQ62	178	C3:5		DQ30	131	A3:2
	DQ61	175	C3:2		DQ29	127	A2:7
	DQ60	174	C2:7		DQ28	126	D3:0
	DQ59	88	C1:2		DQ27	40	A3:4
	DQ58	87	C1:1		DQ26	39	D3:4
	DQ57	84	C3:4		DQ25	35	D2:7
	DQ56	83	C3:1		DQ24	33	A2:5
	DQ55	171	C0:6		DQ23	123	A2:4
	DQ54	170	C0:5		DQ22	121	A2:1
	DQ53	166	C0:2		DQ21	117	D2:2
	DQ52	165	C0:0		DQ20	114	D1:3
	DQ51	80	C1:0		DQ19	31	A2:3
	DQ50	79	C2:6		DQ18	28	A2:2
	DQ49	73	C0:1		DQ17	24	D1:7
	DQ48	72	E1:7		DQ16	23	D1:5
	DQ47	162	E1:2		DQ15	110	A1:4
	DQ46	161	E1:5		DQ14	109	A1:5
	DQ45	155	E3:4		DQ13	106	D1:1
	DQ44	153	E1:1		DQ12	105	A1:1
	DQ43	69	E1:4		DQ11	20	A1:7
	DQ42	68	E3:6		DQ10	19	A1:3
	DQ41	64	E3:3		DQ9	13	A0:7
	DQ40	61	E3:2		DQ8	12	D1:0
	DQ39	151	E0:7		DQ7	99	A0:4
	DQ38	150	E3:0		DQ6	98	D0:3
	DQ37	147	E2:5		DQ5	95	A0:0
	DQ36	146	E2:3		DQ4	94	D0:0
	DQ35	60	E3:1		DQ3	8	D0:5
	DQ34	57	E0:6		DQ2	6	D0:4
	DQ33	55	E0:5		DQ1	4	D0:1
	DQ32	53	E2:4		DQ0	2	D0:2

Table 1- DDRHSM TLA700 Channel Grouping

Group Name	Signal Name	DDR Pin #	TLA70 0 Input	Group Name	Signal Name	DDR Pin #	TLA70 0 Input
Address (Hex)	BA2	113	D1:4	Command (Sym)	S1~	158	Q3
	BA1	52	E2:2		S0~	157	C2:2
	BA0	59	E2:7		RAS~	154	C2:0
	A13	167	C0:3		CAS~	65	C2:3
	A12	115	D1:6	WE~	63	C2:1	
	A11	118	D2:1	Strobes (Hex)	DQS7	86	C3:6
	A10	141	E0:2		DQS6	78	C2:5
	A9	27	D2:3		DQS5	67	E3:5
	A8	122	D2:5		DQS4	56	E2:6
	A7	29	D2:4		DQS3	36	A3:0
	A6	125	A2:6		DQS2	25	D2:0
	A5	32	D2:6		DQS1	14	D0:7
	A4	37	D3:2	DQS0	5	A0:2	
	A3	130	A3:1	ChekBits	NC_CB7	144	E0:3
	A2	41	A3:3		NC_CB6	142	E0:4
A1	43	A3:5	NC_CB5		135	A3:6	
A0	48	E0:0	NC_CB4		134	D3:5	
			NC_CB3		51	E2:1	
Ungrouped	CKE1	111	A1:6	NC_CB2	49	E0:1	
	CKE0	21	D1:2	NC_CB1	45	A3:7	
	RESET~	10	A0:6	NC_CB0	44	D3:6	
	NC_DQS8	47	D3:7				
	NC_DM8	140	E2:0	WrtMasks	DM7	177	C3:3
	NC_S3~	163	E1:6		DM6	169	C2:4
	NC_S2~	71	E1:3		DM5	159	E3:7
	SCL	92	Q1		DM4	149	E1:0
	SDA	91	C1:7		DM3	129	D3:1
	SA2	183	C1:5		DM2	119	A2:0
	SA1	182	C1:6		DM1	107	A1:2
	SA0	181	C1:4	DM0	97	A0:1	
	Vddid	82	C0:7	Misc	DDRCK2	75	CK3
					DDRCK1	16	CK1
					DDRCK1	137	CK0
			DDRCK0				

Table 1 (cont'd.) – DDRHSM TLA700 Channel Grouping

~ Denotes a low true signal

Group Name	Signal Name	DDR Pin #	TLA700 Input	Group Name	Signal Name	DDR Pin #	TLA700 Input
RdDatHi (Hex)	RD_DQ63	179	C3:7	RdDatLo (Hex)	RD_DQ31	133	SC3:3
	RD_DQ62	178	C3:5		RD_DQ30	131	A3:2
	RD_DQ61	175	C3:2		RD_DQ29	127	A2:7
	RD_DQ60	174	C2:7		RD_DQ28	126	SC3:0
	RD_DQ59	88	SA1:2		RD_DQ27	40	A3:4
	RD_DQ58	87	SA1:1		RD_DQ26	39	SC3:4
	RD_DQ57	84	C3:4		RD_DQ25	35	SC2:7
	RD_DQ56	83	C3:1		RD_DQ24	33	A2:5
	RD_DQ55	171	SA0:6		RD_DQ23	123	A2:4
	RD_DQ54	170	SA0:5		RD_DQ22	121	A2:1
	RD_DQ53	166	SA0:2		RD_DQ21	117	SC2:2
	RD_DQ52	165	SA0:0		RD_DQ20	114	SE3:3
	RD_DQ51	80	SA1:0		RD_DQ19	31	A2:3
	RD_DQ50	79	C2:6		RD_DQ18	28	A2:2
	RD_DQ49	73	SA0:1		RD_DQ17	24	SE3:7
	RD_DQ48	72	SA3:7		RD_DQ16	23	SE3:5
	RD_DQ47	162	SA3:2		RD_DQ15	110	A1:4
	RD_DQ46	161	SA3:5		RD_DQ14	109	A1:5
	RD_DQ45	155	E3:4		RD_DQ13	106	SE3:1
	RD_DQ44	153	SA3:1		RD_DQ12	105	A1:1
	RD_DQ43	69	SA3:4		RD_DQ11	20	A1:7
	RD_DQ42	68	E3:6		RD_DQ10	19	A1:3
	RD_DQ41	64	E3:3		RD_DQ9	13	A0:7
	RD_DQ40	61	E3:2		RD_DQ8	12	SE3:0
	RD_DQ39	151	SA2:7		RD_DQ7	99	A0:4
	RD_DQ38	150	E3:0		RD_DQ6	98	SE2:3
	RD_DQ37	147	E2:5		RD_DQ5	95	A0:0
	RD_DQ36	146	E2:3		RD_DQ4	94	SE2:0
	RD_DQ35	60	E3:1		RD_DQ3	8	SE2:5
	RD_DQ34	57	SA2:6		RD_DQ2	6	SE2:4
	RD_DQ33	55	SA2:5		RD_DQ1	4	SE2:1
	RD_DQ32	53	E2:4		RD_DQ0	2	SE2:2

Table 2- DDRHSMRW TLA700 Channel Grouping

The 'S' in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	DDR Pin #	TLA700 Input	Group Name	Signal Name	DDR Pin #	TLA700 Input
WrDatHi (Hex)	WR_DQ63	179	C1:7	WrDatLo (Hex)	WR_DQ31	133	SC1:3
	WR_DQ62	178	C1:5		WR_DQ30	131	D3:2
	WR_DQ61	175	C1:2		WR_DQ29	127	D2:7
	WR_DQ60	174	C0:7		WR_DQ28	126	SC1:0
	WR_DQ59	88	SD1:2		WR_DQ27	40	D3:4
	WR_DQ58	87	SD1:1		WR_DQ26	39	SC1:4
	WR_DQ57	84	C1:4		WR_DQ25	35	SC0:7
	WR_DQ56	83	C1:1		WR_DQ24	33	D2:5
	WR_DQ55	171	SD0:6		WR_DQ23	123	D2:4
	WR_DQ54	170	SD0:5		WR_DQ22	121	D2:1
	WR_DQ53	166	SD0:2		WR_DQ21	117	SC0:2
	WR_DQ52	165	SD0:0		WR_DQ20	114	SE1:3
	WR_DQ51	80	SD1:0		WR_DQ19	31	D2:3
	WR_DQ50	79	C0:6		WR_DQ18	28	D2:2
	WR_DQ49	73	SD0:1		WR_DQ17	24	SE1:7
	WR_DQ48	72	SD3:7		WR_DQ16	23	SE1:5
	WR_DQ47	162	SD3:2		WR_DQ15	110	D1:4
	WR_DQ46	161	SD3:5		WR_DQ14	109	D1:5
	WR_DQ45	155	E1:4		WR_DQ13	106	SE1:1
	WR_DQ44	153	SD3:1		WR_DQ12	105	D1:1
	WR_DQ43	69	SD3:4		WR_DQ11	20	D1:7
	WR_DQ42	68	E1:6		WR_DQ10	19	D1:3
	WR_DQ41	64	E1:3		WR_DQ9	13	D0:7
	WR_DQ40	61	E1:2		WR_DQ8	12	SE1:0
	WR_DQ39	151	SD2:7		WR_DQ7	99	D0:4
	WR_DQ38	150	E1:0		WR_DQ6	98	SE0:3
	WR_DQ37	147	E0:5		WR_DQ5	95	D0:0
	WR_DQ36	146	E0:3		WR_DQ4	94	SE0:0
	WR_DQ35	60	E1:1		WR_DQ3	8	SE0:5
	WR_DQ34	57	SD2:6		WR_DQ2	6	SE0:4
	WR_DQ33	55	SD2:5		WR_DQ1	4	SE0:1
	WR_DQ32	53	E0:4		WR_DQ0	2	SE0:2

Table 2 (cont'd) – DDRHSMRW TLA700 Channel Grouping

The 'S' in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	DDR Pin #	TLA700 Input	Group Name	Signal Name	DDR Pin #	TLA700 Input
Address (Hex)	BA2	113	SE3:4	Command (Sym)	S1~	158	Q3
	BA1	52	E2:2		S0~	157	C2:2
	BA0	59	E2:7		RAS~	154	C2:0
	A13	167	SA0:3		CAS~	65	C2:3
	A12	115	SE3:6	WE~	63	C2:1	
	A11	118	SC2:1	Strobes (Hex)	DQS7	86	C3:6
	A10	141	SA2:2		DQS6	78	C2:5
	A9	27	SC2:3		DQS5	67	E3:5
	A8	122	SC2:5		DQS4	56	E2:6
	A7	29	SC2:4		DQS3	36	A3:0
	A6	125	A2:6		DQS2	25	SC2:0
	A5	32	SC2:6		DQS1	14	SE2:7
	A4	37	SC3:2		DQS0	5	A0:2
	A3	130	A3:1	ChekBits	NC_CB7	144	SA2:3
	A2	41	A3:3		NC_CB6	142	SA2:4
	A1	43	A3:5		NC_CB5	135	A3:6
A0	48	SA2:0	NC_CB4		134	SC3:5	
Ungrouped	CKE1	111	A1:6	NC_CB3	51	E2:1	
	CKE0	21	SE3:2	NC_CB2	49	SA2:1	
	RESET~	10	A0:6	NC_CB1	45	A3:7	
	NC_DQS8	47	SC3:7	NC_CB0	44	SC3:6	
	NC_DM8	140	E2:0	WrtMasks	DM7	177	C3:3
	NC_S3~	163	SA3:6		DM6	169	C2:4
	NC_S2~	71	SA3:3		DM5	159	E3:7
	SCL	92	SCK1		DM4	149	SA3:0
	SDA	91	SA1:7		DM3	129	SC3:1
	SA2	183	SA1:5		DM2	119	A2:0
	SA1	182	SA1:6		DM1	107	A1:2
	SA0	181	SA1:4	DM0	97	A0:1	
	Vddid	82	SA0:7	Misc	DDRCK2	75	CK3
					DDRCK1	16	CK1
					DDRCK0	137	CK0

Table 2 (cont'd) – DDRHSMRW TLA700 Channel Grouping

~ Denotes a low true signal

The 'S' in front of a TLA channel denotes the Slave card of the merged pair

4.0 CLOCK SELECTION

There are two clocking option fields available when using the DDRHSM or DDRHSMRW support packages. These select fields permit the user to setup the TLA acquisition as follows:

SDRAM Clocking: – Permits selecting the DDR Clock to be used to acquire data. Also allows user to use only Chip Select S0~ or Chip Selects S0~ and S1~ for acquisition. The field choices are:

DDR CK0; S0~ only active (default)

DDR CK0; S0~ & S1~ active

DDR CK1; S0~ only active

DDR CK1 S0~ & S1~ active

DDR CK2 S0~ only active

DDR CK2 S0~ & S1~ active

Clock Mode – Allows the user to choose the kind of data acquisition that will be made:

Selective Clocking (default) – This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS~ or CAS~ is asserted low along with S0~ or S1~. After every assertion of CAS~ (with either S0~ or S1~) an additional 17 samples are taken on every DDR CLK edge. If CAS~ and a Chip Select are asserted during these 17 samples the count is reset.

Note: this mode will NOT work if the DDR target is using Chip Selects S3~ or S4~ to enable the DDR memory.

Every SDRAM Clock Edge – As the name implies this will cause the acquisition card to store data on every Rising and Falling edge of the selected SDRAM clock.

Refresh Cycles: – Permits choosing whether Refresh Cycles will be stored or not. The field choices are:

Do Not Acquire (default) – This mode will reduce the number of Refresh cycles stored by the acquisition card to provide optimum use of the acquisition memory.

Note: this mode will NOT work if the DDR target is using Chip Selects S3~ or S4~ to enable the DDR memory.

Acquire – Refresh Cycles will be stored.

5.0 CONFIGURING FOR READ / WRITE DATA ACQUISITION

IMPORTANT !

Prior to configuring your NEX-DDRHSM support package it is *strongly* recommended that Appendix A (“How DDR Data is Clocked”), section 5.2 (“Selecting DDR Read Sample Points”) and section 5.3 (“Selecting DDR Write Sample Points”) be read. This background information is very helpful in properly configuring the support.

5.1 Adjusting Input Thresholds for Proper Data Acquisition

The voltage threshold must be properly set on the TLA for proper acquisition of the DDR bus. We recommend that you verify the center point of the SDRAM CK0, any DDR strobe, and any DDR data bit. The CLK threshold should be set close to 0v because the clock is a differential signal. The threshold setting can be verified that it is correct by taking a TLA acquisition and verifying a 50% duty cycle on the clock by looking at the DDRCK2, DDRCK1 or DDRCK0 MagniVu trace. All other signals should be set close to center of the voltage swing. Please note that synchronous acquisition using a TLA7AAx or TLA7ABx card requires a valid data window of approximately 625ps.

Although you should measure and set the thresholds as described, you can start with a 1.1V threshold value for all signals except for TLA CLK3, CLK1 and CLK0 which should be set to 0.07V because they are differential signals. These values can be used as a starting point.

5.2 Selecting DDR Read Sample Points

For the DDRHSMRW post-processing software to accurately show valid data it is necessary to choose the proper sample points to ensure that valid data is acquired when the software expects it. Since valid DDR Read data is straddled by the Strokes (see Figures 1 and 2), and the Strokes are phase-aligned with the DDR clock for Reads, the Setup & Hold sample point must be set for the valid data that occurs after the clock edge.

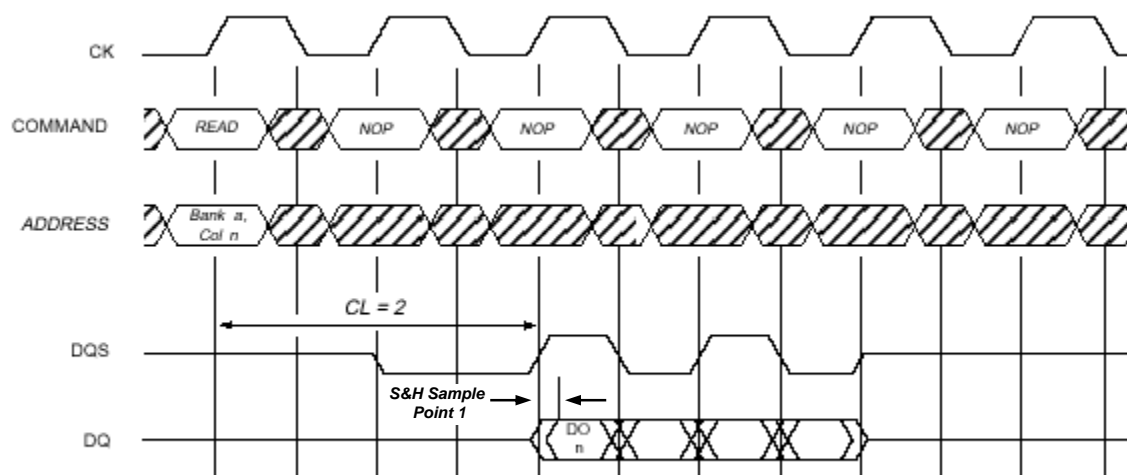


Figure 1- Read Cycle, CAS Latency = 2 cycles

For DDRHSM and DDRHSMRW support data is acquired on both rising and falling clock edges so only one sample point (illustrated by *S&H Sample Point 1* in Figures 1 and 2) need be set.

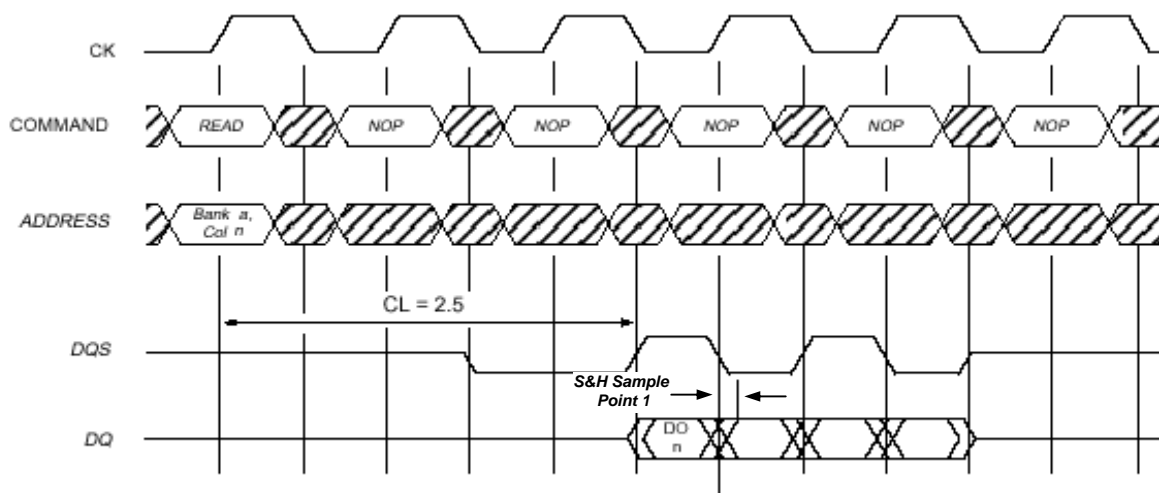


Figure 2- Read Cycle, CAS Latency = 2.5 cycles

5.3 Selecting DDR Write Sample Points

Unlike valid DDR Read data, valid Write data is bisected by the Strobes. This is complicated by the delay from the Write command to the first Strobe rising edge varying anywhere from 75% to 125% of a clock cycle. These two extremes are illustrated in Figures 3 and 4.

IMPORTANT!

For valid Write data to be acquired and stored at the proper point for the DDRHSMRW software to interpret it, the Setup & Hold sample points ***must*** be determined relative to the first rising clock edge after the Write command or, in the case of Registered DDR DIMMs, the second rising clock edge. If the Strobes transition from zeroes to ones before the clock edge then positive Setup and negative Hold values will be entered. If the Strobe transition after the edge then negative Setup and positive Hold values will be correct.

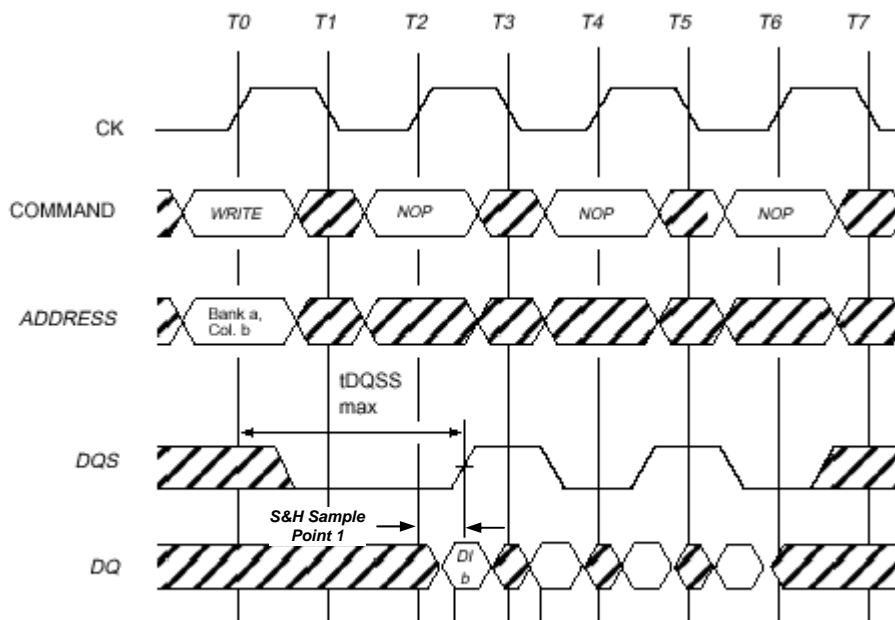


Figure 3- Write Cycle, Maximum Strobe Delay

For DDRHSM and DDRHSMRW support data is acquired on both rising and falling clock edges so only one sample point (illustrated by ***S&H Sample Point 1*** in Figures 3 and 4 need be set. It is recommended that the Write Data sample points be set at or near the transition points of the Strobes. The sample point for the WrMasks group should also be set to the transition point of the Strobes (DQS signals) for proper acquisition, again as shown by ***S&H Sample Point 1***.

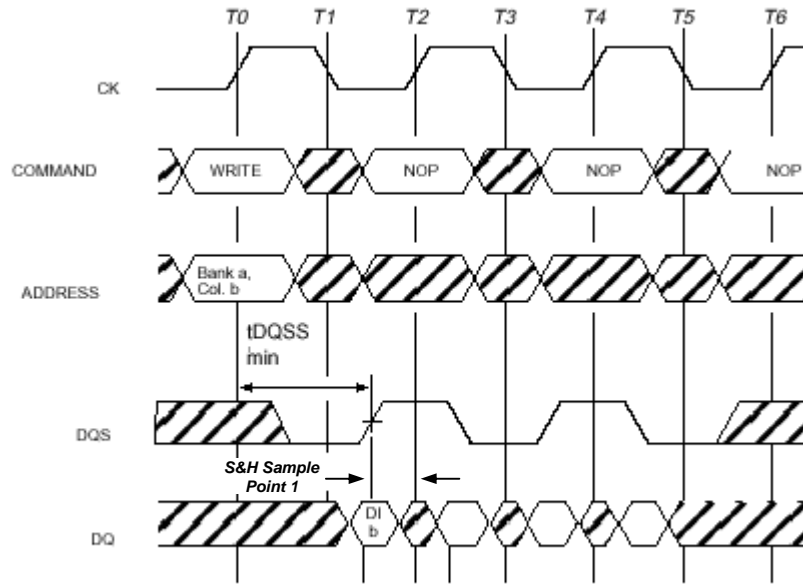


Figure 4- Write Cycle, Minimum Strobe Delay

5.4 DDRHSM Support

Using the NEX-DDRHSM support it is possible to acquire either Read data or Write data by moving the sample point of the data groups appropriately. To adjust the Data group sample points first make an appropriate acquisition of either Read or Write data by triggering on the cycle of interest (Read or Write Command Cycle). Then create a timing window display of MagniVu data and display the two 32-bits groups (DataHi and DataLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2). A sample waveform display of MagniVu Read data is shown in Figure 5 To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (note arrows in Figure 5).

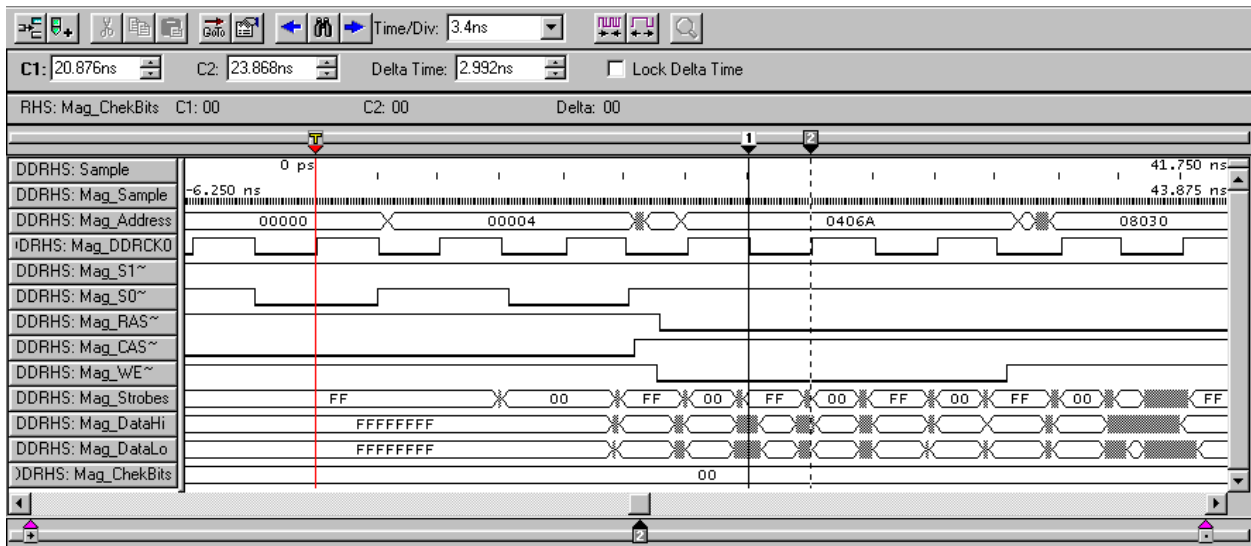


Figure 5- Locating Minimum Valid DDRHSM Read Data Window

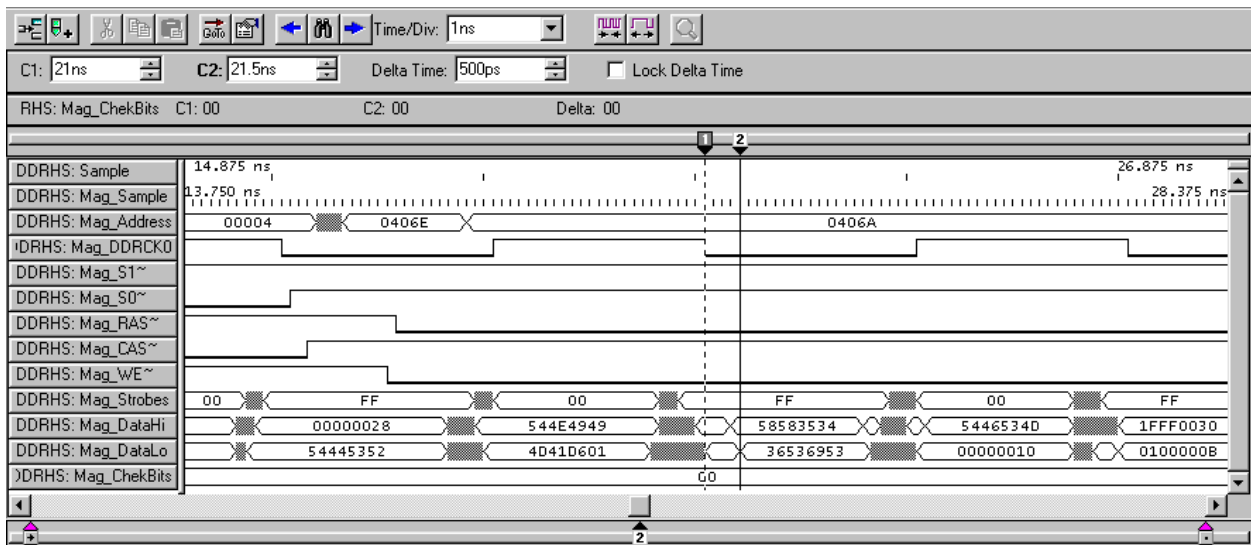


Figure 6- Measuring DDRHSM Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 6 and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is 500ps, meaning that a suitable Setup & Hold value would be $-500\text{ps}/1.125\text{ns}$. Since the data stable window is much larger than required a value of $-1\text{ns}/1.625\text{ns}$ might be better as is further into the stable data window.

It is this value that must be programmed into the LA card's Setup & Hold window to enable proper data acquisition (see Figure 7. This window is found by going to the LA Card's Setup window, then clicking on the **More** button to the right of the clock select field. The TLA7Axx acquisition cards require a stable valid data window of 625s, and this window can be placed to begin from 16.25ns prior to the clock edge to 7.625ns after the edge in 125ps increments. Each 32-bit data group (DataHi and DataLo) will require its own value programmed from the measurements noted in the MagniVu window, although it is very likely that the same value is suitable for both data groups.

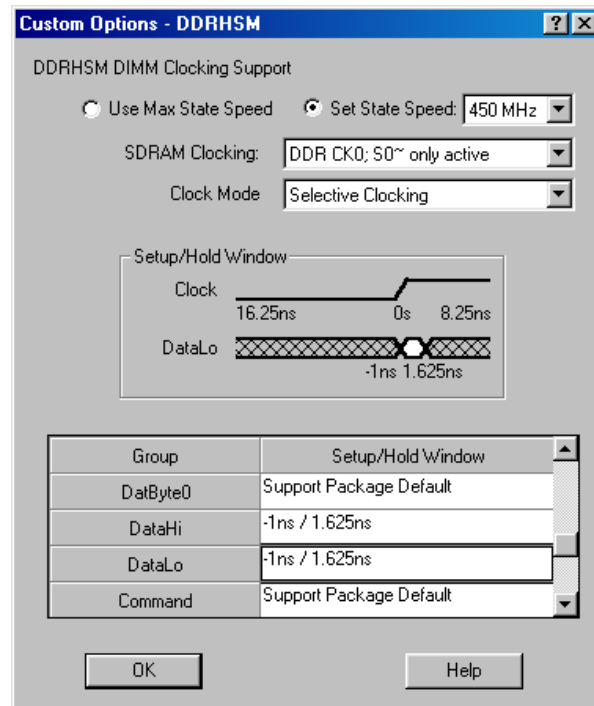


Figure 7- Setting DDRHSM Setup & Hold Sample Points

Setting the Setup & Hold values for acquiring Write data is similar, but the valid data point now more closely aligns with the Strobe edges. Figure 8 shows a Waveform display of DDRHSM Write data with a suitable data valid window delineated by the cursors (see arrows). The window of valid Write data again appears to be 1.6ns. But Figure 9 shows a zoomed-in view of the same data but with the Setup & Hold points marked by the cursors. Note that a suitable value now for reliable data acquisition would be $-1.0\text{ns}/1.625\text{ns}$, coincidentally the same as the value determined for Read data. Note again that the WrtMasks group should have the same Setup & Hold setting as that of the Write Data.

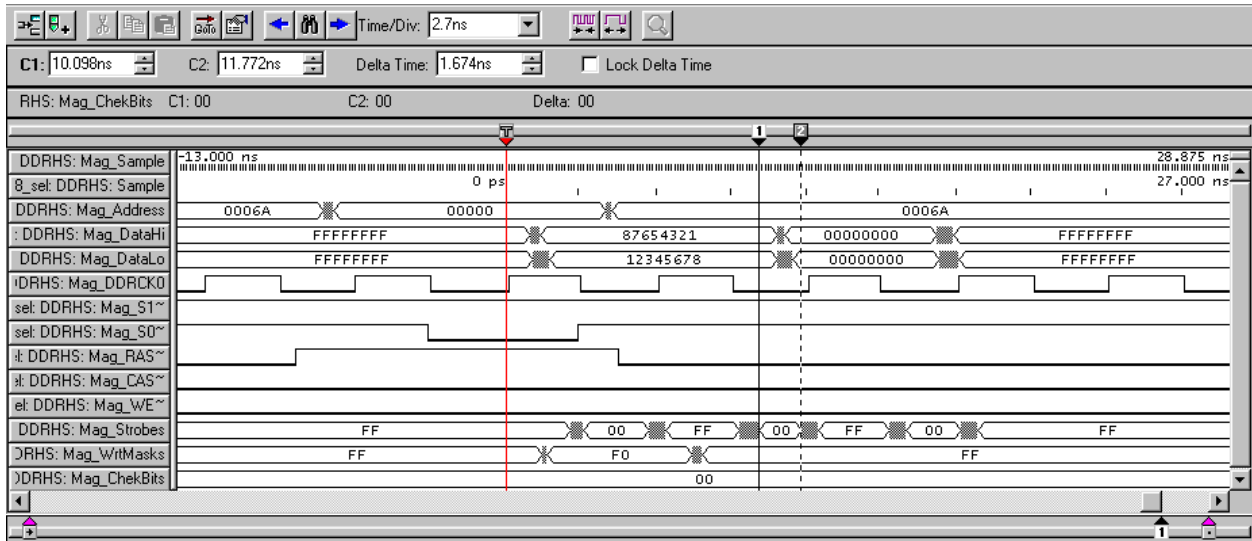


Figure 8- Locating Minimum Valid DDRHSM Write Data Window



Figure 9- Measuring DDRHSM Write Data Setup & Hold

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 10 shows these added data groups (DatByte7-0) added to the same Waveform display shown in Figure 5. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see Figure 11). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit groups make up a 32-bit group.

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (DataHi or DataLo) be reset to “Support Package Default”. This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values –

625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

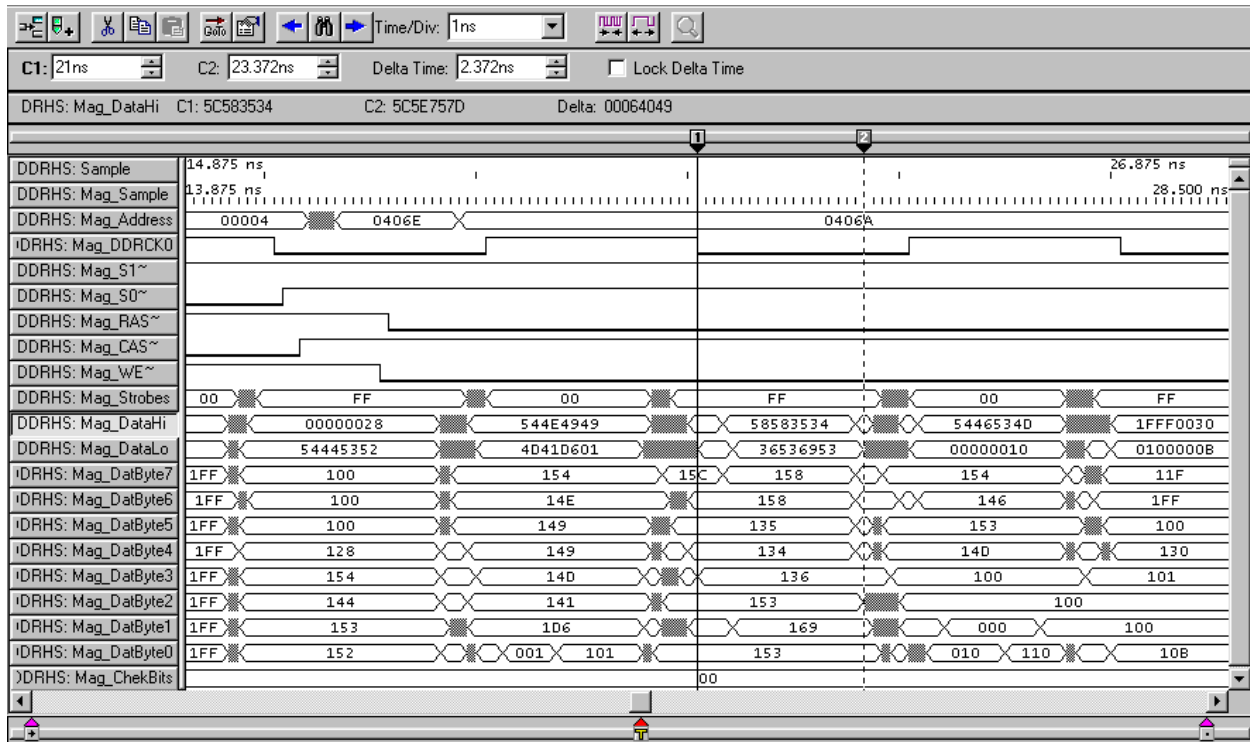


Figure 10- Viewing Individual 8-bit Data Groups

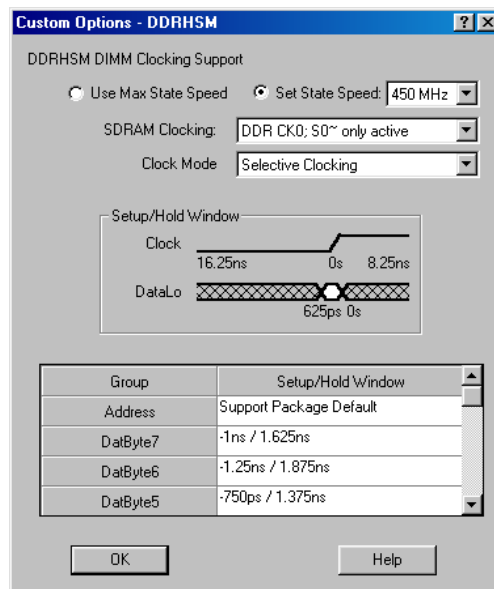


Figure 11- Setting Individual Setup & Hold Values for the 8-bit Data Groups

Note: Values shown are for illustration purposes only

5.5 DDRHSMRW Support

The DDRHSMRW support requires the same setup steps as those outlined in the DDR200 mode (see section 5.4). However, instead of programming 2 data groups it is now necessary to program the sample windows for four 32-bit data groups because both Read and Write data are acquired.

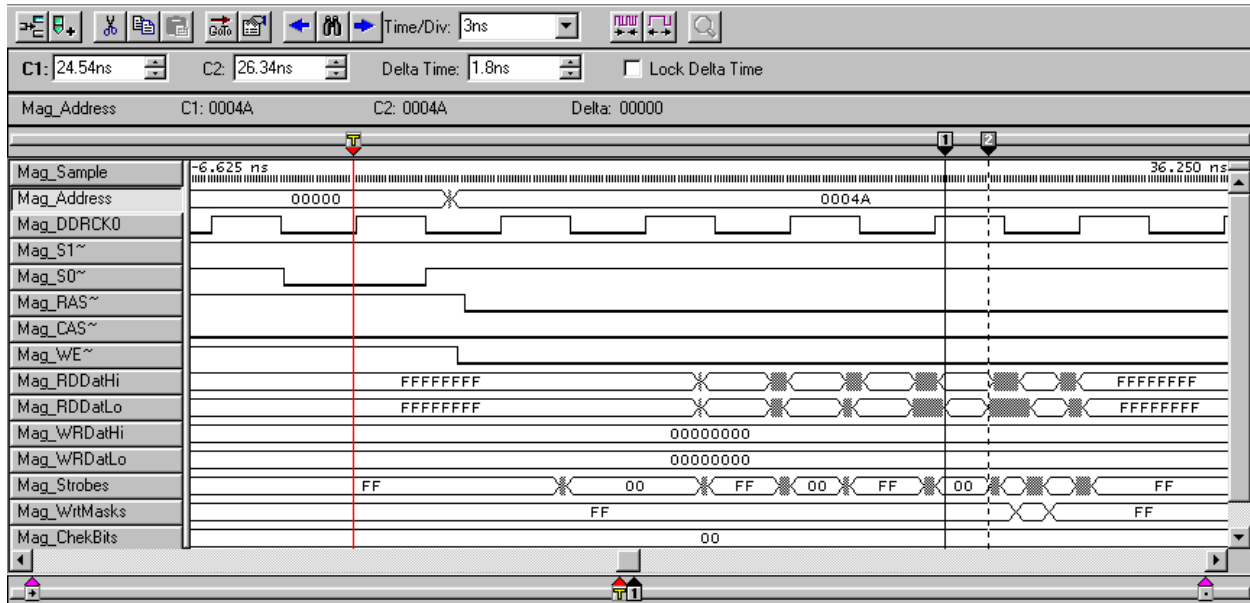


Figure 12- Locating Minimum Valid DDRHSMRW Read Data Window

To adjust the Read Data group sample points first make an appropriate acquisition of Read data by triggering on a Read Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2). A sample waveform display of MagniVu Read data is shown in Figure 12. To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (note arrows in Figure 12).

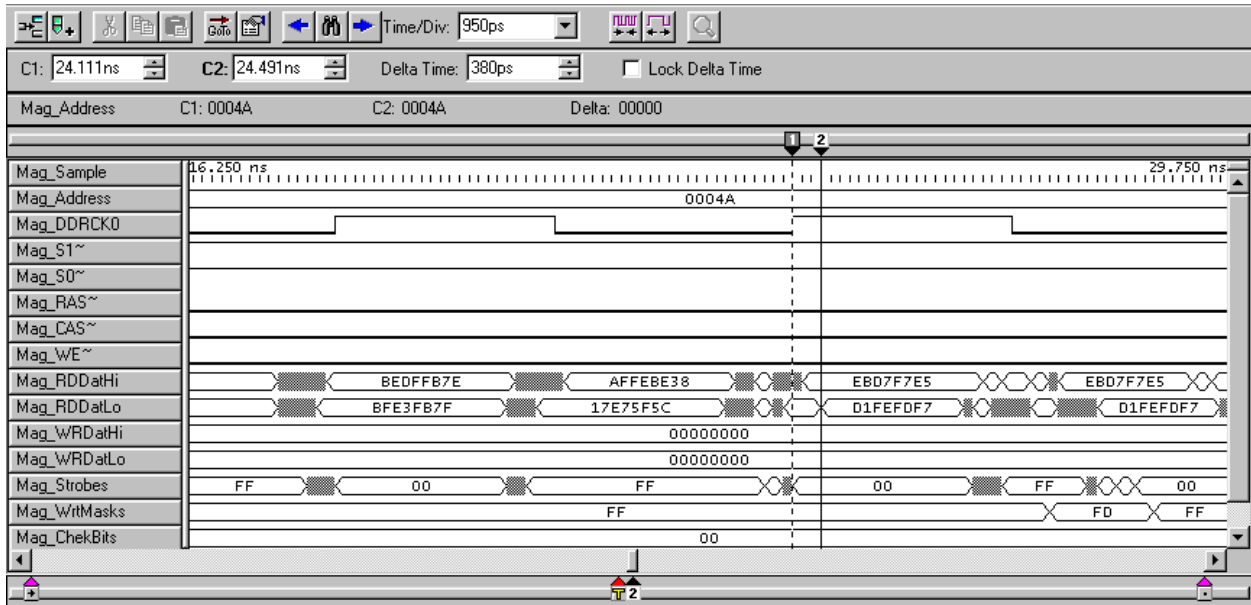


Figure 13- Measuring DDRHSMRW Read Data Setup & Hold

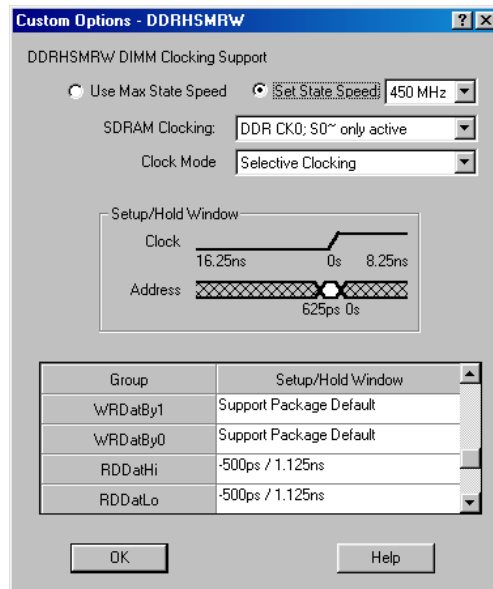


Figure 14- Setting DDRHSMRW Read Data Setup & Hold Sample Points

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 13) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is ~380ps, meaning that a suitable Setup & Hold value would be -500ps/1.125ns. This sample point position must now be set for the RDDatHi and RDDatLo groups in the Setup window. This window is found by going to the LA Card's Setup window, then clicking on the More button to the right of the clock select field.

be set for the WRDatHi and WRDatLo groups in the Setup window (Figure 17). Note that the WrtMasks group should have a Setup & Hold value that aligns with the transition of the Strobes.

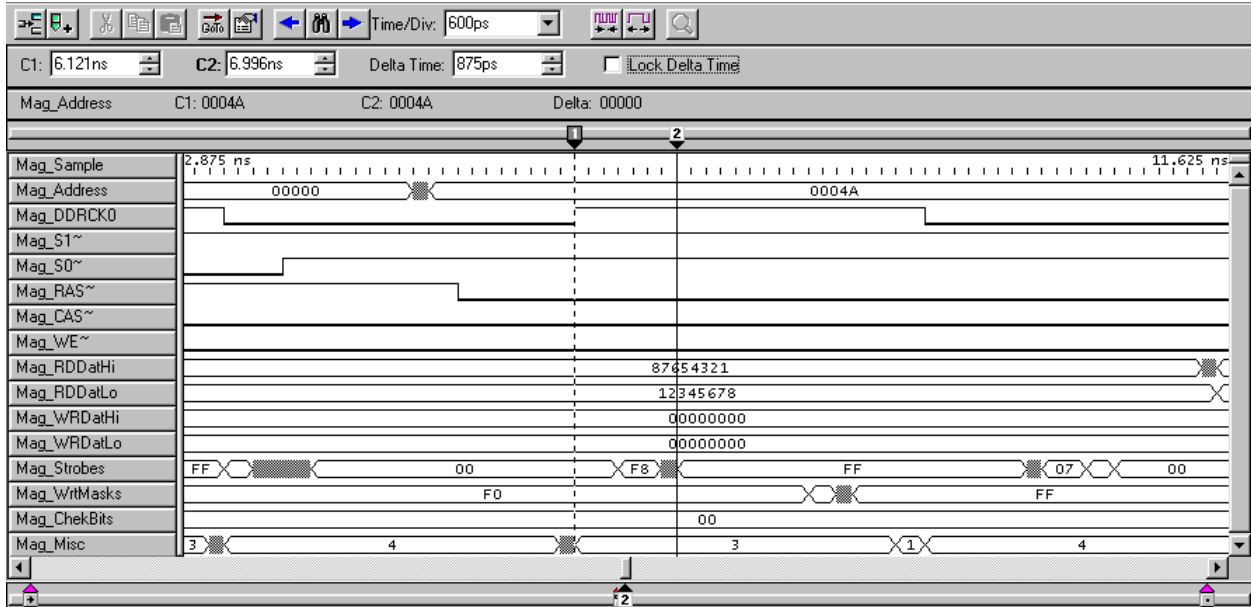


Figure 16- Measuring DDRHSMRW Write Data Setup & Hold

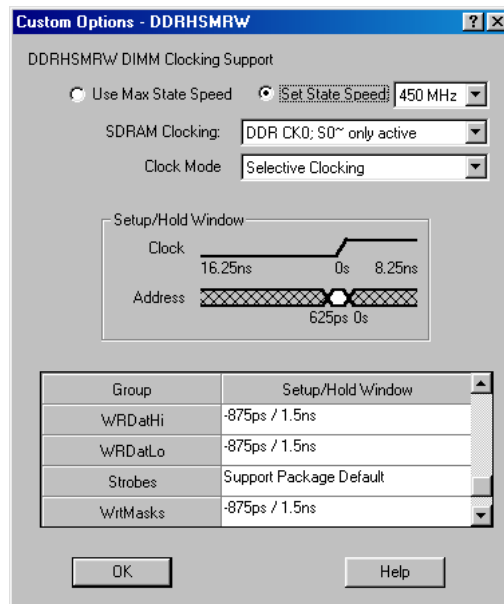


Figure 17- Setting DDRHSMRW Write Data Setup & Hold Sample Points

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 18 shows these added data groups (DatByte7-0) added to the same Waveform display shown in Figure 15. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA

Setup window (see Figure 19). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit groups make up a 32-bit group.

Note: Again, it is very important to remember that, because of the method used to acquire Write Data using the DDRHSMRW support, the Read Data group information must be used to determine the Write Data sample points. For further explanation of this process refer to Appendix A “How DDR Data is Clocked”.

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (RDDatHi, RDDatLo, WRDatHi or WRDatLo) be reset to “Support Package Default”. This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values – 625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

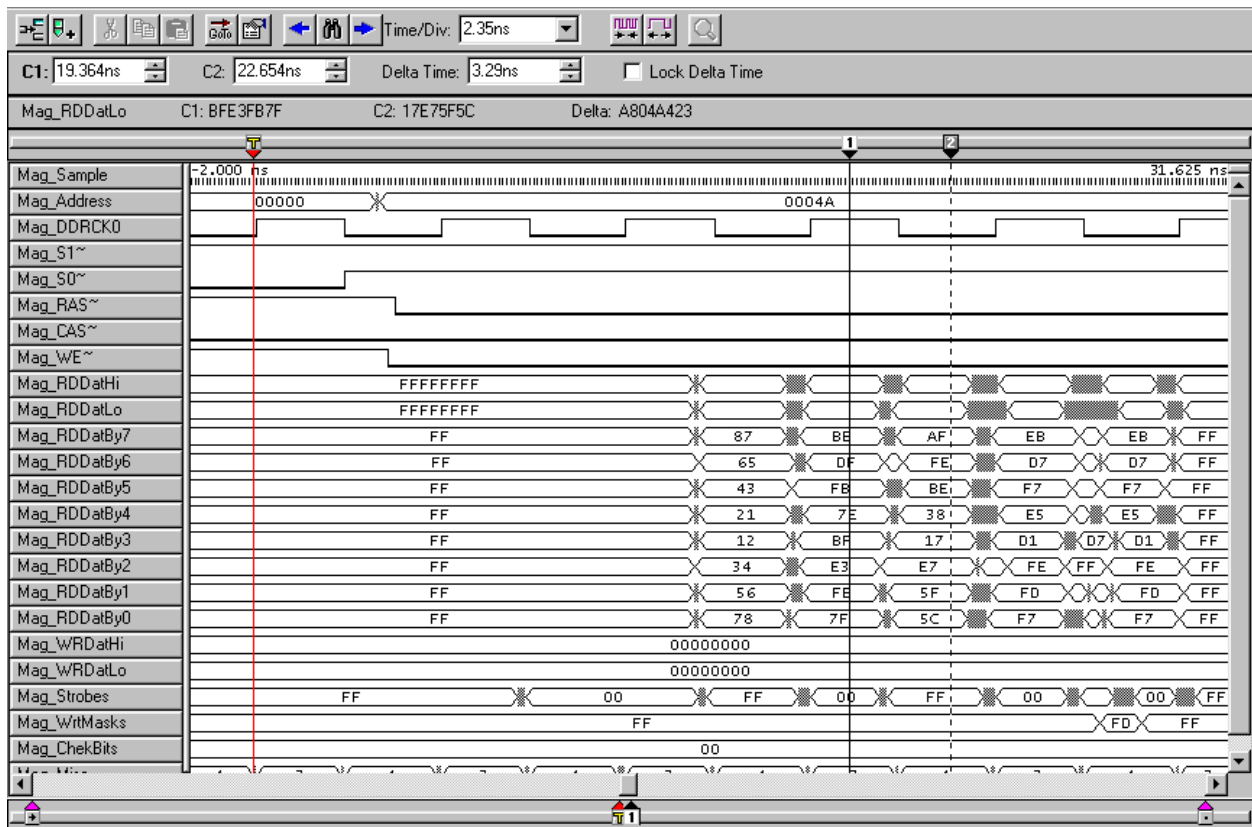


Figure 18- Viewing Individual 8-bit Read Data Groups

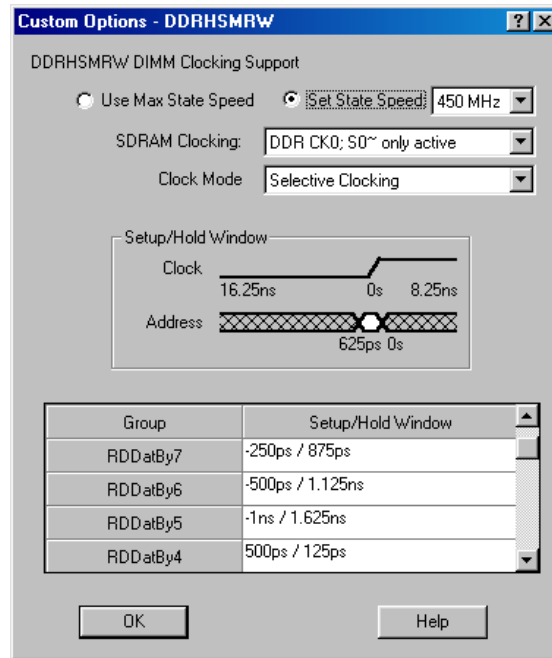


Figure 19- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

Note: Values shown are for illustration purposes only

6.0 VIEWING DATA

6.1 Viewing State Data on the TLA - General

After making an initial acquisition, the TLA will display the data in the Listing (State) format. A Symbol Table has been included in the support package for the Command data group (see Table 3). The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. The symbol file has been created to permit quickly showing the type of transaction that occurred on the DDR Bus - a Read, Write, Precharge, etc. This symbol information can also be used to trigger on a DDR cycle of interest.

It is important to note that changing the group, channel, or wiring of the Command group can result in incorrect symbol information being displayed.

Symbol	Definition
DESL--IGNORE_COMMAND--DATA?	11 xxx
NOP--NO_OPERATION_(S0~)	x0 111
NOP--NO_OPERATION_(S1~)	0x 111
BST--BURST_STOP_(S0~)	x0 110
BST--BURST_STOP_(S1~)	0x 110
READ--COL_ADDR_READ_(S0~)	x0 101
READ--COL_ADDR_READ_(S1~)	0x 101
WRITE--COL_ADDR_WRITE_(S0~)	x0 100
WRITE--COL_ADDR_WRITE_(S1~)	0x 100
ACTV--	x0 011
ROW_ADDRESS_STROBE_(S0~)	
ACTV--	0x 011
ROW_ADDRESS_STROBE_(S1~)	
PRE--	x0 010
PRECHARGE_SELECT_BANK_(S0~)	
PRE--	0x 010
PRECHARGE_SELECT_BANK_(S1~)	
PALL--	x0 010
PRECHARGE_ALL_BANK_(S0~)	
PALL--	0x 010
PRECHARGE_ALL_BANK_(S1~)	
REF--REFRESH_(S0~)	x0 001
REF--REFRESH_(S1~)	0x 001
MRS--MODE_REGISTER_SET_(S0~)	x0 000
MRS--MODE_REGISTER_SET_(S1~)	0x 000

Table 3- DDRHSM / DDRHSMRW Support Command Symbol Table
Signals, left-to-right: S1~, S0~, RAS~, CAS~, WE~

6.2 Viewing DDRHS Data

When using the DDRHSM support package the Address, DataHi, DataLo, and Strobes group data is displayed in hexadecimal format; the Command, ChekBits, WrtMsk, Misc, and all eight Data Byte (DatBytex) groups default to OFF.

The Command group is suppressed because its function is replaced with a column labeled “DDRHSM Mnemonics”. The DDRHSM support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 20 shows the default display where all DDR data is displayed.

Sample	DDRHSM Address	DDRHSM DataHi	DDRHSM DataLo	DDRHSM Mnemonics	DDRHSM Strobes	DDRHSM WrtMasks	Timestamp
2042	0DBFF	FFFFFFFF	FFFFFFFF	REF - REFRESH (S0~)	3F	FF	15.287,500 us
2043	0DBFF	FFFFFFFF	FFFFFFFF	REF - REFRESH (S0~)	FF	FF	15.188,625 us
2044	0DBFF	FFFFFFFF	FFFFFFFF	REF - REFRESH (S0~)	FF	FF	15.149,125 us
2045	0DBFF	20010000	00000000	REF - REFRESH (S0~)	FC	FF	15.228,750 us
2046	00E91	FFFFFFFF	FFFFFFFF	ACTV - ROW ADDRESS STROBE (S0~)	FF	FF	3.871,500 us
2047	01AD7	FFFFFFFF	FFFFFFFF	READ - COL ADDR READ (S0~)	FF	FF	19.750 ns
2048	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2049	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	02	FF	4.875 ns
2050	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	00	FF	4.875 ns
2051	0DBFF	486E6570	4F676552	READ DATA	FF	FF	5.000 ns
2052	0DBFF	448B0057	78457965	READ DATA	FF	FF	5.000 ns
2053	0DBFF	850F7401	F8830824	READ DATA	FF	FF	4.875 ns
2054	0DBFF	267502F8	831C74C0	READ DATA	FF	FF	5.000 ns
2055	0DBFF	448B000C	C258016A	READ DATA	FF	FF	4.875 ns
2056	01ACF	77970740	A3500424	READ DATA	FF	FF	5.000 ns
2057	01ACF	39ECEB00	0000FDE8	READ - COL ADDR READ (S0~)	FF	FF	5.000 ns
2058	0DBFF	E8016AE3	790C2444	READ DATA	FF	FF	5.000 ns
2059	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	00	FF	4.875 ns
2060	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	00	FF	5.000 ns
2061	0DBFF	F88300E8	00008F97	READ DATA	FF	FF	4.875 ns
2062	0DBFF	7796E024	A1D57503	READ DATA	FF	FF	5.000 ns
2063	0DBFF	50006A09	74FF883	READ DATA	FF	FF	4.875 ns
2064	0DBFF	02E87795	105415FF	READ DATA	FF	FF	5.000 ns
2065	0DBFF	FF5351B8	E8000000	READ DATA	FF	FF	5.000 ns
2066	0DBFF	07706877	95103015	READ DATA	FF	FF	4.875 ns
2067	0DBFF	15FF0824	44897797	READ DATA	FF	FF	5.000 ns
2068	0DBFF	E0081D88	7795101C	READ DATA	77	FF	5.000 ns
2069	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	4.875 ns
2070	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2071	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	4.875 ns
2072	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2073	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2074	05FFF	FFFFFFFF	FFFFFFFF	(UNKNOWN)	FF	FF	4.875 ns
2075	01FFF	FFFFFFFF	FFFFFFFF	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	5.000 ns
2076	00E91	FFFFFFFF	FFFFFFFF	ACTV - ROW ADDRESS STROBE (S0~)	FF	FF	59.375 ns
2077	01AC7	FFFFFFFF	FFFFFFFF	READ - COL ADDR READ (S0~)	FF	FF	19.750 ns
2078	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2079	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	02	FF	4.875 ns
2080	0DBFF	FFFFFFFF	FFFFFFFF	DESL - IGNORE COMMAND	00	FF	5.000 ns
2081	0DBFF	7796E008	F8817796	READ DATA	FF	FF	5.000 ns
2082	0DBFF	FF779707	70680E75	READ DATA	FF	FF	4.875 ns
2083	0DBFF	C3595B77	95101815	READ DATA	FF	FF	5.000 ns
2084	0DBFF	E850FC43	8D555657	READ DATA	77	FF	5.000 ns
2085	0DBFF	F685F088	00000B3D	READ DATA	FF	FF	4.875 ns
2086	0DBFF	AE8D0000	F7C1840F	READ DATA	FF	FF	5.000 ns
2087	0DBFF	1C15FF55	000000EC	READ DATA	FF	FF	4.875 ns
2088	04AFF	4E8D1C46	8B779510	READ DATA	7F	FF	5.000 ns

Figure 20- DDRHSM State Display - Show All Data? = Yes

To change the display it is necessary to bring up the window’s Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in Figure 21.

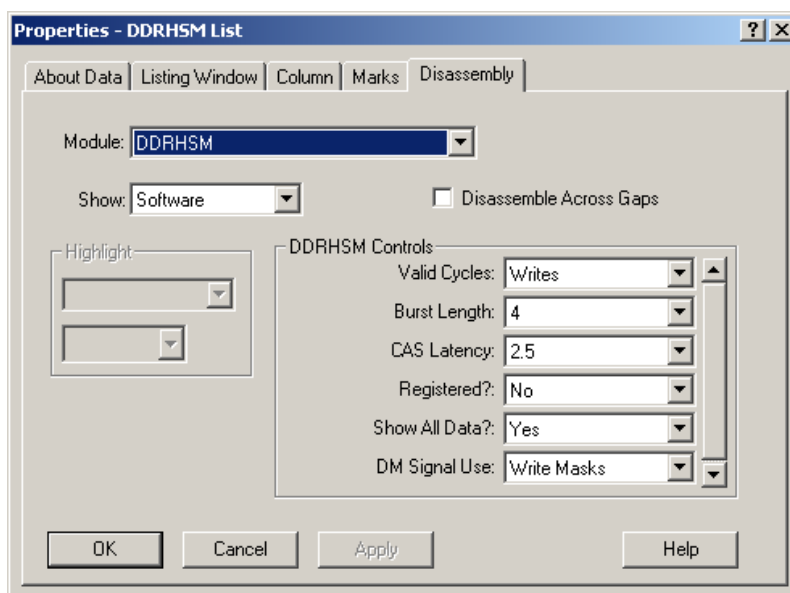


Figure 21- DDRHSM Disassembly Properties

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

Valid Cycles – tells the post-processing software whether the DDRHSM support was configured to acquire valid Read or Write data.

Burst Length – permits setting the burst length for Read and Write data. Valid choices are 2 (the default), 4, and 8. This value must be set properly for all valid Read and Write data to be displayed.

CAS Latency – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 1.5 (default), 2.0, 2.5, and 3 cycles.

Registered? – must be set to reflect whether or not Registered DDR memory is used. Default is No. When set to Yes an additional clock cycle delay is added to CAS Latency and to valid Write Data tagging.

Show All Data? – permits choosing between displaying all DDR data (default), including Invalid Read / Write and Command data, and showing only valid Data and Command data.

DM Signal Use – permits setting Data Mask functionality to Write Masks (default) or Strobes. When set to Write Mask the DM signals will be used to mask Write Data to show which data bytes were valid in the cycle.

When setting **Show All Data?** to No, the display in Figure 20 then becomes the display in Figure 22. This allows the user to see at a glance the valid information on the bus.

Sample	DDRHSM Address	DDRHSM DataHi	DDRHSM DataLo	DDRHSM Mnemonics	DDRHSM Strobes	DDRHSM WrtMasks	Timestamp
2042	0DBFF	-----	-----	REF - REFRESH (50~)	3F	FF	15.287,500 us
2043	0DBFF	-----	-----	REF - REFRESH (50~)	FF	FF	15.188,625 us
2044	0DBFF	-----	-----	REF - REFRESH (50~)	FF	FF	15.149,125 us
2045	0DBFF	-----	-----	REF - REFRESH (50~)	FC	FF	15.228,750 us
2046	00E91	-----	-----	ACTV - ROW ADDRESS STROBE (50~)	FF	FF	3.871,500 us
2047	01AD7	-----	-----	READ - COL ADDR READ (50~)	FF	FF	19.750 ns
2048	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2049	-----	-----	-----	DESL - IGNORE COMMAND	02	FF	4.875 ns
2050	-----	-----	-----	DESL - IGNORE COMMAND	00	FF	4.875 ns
2051	486E6570	4F676552	4F676552	READ DATA	FF	FF	5.000 ns
2052	448B0057	78457965	78457965	READ DATA	FF	FF	5.000 ns
2053	850F7401	F8830824	F8830824	READ DATA	FF	FF	4.875 ns
2054	267502F8	831C74C0	831C74C0	READ DATA	FF	FF	5.000 ns
2055	448B000C	C258016A	C258016A	READ DATA	FF	FF	4.875 ns
2056	77970740	A3500424	A3500424	READ DATA	FF	FF	5.000 ns
2057	01ACF	-----	-----	READ - COL ADDR READ (50~)	FF	FF	5.000 ns
2058	39ECEB00	0000FDE8	0000FDE8	READ DATA	FF	FF	4.875 ns
2059	E8016AE3	750C2444	750C2444	READ DATA	FF	FF	5.000 ns
2060	-----	-----	-----	DESL - IGNORE COMMAND	00	FF	5.000 ns
2061	-----	-----	-----	DESL - IGNORE COMMAND	00	FF	4.875 ns
2062	F883DDEB	00008F97	00008F97	READ DATA	FF	FF	4.875 ns
2063	7796E024	A1D57503	A1D57503	READ DATA	FF	FF	5.000 ns
2064	50006A09	74FFF883	74FFF883	READ DATA	FF	FF	4.875 ns
2065	02E87795	105415FF	105415FF	READ DATA	FF	FF	5.000 ns
2066	FF5351B8	E8000000	E8000000	READ DATA	FF	FF	5.000 ns
2067	07706877	95103015	95103015	READ DATA	FF	FF	4.875 ns
2068	15FF0824	44897797	44897797	READ DATA	FF	FF	5.000 ns
2069	E0081D88	7795101C	7795101C	READ DATA	77	FF	5.000 ns
2070	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	4.875 ns
2071	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2072	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	4.875 ns
2073	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2074	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	4.875 ns
2075	-----	-----	-----	(UNKNOWN)	FF	FF	5.000 ns
2076	01FFF	-----	-----	PRE - PRECHARGE SELECT BANK (50~)	FF	FF	5.000 ns
2077	00E91	-----	-----	ACTV - ROW ADDRESS STROBE (50~)	FF	FF	59.375 ns
2078	01AC7	-----	-----	READ - COL ADDR READ (50~)	FF	FF	19.750 ns
2079	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	5.000 ns
2080	-----	-----	-----	DESL - IGNORE COMMAND	02	FF	4.875 ns
2081	-----	-----	-----	DESL - IGNORE COMMAND	00	FF	5.000 ns
2082	7796E008	F8817796	F8817796	READ DATA	FF	FF	5.000 ns
2083	FF779707	70680E75	70680E75	READ DATA	FF	FF	4.875 ns
2084	C3595B77	95101815	95101815	READ DATA	FF	FF	5.000 ns
2085	E850FC43	8D555657	8D555657	READ DATA	77	FF	5.000 ns
2086	F685F088	00000B3D	00000B3D	READ DATA	FF	FF	4.875 ns
2087	AE8D0000	F7C1840F	F7C1840F	READ DATA	FF	FF	5.000 ns
2088	1C15FF55	000000EC	000000EC	READ DATA	FF	FF	4.875 ns
2089	4E8D1C46	8B779510	8B779510	READ DATA	7F	FF	5.000 ns

Figure 22- DDRHSM State Display - Show All Data? = No

In addition to the Disassembly Properties selections discussed earlier, changing the settings in the **Show** field result in display changes as well:

Hardware – displays all acquired cycles

Software – suppresses all idle or wait cycles

Control Flow – shows Address Command and valid Read / Write data cycles

Subroutine – shows valid Read / Write data cycles only

Changing the Show field setting in the display of Figure 22 from Hardware to Control Flow results in the display of Figure 23 where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles. Figure 24 shows the same data but with Valid Cycles set to Writes.

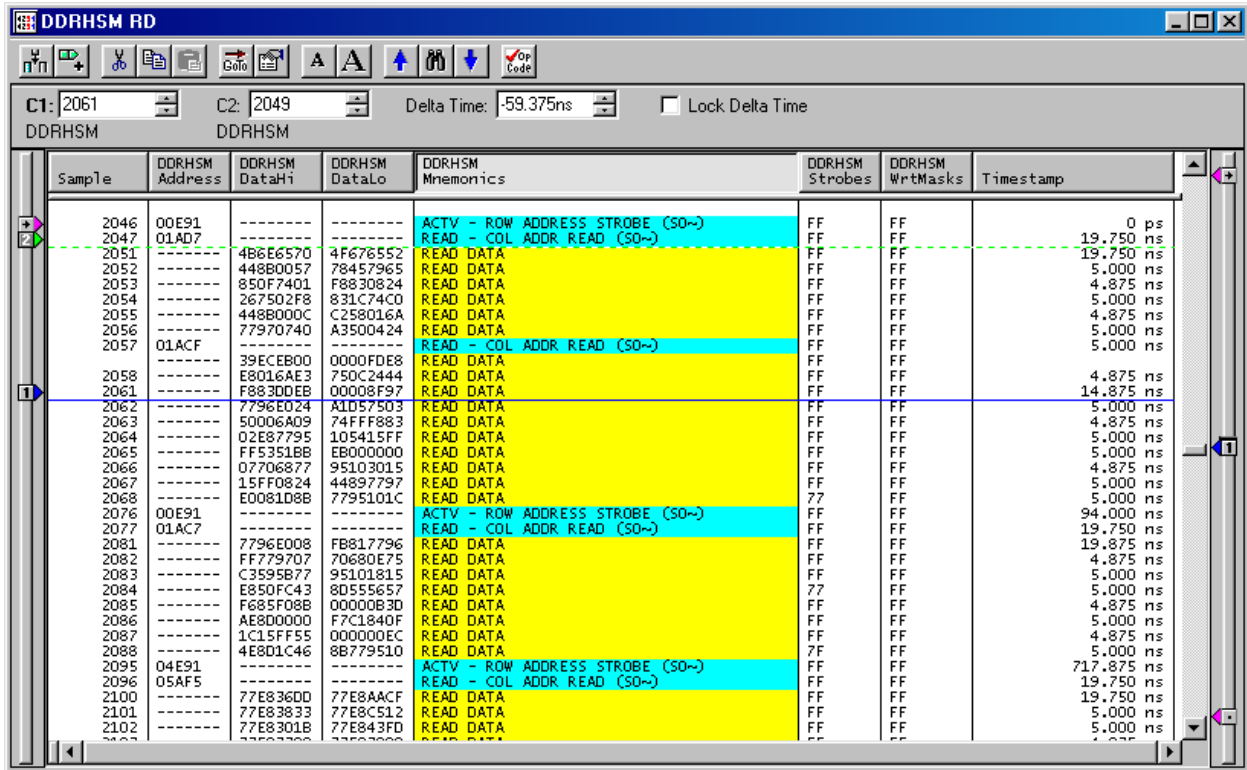


Figure 23- DDRHSM State Display - Show Control Flow; Valid Read Data

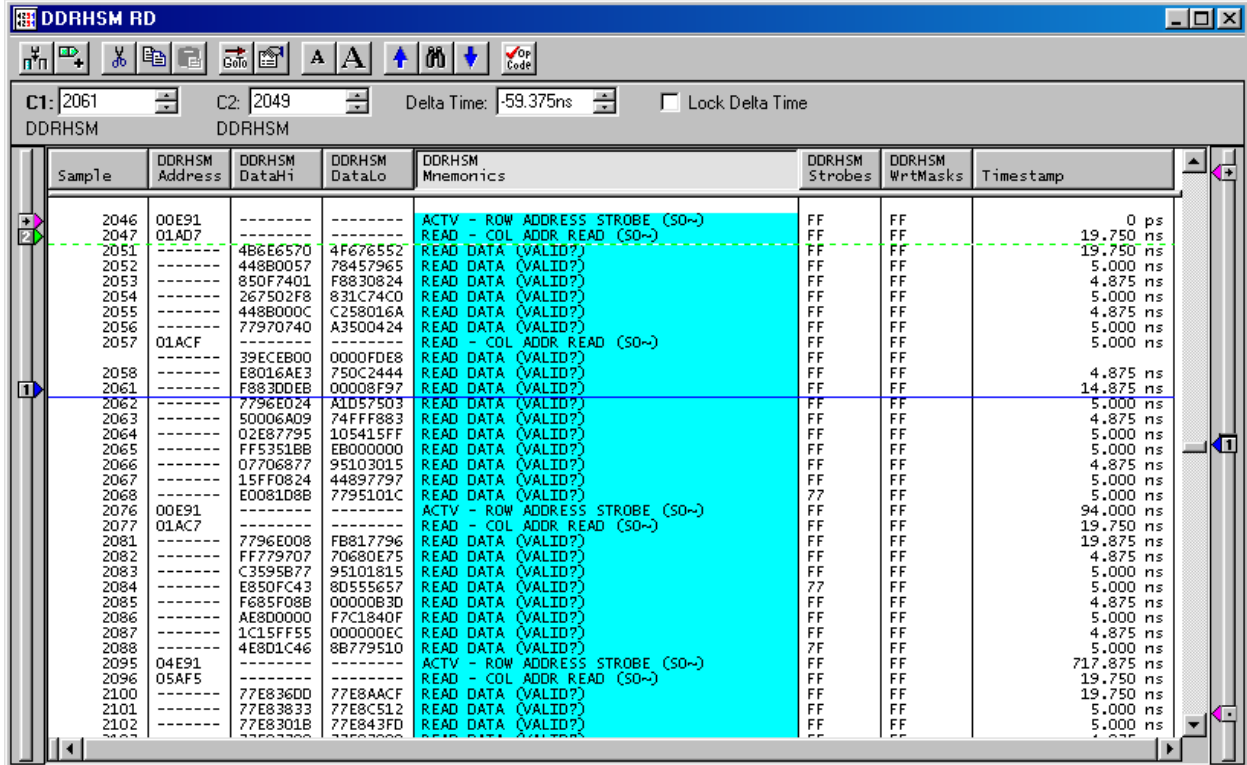


Figure 24- DDRHSM State Display - Show Control Flow; Valid Write Data Selected

6.3 Viewing DDRHSMRW Data

The DDRHSMRW support package displays the Address, RDDatHi, RDDatLo, WRDatHi, WRDatLo, WrtMsk, and Strobes group data in hexadecimal format; Command, ChekBits, Misc, and all sixteen Data Byte (RDDatBy*x* and WRDatBy*x*) groups default to OFF.

The Command group is suppressed because its function is replaced with a column labeled “DDRHSMRW Mnemonics”. The DDRHSMRW support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 25 shows the default display where all DDR data is displayed.

Sample	DDRHS-RW Address	DDRHS-RW RDDatHi	DDRHS-RW RDDatLo	DDRHS-RW WRDatHi	DDRHS-RW WRDatLo	DDRHS-RW Mnemonics	DDRHS-RW Strobes	DDRHS-RW WrtMasks	Command	Timestamp
2015	003C8	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11100	2,875 ns
2016	003C8	FEFF66E	E7FFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11100	3,000 ns
2017	003C8	6E4F64E	65706544	6E4F64E	65706544	DESL - IGNORE COMMAND	FF	00	11100	3,000 ns
2018	0044A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	38,875 ns
2019	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	REF - REFRESH (S0~)	FF	FF	10001	17,875 ns
2020	00000	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	ACTV - ROW ADDRESS STROBE (S0~)	FF	FF	10011	395,000 ns
2021	003D0	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	READ - COL ADDR READ (S0~)	FF	FF	10101	18,000 ns
2022	003D0	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	(UNKNOWN)	FF	FF	10101	2,875 ns
2023	003D4	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11101	3,125 ns
2024	003D4	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11101	2,875 ns
2025	003D4	F4FFFFF	FFFFFFF	FFFFFFF	FFFFFFF	READ - COL ADDR READ (S0~)	00	FF	10101	3,125 ns
2026	003D4	00000000	00000000	FFFFFFF	FFFFFFF	READ DATA	00	FF	10101	2,875 ns
2027	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	F9	11010	3,000 ns
2028	0004A	00000000	00000000	00000000	00000000	READ DATA	00	FF	11010	3,000 ns
2029	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	FF	11010	3,000 ns
2030	0004A	00000000	00000000	00000000	00000000	READ DATA	00	FF	11010	3,000 ns
2031	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	FF	11010	3,000 ns
2032	0004A	00000000	00000000	00000000	00000000	READ DATA	00	FF	11010	3,000 ns
2033	0004A	00000000	00000000	00000000	00000000	READ DATA	FF	FF	11010	3,000 ns
2034	0004A	FFFFFFF	7F3FFFF	00000000	00000000	DESL - IGNORE COMMAND	00	FF	11010	3,000 ns
2035	0004A	FFFFFFF	7F3FFFF	F6FFFFD8	08128C08	DESL - IGNORE COMMAND	02	FF	11010	3,000 ns
2036	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3,000 ns
2037	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3,000 ns
2038	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	2,875 ns
2039	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3,000 ns
2040	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3,125 ns
2041	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	2,875 ns
2042	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3,000 ns
2043	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	4,590,000 us
2044	0044A	00000000	00000000	00000000	00000000	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	731,625 ns
2045	0004A	FFFFFFF	FFFFFFF	FFFFFFF	3EC7DFDF	REF - REFRESH (S0~)	FF	FF	10001	17,875 ns
2046	00000	FFFFFFF	FFFFFFF	FFFFFFF	3E0320D5	ACTV - ROW ADDRESS STROBE (S0~)	FE	FF	10011	197,625 ns
2047	00088	006E0064	80BFFFF	FFFFFFF	FFFFFFF	WRITE - COL ADDR WRITE (S0~)	FF	FF	10100	18,000 ns
2048	00088	006E0064	00690061	006E0064	00690061	(UNKNOWN)	FF	00	10100	3,000 ns
2049	0008C	006E0064	00690061	006E0064	00690061	WRITE DATA	00	00	11100	3,000 ns
2050	0008C	00070000	00540000	00070000	00750061	WRITE DATA	FF	00	11100	2,875 ns
2051	0008C	000041B8	00070510	000041B8	00570510	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3,000 ns
2052	0008C	000043AC	000041A4	000043AC	000745B4	WRITE DATA	00	00	10100	3,000 ns
2053	00080	00003948	00003968	00003948	000079EC	WRITE DATA	FF	00	10100	3,000 ns
2054	00080	00004478	000043C8	00004478	000073E8	WRITE DATA	FF	00	11100	3,000 ns
2055	00080	00003B40	00003B50	00003B40	00007B08	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3,000 ns
2056	00080	00003B74	0000264C	00003B74	0000375C	WRITE DATA	FF	00	10100	3,000 ns
2057	00084	00003968	000043AC	00003968	000047EC	WRITE DATA	00	00	11100	3,000 ns
2058	00084	000043C8	00003948	000043C8	00003BCC	WRITE DATA	FF	00	11100	3,000 ns
2059	00084	000039F4	000043F4	000039F4	00007BFC	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3,000 ns
2060	00084	0000441C	000039DC	0000441C	00007BFC	WRITE DATA	FF	00	10100	3,000 ns
2061	004CE	000038A4	000038A4	000038A4	000038FC	WRITE DATA	00	00	11010	3,000 ns
2062	0044A	00420076	00000053	00420076	000038F7	WRITE DATA	FF	00	11010	2,875 ns
2063	0004A	00070528	00080002	00070528	00080053	WRITE DATA	00	00	11010	3,000 ns
2064	0004A	00720073	00070528	00720073	000F052A	WRITE DATA	FF	00	11010	3,125 ns
2065	0004A	FFFFFFF	FFFFFFF	0072017B	00070528	DESL - IGNORE COMMAND	00	00	11010	3,000 ns
2066	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	2,875 ns
2067	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3,000 ns
2068	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	DESL - IGNORE COMMAND	FF	FF	11010	3,000 ns
2069	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	PRE - PRECHARGE SELECT BANK (S0~)	FF	FF	10010	3,000 ns
2070	0004A	FFFFFFF	FFFFFFF	FFFFFFF	FFFFFFF	(UNKNOWN)	FF	FF	10010	3,000 ns

Figure 25- DDRHSMRW State Display - Show All Data? = Yes

To change the display it is necessary to bring up the window’s Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in Figure 26.

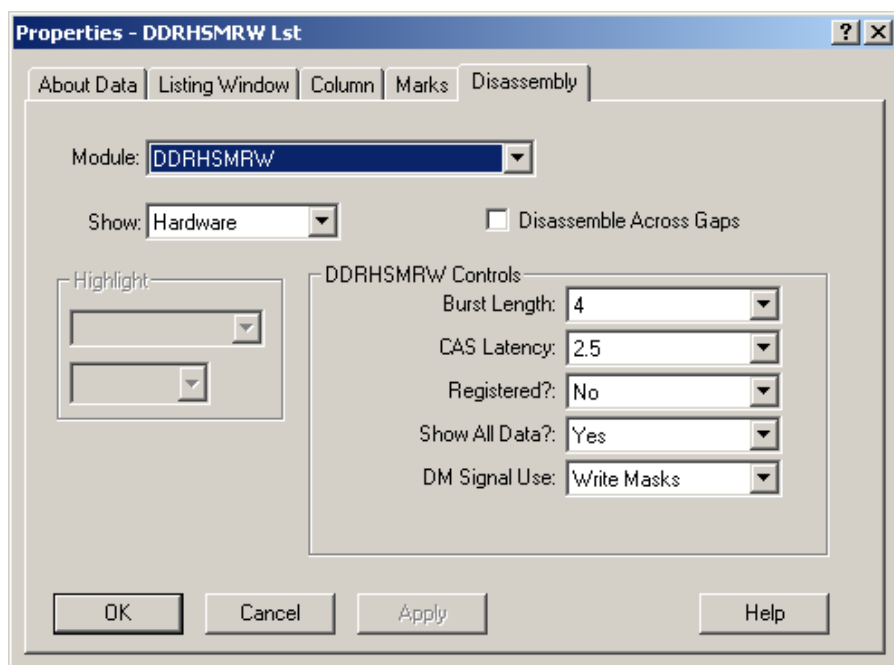


Figure 26- DDRHSMRW Disassembly Properties

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

Burst Length – permits setting the burst length for Read and Write data. Valid choices are 2 (the default), 4, and 8. This value must be set properly for all valid Read and Write data to be displayed.

CAS Latency – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 1.5 (default), 2.0, 2.5, and 3 cycles.

Registered? – must be set to reflect whether or not Registered DDR memory is used. Default is No. When set to Yes an additional clock cycle delay is added to the tagging of Read and Write data..

Show All Data? – permits choosing between displaying all DDR data (default), including Invalid Read / Write and Command data, and showing only valid Data and Command data.

DM Signal Use – permits setting Data Mask functionality to Write Masks (default) or Strobes. When set to Write Mask the DM signals will be used to mask Write Data to show which data bytes were valid in the cycle.

When setting **Show All Data?** to No, the display in Figure 25 then becomes the display in Figure 27. This allows the user to see at a glance the valid information on the bus.

Sample	DDRHS-RW Address	DDRHS-RW RDataHi	DDRHS-RW RDataLo	DDRHS-RW WDataHi	DDRHS-RW WDataLo	DDRHS-RW Mnemonics	DDRHS-RW Strobes	DDRHS-RW WrtMasks	Command	Timestamp
2015	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11100	2.875 ns
2016	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11100	3.000 ns
2017	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	00	11100	3.000 ns
2018	0044A	-----	-----	-----	-----	PRE - PRECHARGE SELECT BANK (SO~)	FF	FF	10010	38.875 ns
2019	0004A	-----	-----	-----	-----	REF - REFRESH (SO~)	FF	FF	10001	17.875 ns
2020	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (SO~)	FF	FF	10011	395.000 ns
2021	00300	-----	-----	-----	-----	READ - COL ADDR READ (SO~)	FF	FF	10101	18.000 ns
2022	-----	-----	-----	-----	-----	(UNKNOWN)	FF	FF	10101	2.875 ns
2023	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11101	3.125 ns
2024	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11101	2.875 ns
2025	00304	-----	-----	-----	-----	READ - COL ADDR READ (SO~)	00	FF	10101	3.125 ns
2026	00000000	00000000	-----	-----	-----	READ DATA	00	FF	10101	2.875 ns
2027	00000000	00000000	-----	-----	-----	READ DATA	FF	F9	11010	3.000 ns
2028	00000000	00000000	-----	-----	-----	READ DATA	00	FF	11010	3.000 ns
2029	00000000	00000000	-----	-----	-----	READ DATA	FF	FF	11010	3.000 ns
2030	00000000	00000000	-----	-----	-----	READ DATA	00	FF	11010	3.000 ns
2031	00000000	00000000	-----	-----	-----	READ DATA	FF	FF	11010	3.000 ns
2032	00000000	00000000	-----	-----	-----	READ DATA	00	FF	11010	3.000 ns
2033	00000000	00000000	-----	-----	-----	READ DATA	FF	FF	11010	3.000 ns
2034	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	FF	11010	3.000 ns
2035	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	C2	FF	11010	3.000 ns
2036	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2037	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2038	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	2.875 ns
2039	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2040	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	3.125 ns
2041	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	2.875 ns
2042	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2043	0004A	-----	-----	-----	-----	PRE - PRECHARGE SELECT BANK (SO~)	FF	FF	10010	4.590,000 us
2044	0044A	-----	-----	-----	-----	PRE - PRECHARGE SELECT BANK (SO~)	FF	FF	10010	731.625 ns
2045	0004A	-----	-----	-----	-----	REF - REFRESH (SO~)	FF	FF	10001	17.875 ns
2046	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (SO~)	FE	FF	10011	197.625 ns
2047	00088	-----	-----	-----	-----	WRITE - COL ADDR WRITE (SO~)	FF	FF	10100	18.000 ns
2048	-----	-----	-----	-----	-----	(UNKNOWN)	FF	00	10100	3.000 ns
2049	-----	-----	006E0064	00690061	-----	WRITE DATA	00	00	11100	3.000 ns
2050	-----	-----	00070000	00750061	-----	WRITE DATA	FF	00	11100	2.875 ns
2051	0008C	-----	-----	-----	-----	WRITE - COL ADDR WRITE (SO~)	00	00	10100	3.000 ns
2052	-----	-----	000041B8	00570E10	-----	WRITE DATA	00	00	10100	3.000 ns
2053	-----	-----	0000438C	000745B4	-----	WRITE DATA	FF	00	11100	3.000 ns
2054	-----	-----	00003948	000079EC	-----	WRITE DATA	00	00	11100	3.000 ns
2055	00080	-----	-----	00004478	000073E8	WRITE DATA	FF	00	11100	3.000 ns
2056	-----	-----	00003840	00007B08	-----	WRITE - COL ADDR WRITE (SO~)	00	00	10100	3.000 ns
2057	-----	-----	00003874	0000375C	-----	WRITE DATA	00	00	10100	3.000 ns
2058	-----	-----	00003968	000047EC	-----	WRITE DATA	00	00	11100	3.000 ns
2059	00084	-----	-----	000043C8	00003BCC	WRITE DATA	FF	00	11100	3.000 ns
2060	-----	-----	000039F4	00007BFC	-----	WRITE - COL ADDR WRITE (SO~)	00	00	10100	3.000 ns
2061	-----	-----	0000441C	000078FC	-----	WRITE DATA	FF	00	10100	3.000 ns
2062	-----	-----	000038A4	000038FC	-----	WRITE DATA	00	00	11010	3.000 ns
2063	-----	-----	00420076	000038F7	-----	WRITE DATA	FF	00	11010	2.875 ns
2064	-----	-----	00070568	00080053	-----	WRITE DATA	00	00	11010	3.000 ns
2065	-----	-----	00720073	000F052A	-----	WRITE DATA	FF	00	11010	3.125 ns
2066	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	00	00	11010	3.000 ns
2067	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	2.875 ns
2068	-----	-----	-----	-----	-----	DESL - IGNORE COMMAND	FF	FF	11010	3.000 ns
2069	0004A	-----	-----	-----	-----	PRE - PRECHARGE SELECT BANK (SO~)	FF	FF	10010	3.000 ns
2070	-----	-----	-----	-----	-----	(UNKNOWN)	FF	FF	10010	3.000 ns

Figure 27- DDRHSMRW State Display - Show All Data? = No

In addition to the Disassembly Properties selections discussed earlier, changing the settings in the **Show** field result in display changes as well:

Hardware – displays all acquired cycles

Software – suppresses all idle or wait cycles

Control Flow – shows Address Command and valid Read / Write data cycles

Subroutine – shows valid Read / Write data cycles only

Changing the Show field setting in the display of Figure 27 from Hardware to Control Flow results in the display of Figure 28 where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

Sample	DDRHS-RW Address	DDRHS-RW RDDatHi	DDRHS-RW RDDatLo	DDRHS-RW WRDatHi	DDRHS-RW WRDatLo	DDRHS-RW Mnemonics	DDRHS-RW Strobes	DDRHS-RW WrtMasks	Command	Timestamp
1993	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10101	3,000 ns
1994	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11101	3,000 ns
1995	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11101	3,000 ns
1996	003C8	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	FF	FF	10101	3,000 ns
1997	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10101	3,000 ns
1998	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11101	3,000 ns
1999	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11101	3,000 ns
2000	003CC	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	FF	FF	10101	3,000 ns
2001	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10101	2,875 ns
2002	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2003	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11010	3,000 ns
2004	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	10010	3,000 ns
2005	-----	00000000	00000000	-----	-----	READ DATA	00	FF	10010	3,000 ns
2006	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11011	3,000 ns
2007	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11011	3,000 ns
2008	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11011	3,000 ns
2020	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	FF	FF	10011	478,500 ns
2021	003D0	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	FF	FF	10101	18,000 ns
2025	003D4	-----	-----	-----	-----	READ - COL ADDR READ (S0~)	00	FF	10101	12,000 ns
2026	-----	00000000	00000000	-----	-----	READ DATA	00	FF	10101	2,875 ns
2027	-----	00000000	00000000	-----	-----	READ DATA	FF	F9	11010	3,000 ns
2028	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11010	3,000 ns
2029	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2030	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11010	3,000 ns
2031	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2032	-----	00000000	00000000	-----	-----	READ DATA	00	FF	11010	3,000 ns
2033	-----	00000000	00000000	-----	-----	READ DATA	FF	FF	11010	3,000 ns
2046	00000	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	FE	FF	10011	5,564,000 ns
2047	00088	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	FF	FF	10100	18,000 ns
2049	-----	-----	-----	006E0064	00690061	WRITE DATA	00	00	11100	6,000 ns
2050	-----	-----	-----	00070000	00750061	WRITE DATA	00	00	11100	2,875 ns
2051	0008C	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	FF	00	10100	3,000 ns
2052	-----	-----	-----	00004188	00570510	WRITE DATA	00	00	10100	3,000 ns
2053	-----	-----	-----	000043AC	000745B4	WRITE DATA	FF	00	10100	3,000 ns
2054	-----	-----	-----	00003948	000079EC	WRITE DATA	00	00	11100	3,000 ns
2055	00080	-----	-----	00004478	000073E8	WRITE DATA	FF	00	11100	3,000 ns
2056	-----	-----	-----	00003840	000078D8	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3,000 ns
2057	-----	-----	-----	00003874	0000375C	WRITE DATA	FF	00	10100	3,000 ns
2058	-----	-----	-----	00003968	000047EC	WRITE DATA	00	00	11100	3,000 ns
2059	00084	-----	-----	000043C8	000038CC	WRITE DATA	FF	00	11100	3,000 ns
2060	-----	-----	-----	000039F4	000078FC	WRITE - COL ADDR WRITE (S0~)	00	00	10100	3,000 ns
2061	-----	-----	-----	0000441C	000078FC	WRITE DATA	FF	00	10100	3,000 ns
2062	-----	-----	-----	000038A4	000038FC	WRITE DATA	00	00	11010	3,000 ns
2063	-----	-----	-----	00420076	000038F7	WRITE DATA	FF	00	11010	2,875 ns
2064	-----	-----	-----	00070568	00060053	WRITE DATA	00	00	11010	3,000 ns
2077	00000	-----	-----	00720073	000F052A	WRITE DATA	FF	00	11010	3,125 ns
2078	00088	-----	-----	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	7F	FF	10011	116,750 ns
2080	-----	-----	-----	00000000	005D0050	WRITE - COL ADDR WRITE (S0~)	FF	FF	10100	18,000 ns
2081	-----	-----	-----	00000000	005D0050	WRITE DATA	00	00	11100	6,000 ns
2082	0008C	-----	-----	-----	-----	WRITE - COL ADDR WRITE (S0~)	FF	00	11100	3,000 ns
2083	-----	-----	-----	00000000	00000000	WRITE DATA	00	00	10100	3,000 ns
2084	-----	-----	-----	00000000	00000000	WRITE DATA	FF	00	11100	3,000 ns

Figure 28- DDRHSMRW State Display - Show Control Flow

6.4 DDRHSMRW Mnemonics Description

Table 4 gives a brief description of each of the text lines displayed in the post-processing software display.

Mnemonic	Description
ACTV - ROW ADDRESS STROBE (S0~)	Active command – activate a row in a bank for subsequent access (chip select 0)
ACTV - ROW ADDRESS STROBE (S1~)	Active command – activate a row in a bank for subsequent access (chip select 1)
BST - BURST STOP (S0~)	Burst Terminate command – truncate current Read burst (chip select 0)
BST - BURST STOP (S1~)	Burst Terminate command – truncate current Read burst (chip select 1)
DESL - IGNORE COMMAND	Deselect function – no new command
MRS - MODE REGISTER SET (S0~)	Mode Register Set command – mode register load (chip select 0)
MRS - MODE REGISTER SET (S1~)	Mode Register Set command – mode register load (chip select 1)
NOP - NO OPERATION (S0~)	No Operation command (chip select 0)
NOP - NO OPERATION (S1~)	No Operation command (chip select 1)
PRE - PRECHARGE SELECT BANK (S0~)	Precharge command (chip select 0)
PRE - PRECHARGE SELECT BANK (S1~)	Precharge command (chip select 1)
READ - COL ADDR READ (S0~)	Read command – initiates a burst read access to active row (chip select 0)
READ - COL ADDR READ (S1~)	Read command – initiates a burst read access to active row (chip select 1)
READ DATA	Valid Read data on the bus
REF - REFRESH (S0~)	Self Refresh command (chip select 0)
REF - REFRESH (S1~)	Self Refresh command (chip select 1)
WRITE - COL ADDR WRITE (S0~)	Write command – initiates a burst write access to active row (chip select 0)
WRITE - COL ADDR WRITE (S1~)	Write command – initiates a burst write access to active row (chip select 1)
WRITE DATA	Valid Write data on the bus
DDRCK0, DDRCK1, & DDRCK2	No active clock detected by software
INACTIVE	
(UNKNOWN)	Command Cycle on falling edge of clock

Table 4- DDRHSM / DDRHSMRW Mnemonics Definition

6.5 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: DDRHSM (or DDRHSMRW) and DDRHSM-MagniVu (or DDRHSMRW-MagniVu). The first (DDRHSM or DDRHSMRW) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, DDRHSM-MagniVu (or DDRHSMRW-MagniVu), will show all of the channels in 8GHz MagniVu mode, so that edge relationships can be examined around the MagniVu trigger point. MagniVu is very useful and in some cases necessary to see/resolve DDR data. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

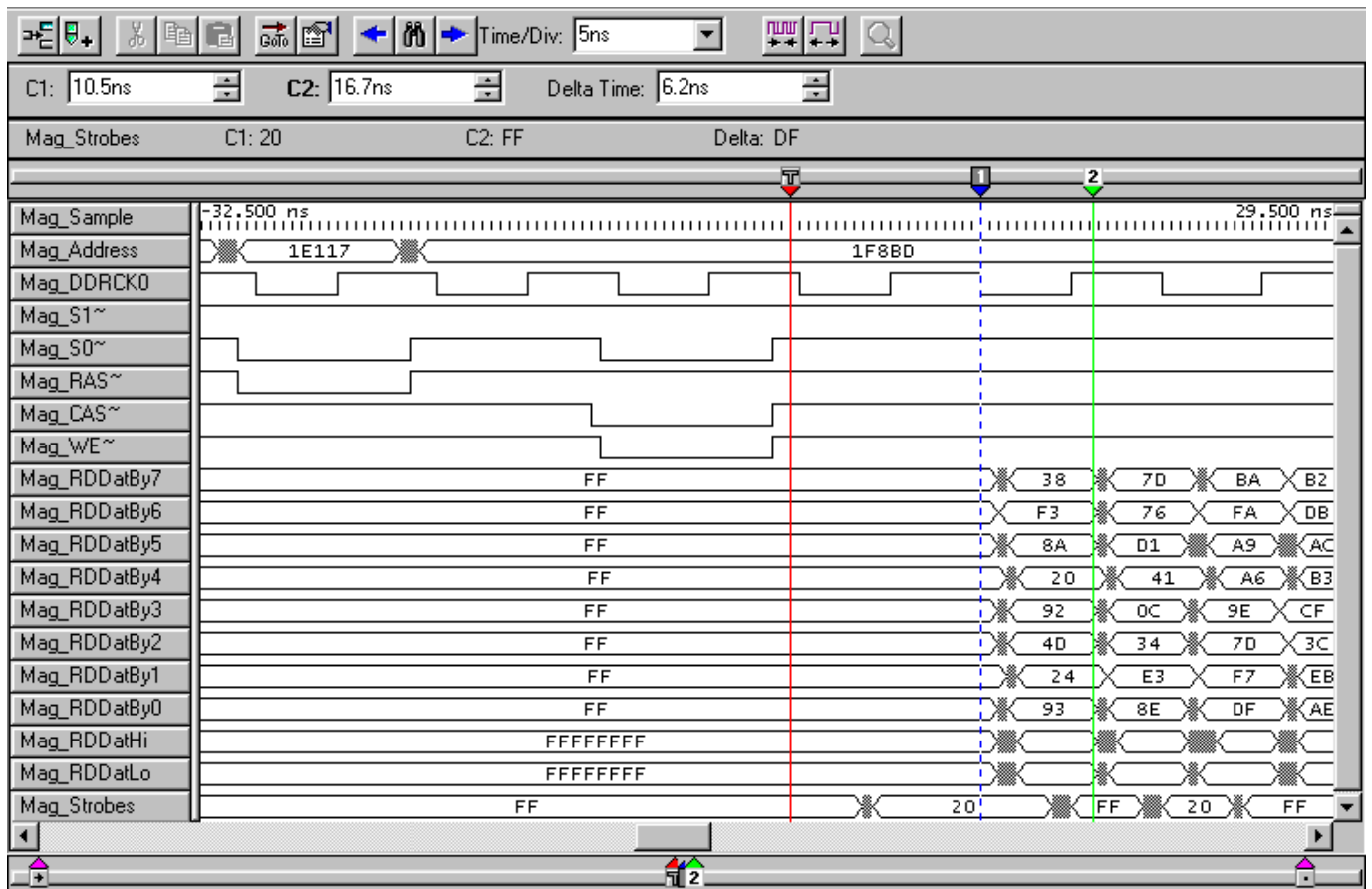


Figure 29- DDRHSM MagniVu Display on TLA

7.0 HINTS & TIPS

7.1 Triggering on a Command using DDRHSM or DDRHSMRW

The DDRHSM and DDRHSMRW support packages clock data into the logic analyzer on both the rising and falling edges of the selected DDR Clock. Command information is only valid on the rising edge of the clock, but it is very possible (even likely) that valid information is also available on the falling edge of the clock preceding the Command's valid rising edge. This can result in a false trigger of the TLA. With the DDRHSMRW post-processing software such a cycle (falling edge of DDR Clock with valid Command data) is labeled as an Unknown cycle. These cycles would be filtered out (suppressed) when changing the Disassembly Properties display mode to something other than Hardware, resulting in a Trigger position that is hidden from the user.

To eliminate this problem it is suggested that a trigger condition be defined that ANDs the desired Command with the DDR Clock channel being used for acquisition in a LOW state (see Figure 30). (Since the data stored by the TLA reflects its state before the acquisition clock occurs the DDR Clock is stored as a LOW for a rising clock edge and as a HIGH for a falling clock edge.) Figure 31 shows the actual Trigger Clause definition used in the trigger program shown in Figure 30.

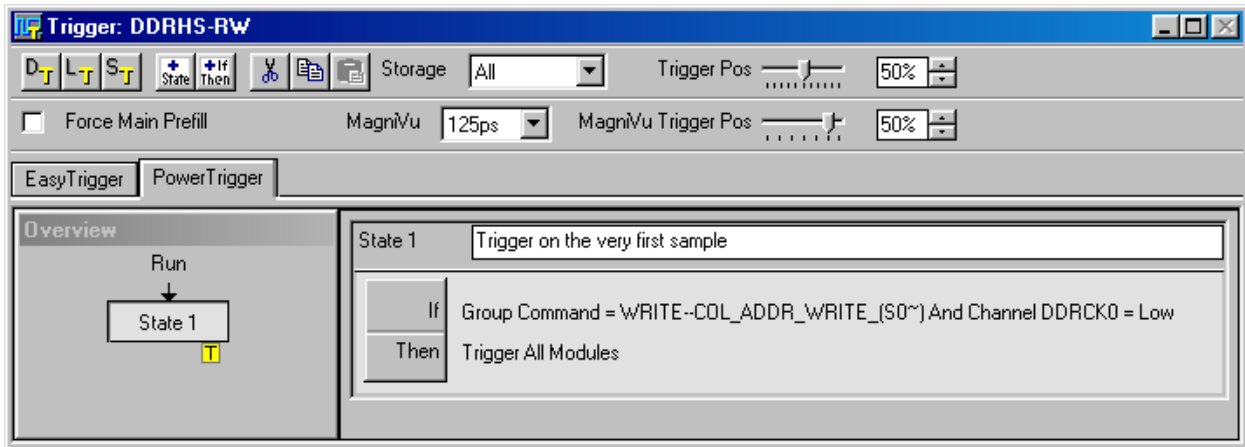


Figure 30- Recommended DDRHSM / DDRHSMRW Command Trigger

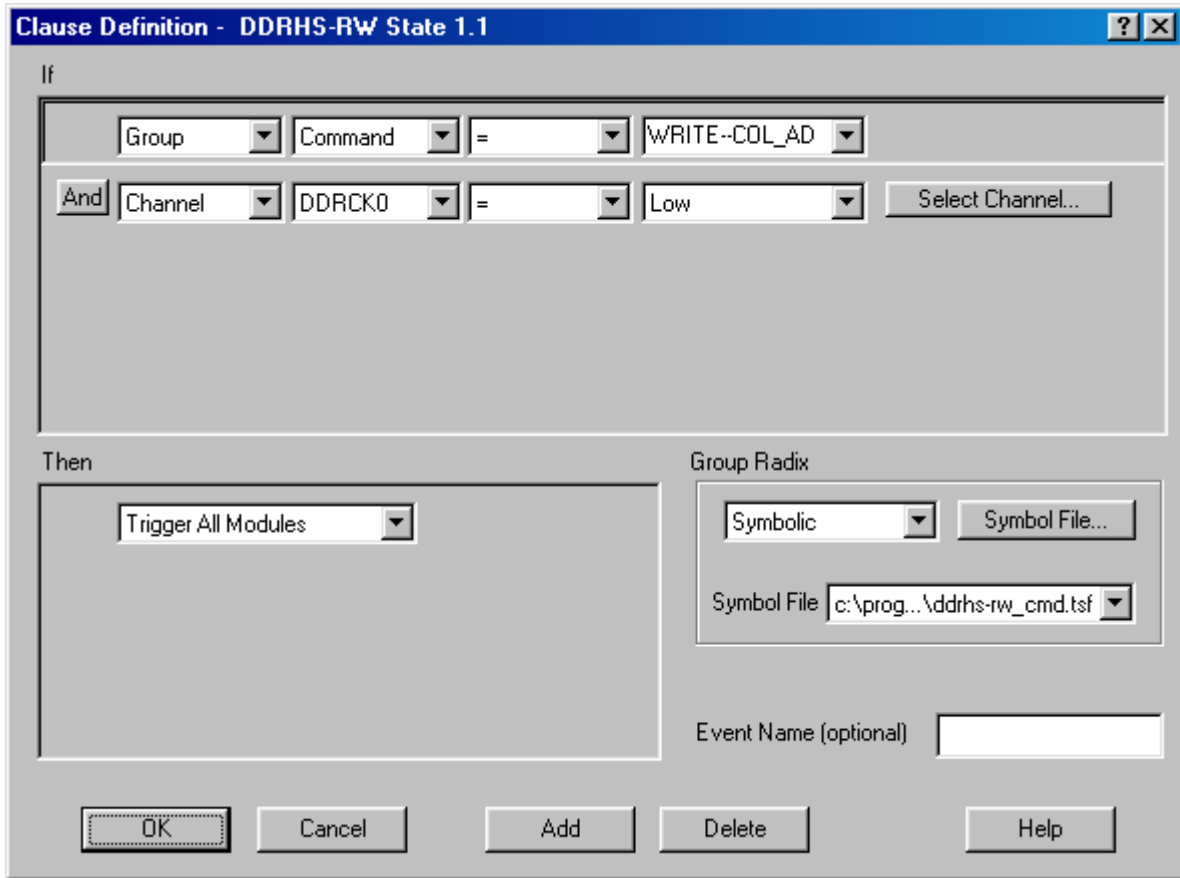


Figure 31- Recommended DDRHSM Command Trigger - Detail

7.2 Capturing MRS (Mode Register Set) Data

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the DDRHSM and DDRHSMRW supports for the post-processing software to properly decode the acquisitions. The TLA trigger shown in Figure 32 can be used to acquire the MRS cycles when using these supports.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

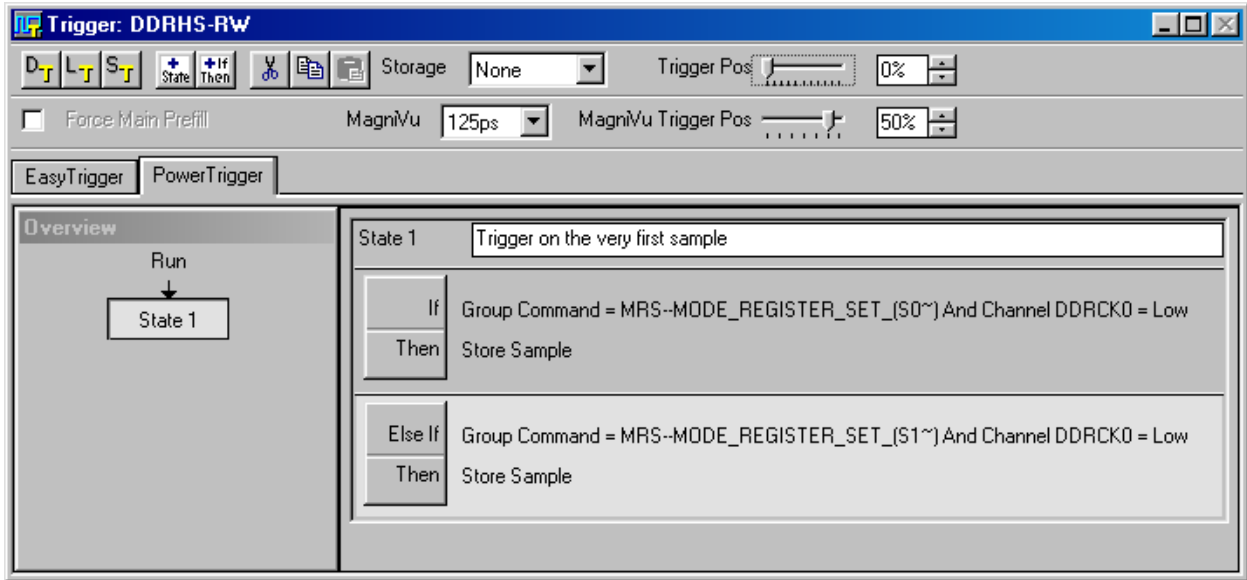


Figure 32- DDRHS / DDRHSMRW MRS Trigger

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in Figure 33. The last acquired MRS cycle will reflect the settings used in the DDR target – in this case, a CAS latency of 2 cycles with a Burst length of 8.

Sample	DDRHSMRW Address	DDRHSMRW R0DatHi	DDRHSMRW R0DatLo	DDRHSMRW WRDatHi	DDRHSMRW WRDatLo	DDRHSMRW Mnemonics	D	S
88	0002B	-----	-----	-----	-----	MRS - MODE REGISTER SET (S0~)	F	F
	0002B	-----	-----	-----	-----	Normal MRS	F	F
	0002B	-----	-----	-----	-----	Normal Operation	F	F
	0002B	-----	-----	-----	-----	Latency = 2	F	F
	0002B	-----	-----	-----	-----	Burst Type = Interleaved	F	F
	0002B	-----	-----	-----	-----	Burst Length = 8	F	F
89	04000	-----	-----	-----	-----	MRS - MODE REGISTER SET (S0~)	F	F
	04000	-----	-----	-----	-----	Reserved	F	F
90	00400	-----	-----	-----	-----	MRS - MODE REGISTER SET (S0~)	F	F
	00400	-----	-----	-----	-----	Normal MRS	F	F
	00400	-----	-----	-----	-----	Operating Mode = Reserved	F	F
	00400	-----	-----	-----	-----	Latency = Reserved	F	F
	00400	-----	-----	-----	-----	Burst Type = Sequential	F	F
	00400	-----	-----	-----	-----	Burst Length = Reserved	F	F
91	0002B	-----	-----	-----	-----	MRS - MODE REGISTER SET (S0~)	F	F
	0002B	-----	-----	-----	-----	Normal MRS	F	F
	0002B	-----	-----	-----	-----	Normal Operation	F	F
	0002B	-----	-----	-----	-----	Latency = 2	F	F
	0002B	-----	-----	-----	-----	Burst Type = Interleaved	F	F
	0002B	-----	-----	-----	-----	Burst Length = 8	F	F

Figure 33- MRS Cycle Acquisition Disassembly

APPENDIX A - How DDR Data is Clocked

A.1 Background

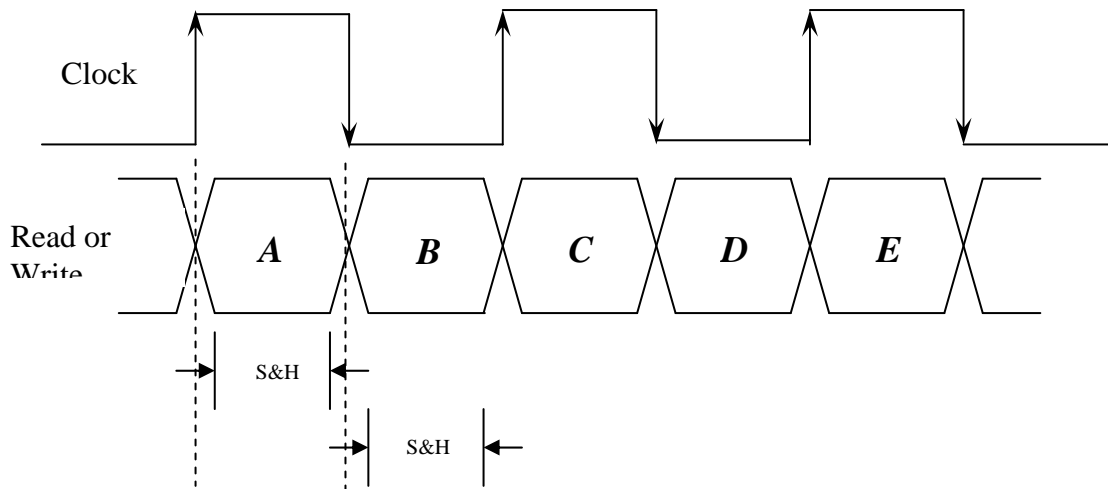
Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section *and* the D3 section. Through the User Interface of the TLA, demux can be performed by connecting the A0-A3 sections and storing the data in both the A0-A3 and D0-D3 data sections. More extensive demux capabilities are possible using the software tools that were used to create the various DDR packages. A very useful side benefit of using demux is that, since only one set of TLA data channels have to be connected, only one probe load is added to the target, even though data is stored in two different locations of the acquisition card.

A.2 DDR Acquisition - General

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. The speeds of DDR (200, 266, and 400MHz) require different setups to enable proper data acquisition. In addition, instead of trying to use the 8 Data Strokes to acquire data our solution uses one of the DDR SDRAM Clocks (either CK0 or CK1, user selectable) and all data acquisition is adjusted in relation to the clock edges. The 8 Data Strokes cannot be easily used to acquire data as some TLA configurations only support 4 Clock Inputs. Also, the Strokes cannot be used to acquire Address and Command information.

A.3 DDRHSM Support

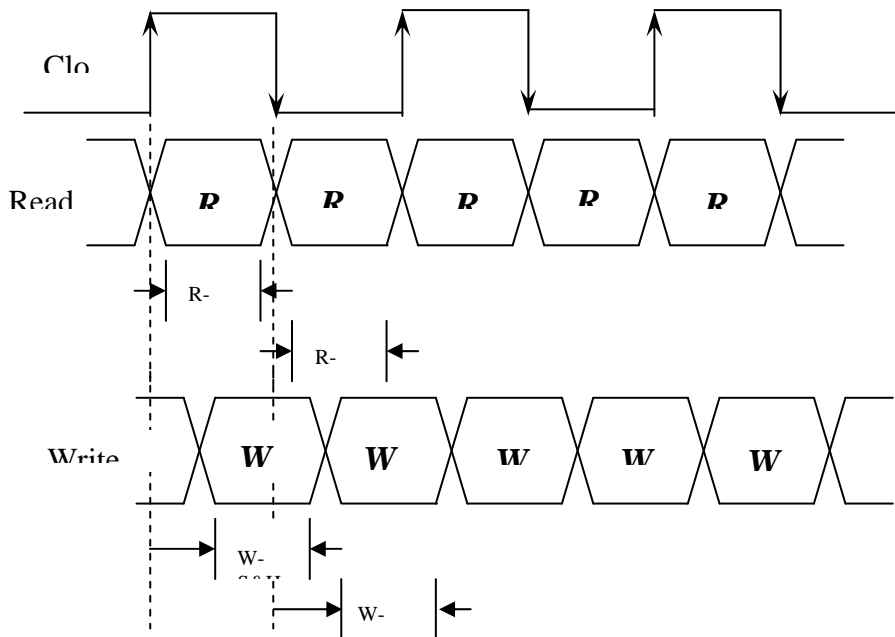
This support requires a single 450MHz 136-channel TLA7AA4 or TLA7AB4 acquisition card. Because of the speed and channel count requirements only Read or Write data can be acquired during a single acquisition. Data is acquired on every edge of the DDR clock, and demultiplexing of the data is not done. Typical usage requires setting the Sample Point only for the DataHi and DataLo groups. However, if unusually large skews exist between some of the Data Strokes and their associated groups, then Sample Points can be set for each of the 8 Data groups (DatByte0-7) so that valid data acquisition can be assured. It is important to note that setting Sample Points (termed Setup & Hold points in the TLA) on any of the individual data groups (DatByte0-7) will override any adjustments made to the overall data groups (DataHi and DataLo).



Sample	DDR200 Address	DDR200 DataHi	DDR200 DataLo	DDR200 Mnemonics	Strobes	Timestamp
149	1927F	FFFFFFFF	FFFFFFFF	(ROW ACTIVE)	FF	4.500 ns
150	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.500 ns
151	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	4.500 ns
152	180F1	FFFFFFFF	FFFFFFFF	(COLUMN ACTIVE - READ)	FF	5.500 ns
153	180F1	FFFFFFFF	FFFFFFFF	(COLUMN ACTIVE - READ)	FF	5.000 ns
154	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.000 ns
155	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.000 ns
156	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	00	5.000 ns
157	10011	FE7BEFB6	CB0C71C6	(DESELECT (NOP))	00	5.000 ns
158	10011	B6DAEBAE	B2DF6DF7	(DESELECT (NOP))	FF	5.000 ns
159	10011	A259A492	4D34D36D	(DESELECT (NOP))	00	4.500 ns
160	10011	2470C38E	38E78E28	(DESELECT (NOP))	FF	5.500 ns
161	10011	BA79E7DF	7DF5D345	(DESELECT (NOP))	00	5.000 ns
162	10011	EF7CE3AE	BAEEA8A6	(DESELECT (NOP))	FF	5.000 ns
163	10011	E9708A28	A2CF2CB2	(DESELECT (NOP))	00	4.500 ns
164	10011	28F28E38	F3CF3CF2	(DESELECT (NOP))	FF	5.500 ns
165	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	00	5.000 ns
166	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.000 ns
167	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	4.500 ns
168	18411	FFFFFFFF	FFFFFFFF	(PRECHARGE)	FF	5.500 ns

A.4 DDRHSMRW Support

This support requires two (2) merged 136-channel 450MHz TLA7AA4 or TLA7AB4 acquisition cards used in a TLA7XX. The merged cards enable both Read and Write data to be acquired simultaneously from a DDR system. Data is acquired using both edges of the DDR clock, and demultiplexing is done to permit acquiring both Read and Write data on every clock edge. One Sample Point must be adjusted to acquire valid Read data in reference to the clock edge; a second Sample Point must be set to acquire valid Write data in relation to the edge. Again, different Sample Points must be set for each of the Read / Write data groups (RDDatHi, RDDatLo, WRDatHi, and WRDatLo), and if necessary, sample points can be set for any of the 8-bit data groups.



Sample	Address	RDDatHi	RDDatLo	WRDatHi	WRDatLo	Command	Strobes	Timestamp
19	10011	20528000	008E0000	20528000	00070000	DESL--IGNORE_COMMAND--DATA?	20	-25.000 ns
20	142F3	20528004	0DCE0000	20528000	0DCE0000	ACTV--ROW_ADDRESS_STROBE_(SO~)	2C	-19.500 ns
21	142F3	20528004	0C460000	20528004	0DCE0000	ACTV--ROW_ADDRESS_STROBE_(SO~)	2C	-15.000 ns
22	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	-9.500 ns
23	10011	20528000	010C0000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	-5.000 ns
24	14031	2052800C	050C0000	20528000	050C0000	READ--COL_ADDR_READ_(SO~)	20	0 ps
25	14031	20528008	040C0000	2052800C	050C0000	READ--COL_ADDR_READ_(SO~)	28	5.000 ns
26	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	10.500 ns
27	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	15.000 ns
28	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	20.500 ns
29	10011	20D38C30	C30C20A2	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	25.000 ns
30	10011	2C528082	08248208	20D38C30	C30C20A2	DESL--IGNORE_COMMAND--DATA?	B4	30.500 ns
31	10011	7D77F7DF	FFDF3C7	2C528082	08248208	DESL--IGNORE_COMMAND--DATA?	60	35.500 ns
32	10011	BA739659	65155555	7D77F7DF	FFDF3C7	DESL--IGNORE_COMMAND--DATA?	FF	40.000 ns
33	10011	2FAEBBE	FBAE39E7	BA739659	65155555	DESL--IGNORE_COMMAND--DATA?	20	45.000 ns
34	10011	E3DE84D3	4D3492C8	2FAEBBE	FBAE39E7	DESL--IGNORE_COMMAND--DATA?	FF	50.500 ns
35	10011	FBFFBCF7	DF6D9618	E3DE84D3	4D3492C8	DESL--IGNORE_COMMAND--DATA?	20	55.500 ns
36	10011	A6DBEDB4	D75D65B6	FBFFBCF7	DF6D9618	DESL--IGNORE_COMMAND--DATA?	3C	60.500 ns
37	10011	A252A1B4	00044482	A6DBEDB4	D75D65B6	DESL--IGNORE_COMMAND--DATA?	20	65.000 ns
38	10011	AEDBADB6	0E0761B6	A6DBEDB4	D75D65B6	DESL--IGNORE_COMMAND--DATA?	20	70.500 ns
39	10011	A8D2AC30	08040010	AEDBADB6	0E0761B6	DESL--IGNORE_COMMAND--DATA?	21	75.000 ns
40	10011	2652A024	00054010	A0D2A030	00040010	PRE--PRECHARGE_SELECT_BANK_(SO~)	20	80.000 ns
41	14411	24528004	08044010	2652A024	08054010	PRE--PRECHARGE_SELECT_BANK_(SO~)	20	85.000 ns
42	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	90.500 ns
43	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	95.000 ns
44	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	22	100.500 ns

APPENDIX B - Considerations

B.1 DDRHS Bus Loading

It must be noted that the NEX-DDRHSM Bus Adapter does not provide any buffering of the DDR memory signals. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using this adapter, to see the exact timing relationships and signal waveforms from the system. It is important to note that the NEX-DDRHSM is an impedance controlled, matched trace length design. This adds greatly to its ability to maintain signal integrity and timing relationships of the DDR bus.

APPENDIX C - DDR DIMM 184-pin Pinout

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 - 144, right side 145 - 184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 - 144, right side 145 - 184)		
Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	X64 Non-Parity	x72 ECC	Pin #	X64 Non-Parity	x72 ECC
1	V _{REF}	V _{REF}	93	V _{SS}	V _{SS}	48	A0	A0	140	NC	DM8,DQS17
2	DQ0	DQ0	94	DQ4	DQ4	49	NC	CB2	141	A10	A10
3	V _{SS}	V _{SS}	95	DQ5	DQ5	50	V _{SS}	V _{SS}	142	NC	CB6
4	DQ1	DQ1	96	V _{DDQ}	V _{DDQ}	51	NC	CB3	143	V _{DDQ}	V _{DDQ}
5	DQS0	DQS0	97	DM0,DQS9	DM0,DQS9	52	BA1	BA1	144	NC	CB7
6	DQ2	DQ2	98	DQ6	DQ6	KEY			KEY		
7	VDD	VDD	99	DQ7	DQ7	53	DQ32	DQ32	145	V _{SS}	V _{SS}
8	DQ3	DQ3	100	V _{SS}	V _{SS}	54	V _{DDQ}	V _{DDQ}	146	DQ36	DQ36
9	NC	NC	101	NC	NC	55	DQ33	DQ33	147	DQ37	DQ37
10	RESET/	RESET/	102	NC	NC	56	DQS4	DQS4	148	V _{DD}	V _{DD}
11	V _{SS}	V _{SS}	103	NC	NC	57	DQ34	DQ34	149	DM4,DQS13	DM4,DQS13
12	DQ8	DQ8	104	V _{DDQ}	V _{DDQ}	58	V _{SS}	V _{SS}	150	DQ38	DQ38
13	DQ9	DQ9	105	DQ12	DQ12	59	BA0	BA0	151	DQ39	DQ39
14	DQS1	DQS1	106	DQ13	DQ13	60	DQ35	DQ35	152	V _{SS}	V _{SS}
15	V _{DDQ}	V _{DDQ}	107	DM1,DQS10	DM1,DQS10	61	DQ40	DQ40	153	DQ44	DQ44
16	NC (CK1)	NC (CK1)	108	V _{DD}	V _{DD}	62	V _{DDQ}	V _{DDQ}	154	RAS/	RAS/
17	NC (CK1/)	NC (CK1/)	109	DQ14	DQ14	63	WE/	WE/	155	DQ45	DQ45
18	V _{SS}	V _{SS}	110	DQ15	DQ15	64	DQ41	DQ41	156	V _{DDQ}	V _{DDQ}
19	DQ10	DQ10	111	CKE1	CKE1	65	CAS/	CAS/	157	S0/	S0/
20	DQ11	DQ11	112	V _{DDQ}	V _{DDQ}	66	V _{SS}	V _{SS}	158	S1/	S1/
21	CKE0	CKE0	113	NC,BA2	NC,BA2	67	DQS5	DQS5	159	DM5,DQS14	DM5,DQS14
22	V _{DDQ}	V _{DDQ}	114	DQ20	DQ20	68	DQ42	DQ42	160	V _{SS}	V _{SS}
23	DQ16	DQ16	115	A12,NC	A12,NC	69	DQ43	DQ43	161	DQ46	DQ46
24	DQ17	DQ17	116	V _{SS}	V _{SS}	70	V _{DD}	V _{DD}	162	DQ47	DQ47
25	DQS2	DQS2	117	DQ21	DQ21	71	NC, S2/	NC, S2/	163	NC, S3/	NC, S3/
26	V _{SS}	V _{SS}	118	A11	A11	72	DQ48	DQ48	164	V _{DDQ}	V _{DDQ}
27	A9	A9	119	DM2,DQS11	DM2,DQS11	73	DQ49	DQ49	165	DQ52	DQ52
28	DQ18	DQ18	120	V _{DD}	V _{DD}	74	V _{SS}	V _{SS}	166	DQ53	DQ53
29	A7	A7	121	DQ22	DQ22	75	NC (CK2/)	NC (CK2/)	167	NC, A13	NC, A13
30	V _{DDQ}	V _{DDQ}	122	A8	A8	76	NC (CK2)	NC (CK2)	168	V _{DD}	V _{DD}
31	DQ19	DQ19	123	DQ23	DQ23	77	V _{DDQ}	V _{DDQ}	169	DM6,DQS15	DM6,DQS15
32	A5	A5	124	V _{SS}	V _{SS}	78	DQS6	DQS6	170	DQ54	DQ54
33	DQ24	DQ24	125	A6	A6	79	DQ50	DQ50	171	DQ55	DQ55
34	V _{SS}	V _{SS}	126	DQ28	DQ28	80	DQ51	DQ51	172	V _{DDQ}	V _{DDQ}
35	DQ25	DQ25	127	DQ29	DQ29	81	V _{SS}	V _{SS}	173	NC	NC
36	DQS3	DQS3	128	V _{DDQ}	V _{DDQ}	82	V _{DDID}	V _{DDID}	174	DQ60	DQ60
37	A4	A4	129	DM3,DQS12	DM3,DQS12	83	DQ56	DQ56	175	DQ61	DQ61
38	V _{DD}	V _{DD}	130	A3	A3	84	DQ57	DQ57	176	V _{SS}	V _{SS}
39	DQ26	DQ26	131	DQ30	DQ30	85	V _{DD}	V _{DD}	177	DM7,DQS16	DM7,DQS16
40	DQ27	DQ27	132	V _{SS}	V _{SS}	86	DQS7	DQS7	178	DQ62	DQ62
41	A2	A2	133	DQ31	DQ31	87	DQ58	DQ58	179	DQ63	DQ63
42	V _{SS}	V _{SS}	134	NC	CB4	88	DQ59	DQ59	180	V _{DDQ}	V _{DDQ}
43	A1	A1	135	NC	CB5	89	V _{SS}	V _{SS}	181	SA0	SA0
44	NC	CB0	136	V _{DDQ}	V _{DDQ}	90	NC	NC	182	SA1	SA1
45	NC	CB1	137	CK0	CK0	91	SDA	SDA	183	SA2	SA2
46	V _{DD}	V _{DD}	138	CK0/	CK0/	92	SCL	SCL	184	V _{DDSPD}	V _{DDSPD}
47	NC	DQS8	139	V _{SS}	V _{SS}						

NC = No Connect; NU = Not Useable; DU = Do Not Use

APPENDIX D - NEX-DDRHSM P6860 Compression Pinouts

For further information on the P6860 Connectorless probe compression footprint please refer to the “P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

Pad #	TLA Channel	DDR Pin #	DDR Signal
A15	CK1-		GND
A13	CK1+	92	SCL
B12	A1:7	91	SDA
B10	A1:6	182	SA1
A12	A1:5	183	SA2
A10	A1:4	181	SA0
B9	A1:3	90	NC90
B7	A1:2	88	DQ59
A9	A1:1	87	DQ58
A7	A1:0	80	DQ51
B6	A0:7	82	VddID
B4	A0:6	171	DQ55
A6	A0:5	170	DQ54
A4	A0:4		
B3	A0:3	167	A13
B1	A0:2	166	DQ53
A3	A0:1	73	DQ49
A1	A0:0	165	DQ52

P21

Probe Connection SL – A0 / A1

Pad #	TLA Channel	DDR Pin #	DDR Signal
A15	CK3-	76	CK2~
A13	CK3+	75	CK2
B12	C3:7	179	DQ63
B10	C3:6	86	DQS7
A12	C3:5	178	DQ62
A10	C3:4	84	DQ57
B9	C3:3	177	DM7
B7	C3:2	175	DQ61
A9	C3:1	83	DQ56
A7	C3:0	173	NC1
B6	C2:7	174	DQ60
B4	C2:6	79	DQ50
A6	C2:5	78	DQS6
A4	C2:4	169	DM6
B3	C2:3	65	CAS~
B1	C2:2	157	S0~
A3	C2:1	63	WE~
A1	C2:0	154	RAS~

P12

Probe Connection MA – C2 / C3

Pad #	TLA Channel	DDR Pin #	DDR Signal
A15	CK0-		
A13	CK0+		
B12	A3:7	72	DQ48
B10	A3:6	163	NC_S3~
A12	A3:5	161	DQ46
A10	A3:4	69	DQ43
B9	A3:3	71	NC_S2~
B7	A3:2	162	DQ47
A9	A3:1	153	DQ44
A7	A3:0	149	DM4
B6	A2:7	151	DQ39
B4	A2:6	57	DQ34
A6	A2:5	55	DQ33
A4	A2:4	142	NC_CB6
B3	A2:3	144	NC_CB7
B1	A2:2	141	A10
A3	A2:1	49	NC_CB2
A1	A2:0	48	A0

P31

Probe Connection SL - A2 / A3

Pad #	TLA Channel	DDR Pin #	DDR Signal
A15	Q3-		GND
A13	Q3+	158	S1~
B12	E3:7	159	DM5
B10	E3:6	68	DQ42
A12	E3:5	67	DQS5
A10	E3:4	155	DQ45
B9	E3:3	64	DQ41
B7	E3:2	61	DQ40
A9	E3:1	60	DQ35
A7	E3:0	150	DQ38
B6	E2:7	59	BA0
B4	E2:6	56	DQS4
A6	E2:5	147	DQ37
A4	E2:4	53	DQ32
B3	E2:3	146	DQ36
B1	E2:2	52	BA1
A3	E2:1	51	NC_CB3
A1	E2:0	140	NC_DM8

P42

Probe Connection MA – E2 / E3

APPENDIX D - NEX-DDRHS P6860 Compression Pinouts (cont'd.)

Pad #	TLA Channel	DDR Pin #	DDR Signal
A15	CK3-		
A13	CK3+		
B12	C3:7	47	NC_DQS8
B10	C3:6	44	NC_CB0
A12	C3:5	134	NC_CB4
A10	C3:4	39	DQ26
B9	C3:3	133	DQ31
B7	C3:2	37	A4
A9	C3:1	129	DM3
A7	C3:0	126	DQ28
B6	C2:7	35	DQ25
B4	C2:6	32	A5
A6	C2:5	122	A8
A4	C2:4	29	A7
B3	C2:3	27	A9
B1	C2:2	117	DQ21
A3	C2:1	118	A11
A1	C2:0	25	DQS2

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Probe Connection SL - C2 / C3

Pad ##	TLA Channel	DDR Pin #	DDR Signal
A15	CK0-	138	CK0~
A13	CK0+	137	CK0
B12	A3:7	45	NC_CB1
B10	A3:6	135	NC_CB5
A12	A3:5	43	A1
A10	A3:4	40	DQ27
B9	A3:3	41	A2
B7	A3:2	131	DQ30
A9	A3:1	130	A3
A7	A3:0	36	DQS3
B6	A2:7	127	DQ29
B4	A2:6	125	A6
A6	A2:5	33	DQ24
A4	A2:4	123	DQ23
B3	A2:3	31	DQ19
B1	A2:2	28	DQ18
A3	A2:1	121	DQ22
A1	A2:0	119	DM2

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Probe Connection MA – A2 / A3

Pad #	TLA Channel	DDR Pin #	DDR Signal
A15	Q3-		
A13	Q3+		
B12	E3:7	24	DQ17
B10	E3:6	115	A12
A12	E3:5	23	DQ16
A10	E3:4	113	BA2
B9	E3:3	114	DQ20
B7	E3:2	21	CKE0
A9	E3:1	106	DQ13
A7	E3:0	12	DQ8
B6	E2:7	14	DQS1
B4	E2:6	102	NC2
A6	E2:5	8	DQ3
A4	E2:4	6	DQ2
B3	E2:3	98	DQ6
B1	E2:2	2	DQ0
A3	E2:1	4	DQ1
A1	E2:0	94	DQ4

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Probe Connection SL – E2 / E3

Pad ##	TLA Channel	DDR Pin #	DDR Signal
A15	CK1-	17	CK1~
A13	CK1+	16	CK1
B12	A1:7	20	DQ11
B10	A1:6	111	CKE1
A12	A1:5	109	DQ14
A10	A1:4	110	DQ15
B9	A1:3	19	DQ10
B7	A1:2	107	DM1
A9	A1:1	105	DQ12
A7	A1:0	103	NC103
B6	A0:7	13	DQ9
B4	A0:6	10	RESET~
A6	A0:5	9	NC4
A4	A0:4	99	DQ7
B3	A0:3	101	NC3
B1	A0:2	5	DQS0
A3	A0:1	97	DM0
A1	A0:0	95	DQ5

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Probe Connection MA – A0 / A1

APPENDIX E – Data Group / Data Byte / Strobe Cross-Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
DataHi	DatByte7	DQS7	63,62,61,60,59,58,57,56
	DatByte6	DQS6	55,54,53,52,51,50,49,48
	DatByte5	DQS5	47,46,45,44,43,42,41,40
	DatByte4	DQS4	39,38,37,36,35,34,33,32
DataLo	DatByte3	DQS3	31,30,29,28,27,26,25,24
	DatByte2	DQS2	23,22,21,20,19,18,17,16
	DatByte1	DQS1	15,14,13,12,11,10,9,8
	DatByte0	DQS0	7,6,5,4,3,2,1,0

DDRHSM Groups/Bytes/Strobes Cross Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
RdDatHi	RDDatBy7	DQS7	63,62,61,60,59,58,57,56
	RDDatBy6	DQS6	55,54,53,52,51,50,49,48
	RDDatBy5	DQS5	47,46,45,44,43,42,41,40
	RDDatBy4	DQS4	39,38,37,36,35,34,33,32
RdDatLo	RDDatBy3	DQS3	31,30,29,28,27,26,25,24
	RDDatBy2	DQS2	23,22,21,20,19,18,17,16
	RDDatBy1	DQS1	15,14,13,12,11,10,9,8
	RDDatBy0	DQS0	7,6,5,4,3,2,1,0
WrDatHi	WRDatBy7	DQS7	63,62,61,60,59,58,57,56
	WRDatBy6	DQS6	55,54,53,52,51,50,49,48
	WRDatBy5	DQS5	47,46,45,44,43,42,41,40
	WRDatBy4	DQS4	39,38,37,36,35,34,33,32
WrDatLo	WRDatBy3	DQS3	31,30,29,28,27,26,25,24
	WRDatBy2	DQS2	23,22,21,20,19,18,17,16
	WRDatBy1	DQS1	15,14,13,12,11,10,9,8
	WRDatBy0	DQS0	7,6,5,4,3,2,1,0

DDRHSMRW Groups/Bytes/Strobes Cross Reference

APPENDIX F - References

JEDEC Double Data Rate (DDR) SDRAM Specification
JESD-79-R2 – February 2002

Micron MT46V16M4/MT46V8M8/MT46V4M16 Double Data Rate (DDR) SDRAM
Data Sheet Rev. 2/00

Tektronix TLA700 System User's Manual

Tektronix TLA700 Logic Analyzer User's Manual

P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual
Tektronix part number 071-1059-00

APPENDIX G - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.