



NEX-DDRII400

DDRII (Double Data Rate)

Synchronous DRAM DIMM Support

Including these Software Support packages:
400DDR2M 400DDR2S DDRSPA

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1.0 OVERVIEW

1.1 General Information

The NEX-DDR2 adapter has been designed to provide a quick and easy connection to interface a Tektronix TLA700 Logic Analyzer to a 240-pin 1.8Volt 64/72-bit wide DDR2 (Double Data Rate II) Synchronous DRAM Dual In-Line Memory Module (DDR2 SDRAM DIMM) socket. Analyzer connections are made through P6860 and, optionally, one P6880 High-Density Connectorless probes to help minimize the size of the adapter board, thus reducing trace length and keeping signal loading to a minimum.

The NEX-DDR2400 support requires two merged TLA7AA4 or TLA7AB4 136-channel acquisition cards. This support is designed to give the user the ability to acquire up to 400MHz DDR2 Read and Write data. For this support to work, both merged cards must have the 450MHz state clocking option (refer to Section 5.0 for further information). The NEX-DDR2400 support is usable with a TLA7XX-series Logic Analyzer only, and the TLA must be running V4.2 or later of the TLA Application Software. The NEX-DDR2400 software also post-processes the acquisition to display valid cycle information to the user.

The DDR2 specification calls out several signals that can either be used as additional Data Strokes or Write Masks. To support both configurations two software packages have been included with the NEX-DDR2400 support:

400DDR2S allows the user to acquire DDR2 data from a target that uses 18 Data Strokes (16 for Data and 2 for Check Bits) instead of Write Masks. This support requires 7-P6860 and 1-P6880 High-Density Compression probes.

400DDR2M allows the user to acquire DDR2 data from a target that uses 8 Data Strokes and 8 Write Masks. This support requires 8-P6860 High-Density Compression probes.

Note that this manual uses some terms generically. For instance, references to the TLA700 apply to all suitable TLA700 Logic Analyzers. DDR2400 refers to both the 400DDR2S and 400DDR2M software support packages.

Appendix E has a silk-screened print of the NEX-DDR2 adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the DDR-II SDRAM Specification and the Tektronix TLA700 Logic Analyzers. It is also expected that the user is familiar with the Windows environment used on the TLA (Windows 2000).

2.0 SOFTWARE INSTALLATION

The NEX-DDR2400 software is installed using the same method as other Windows programs. Place the 400DDR2S or 400DDR2M Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install, Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer module in the Setup window, select Load Support Package from the File pull-down, then choose either 400DDR2S or 400DDR2M and click on **Okay**. Note that the support requires two merged modules and that the TLA acquisition cards must be configured properly for the software to load.

3.0 CONNECTING to the NEX-DDR2 ADAPTER

3.1 General

Care should be taken to support the weight of the acquisition probes so that the adapter board and/or target socket are not damaged

The NEX-DDR2 adapter is larger than a standard DDR DIMM module and is designed to function as an extender card, providing an easy connection to the logic analyzer for DDR data acquisition. Because of this design approach it is entirely possible that placing a target card onto the NEX-DDR2400 adapter may result in improper operation of the target card or system.

Care should be used when removing a DIMM under test from the Adapter. The extraction tabs will break if excessive force is used.

The NEX-DDR2400 support requires two merged TLA7Axx acquisition cards. The Master card is the card in the lower-numbered slots; the Slave card is the card in the higher-numbered slots. When using the 400DDR2S support with a target configured for 18 Data Strokes the acquisition cards must be connected to the NEX-DDR2400 adapter as follows using seven (7) P6860 probes and one (1) P6880 probe:

- TLA Master P6860 A2/A3 probe head to DDR2 MA-A2/A3 position
- TLA Master P6860 A0/A1 probe head to DDR2 MA-A0/A1 position
- TLA Master P6860 C2/C3 probe head to DDR2 MA-C2/C3 position
- TLA Master P6860 E2/E3 probe head to DDR2 MA-E2/E3 position
- TLA Slave P6860 A2/A3 probe head to DDR2 SL-A2/A3 position
- TLA Slave P6860 C2/C3 probe head to DDR2 SL-C2/C3 position
- TLA Slave P6860 E2/E3 probe head to DDR2 SL-E2/E3 position
- TLA Slave P6880 A0 probe head to DDR2 SL-A0 (DIFF) position
- TLA Slave P6880 A1 probe head to DDR2 SL-A1 (DIFF) position

Table 1 shows the Channel Grouping / Wiring for use with the 400DDR2S support. When using the 400DDR2M support with a target configured for 8 Data Strobes and 8 Write Masks the acquisition cards must be connected to the NEX-DDR11400 adapter as follows using eight (8) P6860 probes:

TLA Master P6860 A2/A3 probe head to DDR11 MA-A2/A3 position
TLA Master P6860 A0/A1 probe head to DDR11 MA-A0/A1 position
TLA Master P6860 C2/C3 probe head to DDR11 MA-C2/C3 position
TLA Master P6860 E2/E3 probe head to DDR11 MA-E2/E3 position
TLA Slave P6860 A2/A3 probe head to DDR11 SL-A2/A3 position
TLA Slave P6860 C2/C3 probe head to DDR11 SL-C2/C3 position
TLA Slave P6860 E2/E3 probe head to DDR11 SL-E2/E3 position
TLA Slave P6860 A0/A1 probe head to DDR11 SL-A0 (DIFF) position
TLA Slave P6860 D0/D1 probe head to DDR11 SL-A1 (DIFF) position

Table 2 shows the Channel Grouping / Wiring for use with the 400DDR2M support.

IMPORTANT: When using the 400DDR2M support it is strongly recommended that DDR11 DIMM pin #212 be tied to ground. This signal is the inverted half of the DQS14 pair when used as a Data Strobe, and is defined as a No Connect when the signal is used as a Write Mask. If pin #212 is not tied to ground inaccurate acquisition of the DM5 Write Mask may result.

| Group Name | Signal Name | DDRII Pin # | TLA700 Input | Group Name | Signal Name | DDRII Pin # | TLA700 Input |
|------------------|-------------|-------------|--------------|------------------|-------------|-------------|--------------|
| RdDatHi (Hex) | RD_DQ63 | 236 | A0:2 | RdDatLo (Hex) | RD_DQ31 | 159 | SA3:3 |
| | RD_DQ62 | 235 | A0:1 | | RD_DQ30 | 158 | SA3:5 |
| | RD_DQ61 | 230 | A0:5 | | RD_DQ29 | 153 | SA2:4 |
| | RD_DQ60 | 229 | A1:0 | | RD_DQ28 | 152 | SE3:0 |
| | RD_DQ59 | 117 | A0:0 | | RD_DQ27 | 40 | SA3:2 |
| | RD_DQ58 | 116 | A0:3 | | RD_DQ26 | 39 | SA3:4 |
| | RD_DQ57 | 111 | A0:4 | | RD_DQ25 | 34 | SC2:4 |
| | RD_DQ56 | 110 | A0:6 | | RD_DQ24 | 33 | SC2:2 |
| | RD_DQ55 | 227 | A1:1 | | RD_DQ23 | 150 | SA2:3 |
| | RD_DQ54 | 226 | A1:3 | | RD_DQ22 | 149 | SA2:1 |
| | RD_DQ53 | 218 | A1:6 | | RD_DQ21 | 144 | SE2:4 |
| | RD_DQ52 | 217 | A1:7 | | RD_DQ20 | 143 | SA2:0 |
| | RD_DQ51 | 108 | A0:7 | | RD_DQ19 | 31 | SE2:5 |
| | RD_DQ50 | 107 | A1:2 | | RD_DQ18 | 30 | SC2:1 |
| | RD_DQ49 | 99 | A1:5 | | RD_DQ17 | 25 | SC2:0 |
| | RD_DQ48 | 98 | A1:4 | | RD_DQ16 | 24 | SA2:2 |
| | RD_DQ47 | 215 | C3:4 | | RD_DQ15 | 141 | A3:7 |
| | RD_DQ46 | 214 | C3:2 | | RD_DQ14 | 140 | A3:5 |
| | RD_DQ45 | 209 | C3:1 | | RD_DQ13 | 132 | A3:2 |
| | RD_DQ44 | 208 | C2:7 | | RD_DQ12 | 131 | A3:1 |
| | RD_DQ43 | 96 | C3:5 | | RD_DQ11 | 22 | A3:6 |
| | RD_DQ42 | 95 | C3:3 | | RD_DQ10 | 21 | A3:4 |
| | RD_DQ41 | 90 | C3:0 | | RD_DQ9 | 13 | A3:3 |
| | RD_DQ40 | 89 | C2:6 | | RD_DQ8 | 12 | A2:7 |
| | RD_DQ39 | 206 | C2:4 | | RD_DQ7 | 129 | A2:6 |
| | RD_DQ38 | 205 | E2:5 | | RD_DQ6 | 128 | A2:3 |
| | RD_DQ37 | 200 | E2:2 | | RD_DQ5 | 123 | A2:1 |
| | RD_DQ36 | 199 | E2:3 | | RD_DQ4 | 122 | A2:0 |
| | RD_DQ35 | 87 | C2:5 | | RD_DQ3 | 10 | A3:0 |
| | RD_DQ34 | 86 | E2:4 | | RD_DQ2 | 9 | A2:5 |
| | RD_DQ33 | 81 | E2:0 | | RD_DQ1 | 4 | A2:4 |
| | RD_DQ32 | 80 | E2:1 | | RD_DQ0 | 3 | A2:2 |

Table 1- 400DDR2S (Strobes) TLA700 Channel Grouping

Notes:

1. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
2. All signals are required for accurate post-processing of acquired data

| Group Name | Signal Name | DDRII Pin # | TLA700 Input | Group Name | Signal Name | DDRII Pin # | TLA700 Input |
|------------------|-------------|-------------|--------------|------------------|-------------|-------------|--------------|
| WrDatHi (Hex) | WR_DQ63 | 236 | D0:2 | WrDatLo (Hex) | WR_DQ31 | 159 | SD3:3 |
| | WR_DQ62 | 235 | D0:1 | | WR_DQ30 | 158 | SD3:5 |
| | WR_DQ61 | 230 | D0:5 | | WR_DQ29 | 153 | SD2:4 |
| | WR_DQ60 | 229 | D1:0 | | WR_DQ28 | 152 | SE1:0 |
| | WR_DQ59 | 117 | D0:0 | | WR_DQ27 | 40 | SD3:2 |
| | WR_DQ58 | 116 | D0:3 | | WR_DQ26 | 39 | SD3:4 |
| | WR_DQ57 | 111 | D0:4 | | WR_DQ25 | 34 | SC0:4 |
| | WR_DQ56 | 110 | D0:6 | | WR_DQ24 | 33 | SC0:2 |
| | WR_DQ55 | 227 | D1:1 | | WR_DQ23 | 150 | SD2:3 |
| | WR_DQ54 | 226 | D1:3 | | WR_DQ22 | 149 | SD2:1 |
| | WR_DQ53 | 218 | D1:6 | | WR_DQ21 | 144 | SE0:4 |
| | WR_DQ52 | 217 | D1:7 | | WR_DQ20 | 143 | SD2:0 |
| | WR_DQ51 | 108 | D0:7 | | WR_DQ19 | 31 | SE0:5 |
| | WR_DQ50 | 107 | D1:2 | | WR_DQ18 | 30 | SC0:1 |
| | WR_DQ49 | 99 | D1:5 | | WR_DQ17 | 25 | SC0:0 |
| | WR_DQ48 | 98 | D1:4 | | WR_DQ16 | 24 | SD2:2 |
| | WR_DQ47 | 215 | C1:4 | | WR_DQ15 | 141 | D3:7 |
| | WR_DQ46 | 214 | C1:2 | | WR_DQ14 | 140 | D3:5 |
| | WR_DQ45 | 209 | C1:1 | | WR_DQ13 | 132 | D3:2 |
| | WR_DQ44 | 208 | C0:7 | | WR_DQ12 | 131 | D3:1 |
| | WR_DQ43 | 96 | C1:5 | | WR_DQ11 | 22 | D3:6 |
| | WR_DQ42 | 95 | C1:3 | | WR_DQ10 | 21 | D3:4 |
| | WR_DQ41 | 90 | C1:0 | | WR_DQ9 | 13 | D3:3 |
| | WR_DQ40 | 89 | C0:6 | | WR_DQ8 | 12 | D2:7 |
| | WR_DQ39 | 206 | C0:4 | | WR_DQ7 | 129 | D2:6 |
| | WR_DQ38 | 205 | E0:5 | | WR_DQ6 | 128 | D2:3 |
| | WR_DQ37 | 200 | E0:2 | | WR_DQ5 | 123 | D2:1 |
| | WR_DQ36 | 199 | E0:3 | | WR_DQ4 | 122 | D2:0 |
| | WR_DQ35 | 87 | C0:5 | | WR_DQ3 | 10 | D3:0 |
| | WR_DQ34 | 86 | E0:4 | | WR_DQ2 | 9 | D2:5 |
| | WR_DQ33 | 81 | E0:0 | | WR_DQ1 | 4 | D2:4 |
| | WR_DQ32 | 80 | E0:1 | | WR_DQ0 | 3 | D2:2 |

Table 1 (cont'd) – 400DDR2S (Strobes) TLA700 Channel Grouping

Notes:

1. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
2. All signals are required for accurate post-processing of acquired data

| Group Name | Signal Name | DDRII Pin # | TLA700 Input | Group Name | Signal Name | DDRII Pin # | TLA700 Input |
|------------------|--------------|-------------|--------------|------------------|-------------|-------------|--------------|
| Address (Hex) | BA1 | 190 | E3:4 | Command (Sym) | * S1~ | 76 | C2:3 |
| | BA0 | 71 | E3:6 | | * S0~ | 193 | C2:0 |
| | A16/BA2 | 54 | SC3:4 | | * RAS~ | 192 | Q3 |
| | A15 | 173 | SA3:6 | | * CAS~ | 74 | C2:2 |
| | A14 | 174 | SE3:6 | * WE~ | 73 | C2:1 | |
| | A13 | 196 | E3:3 | Strobes (Hex) | DQS16 +/- | 232 / 233 | SA1:0 |
| | A12 | 176 | SC3:3 | | DQS15 +/- | 223 / 224 | SA1:4 |
| | A11 | 57 | SC3:2 | | DQS14 +/- | 211 / 212 | SCK1 |
| | A10 | 70 | E3:7 | | DQS13 +/- | 202 / 203 | SA1:5 |
| | A9 | 177 | SE3:3 | | DQS12 +/- | 155 / 156 | SA0:6 |
| | A8 | 179 | SE3:2 | | DQS11 +/- | 146 / 147 | SA0:5 |
| | A7 | 58 | SE3:4 | | DQS10 +/- | 134 / 135 | SA0:3 |
| | A6 | 180 | SA3:1 | | DQS9 +/- | 125 / 126 | SA0:1 |
| | A5 | 60 | SE2:7 | | DQS7 +/- | 114 / 113 | SA1:1 |
| | A4 | 61 | SA2:7 | | DQS6 +/- | 105 / 104 | SA1:2 |
| | A3 | 182 | SA3:0 | | DQS5 +/- | 93 / 92 | SA1:6 |
| | A2 | 63 | SE2:6 | | DQS4 +/- | 84 / 83 | SA1:7 |
| A1 | 183 | SA2:6 | DQS3 +/- | | 37 / 36 | SA0:7 | |
| A0 | 188 | C3:6 | DQS2 +/- | 28 / 27 | SA0:4 | | |
| Ungrouped | CKE1 | 171 | SA3:7 | RDChkBts1 7 | RD_NC_CB7 | 168 | SC2:5 |
| | CKE0 | 52 | SC3:5 | | RD_NC_CB6 | 167 | SE3:1 |
| | ODT1 | 77 | E3:2 | | RD_NC_CB5 | 162 | SC2:6 |
| | ODT0 | 195 | E3:1 | | RD_NC_CB4 | 161 | SC3:1 |
| | RC1 | 18 | SC3:7 | RDChkBits 8 | RD_NC_CB3 | 49 | SA2:5 |
| | RC0 | 55 | SE3:5 | | RD_NC_CB2 | 48 | SC2:3 |
| | SCL | 120 | SE2:1 | | RD_NC_CB1 | 43 | SC3:0 |
| | SDA | 119 | SE2:0 | | RD_NC_CB0 | 42 | SC2:7 |
| | SA2 | 101 | E3:0 | WRChkBts1 7 | WR_NC_CB7 | 168 | SC0:5 |
| | SA1 | 240 | SA1:3 | | WR_NC_CB6 | 167 | SE1:1 |
| | SA0 | 239 | E2:6 | | WR_NC_CB5 | 162 | SC0:6 |
| | DQS17 +/- | 164 / 165 | SCK3 | WR_NC_CB4 | 161 | SC1:1 | |
| | DQS8 +/- | 46 / 45 | SQ3 | WRChkBits 8 | WR_NC_CB3 | 49 | SD2:5 |
| * DDRCK2 +/- | 220 / 221 | CK1 | WR_NC_CB2 | | 48 | SC0:3 | |
| - | - | - | WR_NC_CB1 | | 43 | SC1:0 | |
| * DDRCK1 +/- | 137 / 138 | CK0 | WR_NC_CB0 | | 42 | SC0:7 | |
| - | - | - | - | - | - | - | |
| * DDRCK0 +/- | 185 / 186 | CK3 | - | - | - | - | |
| - | - | - | - | - | - | - | |
| Misc | * DDRCK2 +/- | 220 / 221 | CK1 | - | - | - | |
| - | - | - | - | - | - | - | |
| * DDRCK1 +/- | 137 / 138 | CK0 | - | - | - | - | |
| - | - | - | - | - | - | - | |
| * DDRCK0 +/- | 185 / 186 | CK3 | - | - | - | - | |
| - | - | - | - | - | - | - | |

Table 1 (cont'd) – 400DDR2S (Strobes) TLA700 Channel Grouping

Notes:

1. ‘ ~ ’ denotes a low-true signal
2. The ‘S’ in front of a TLA channel denotes the Slave card of the merged pair
3. Signal names preceded by an asterisk (*) are required for accurate acquisition and post-processing of acquired data

| Group Name | Signal Name | DDRII Pin # | TLA700 Input | Group Name | Signal Name | DDRII Pin # | TLA700 Input |
|------------------|-------------|-------------|--------------|------------------|-------------|-------------|--------------|
| RdDatHi (Hex) | RD_DQ63 | 236 | A0:2 | RdDatLo (Hex) | RD_DQ31 | 159 | SA3:3 |
| | RD_DQ62 | 235 | A0:1 | | RD_DQ30 | 158 | SA3:5 |
| | RD_DQ61 | 230 | A0:5 | | RD_DQ29 | 153 | SA2:4 |
| | RD_DQ60 | 229 | A1:0 | | RD_DQ28 | 152 | SE3:0 |
| | RD_DQ59 | 117 | A0:0 | | RD_DQ27 | 40 | SA3:2 |
| | RD_DQ58 | 116 | A0:3 | | RD_DQ26 | 39 | SA3:4 |
| | RD_DQ57 | 111 | A0:4 | | RD_DQ25 | 34 | SC2:4 |
| | RD_DQ56 | 110 | A0:6 | | RD_DQ24 | 33 | SC2:2 |
| | RD_DQ55 | 227 | A1:1 | | RD_DQ23 | 150 | SA2:3 |
| | RD_DQ54 | 226 | A1:3 | | RD_DQ22 | 149 | SA2:1 |
| | RD_DQ53 | 218 | A1:6 | | RD_DQ21 | 144 | SE2:4 |
| | RD_DQ52 | 217 | A1:7 | | RD_DQ20 | 143 | SA2:0 |
| | RD_DQ51 | 108 | A0:7 | | RD_DQ19 | 31 | SE2:5 |
| | RD_DQ50 | 107 | A1:2 | | RD_DQ18 | 30 | SC2:1 |
| | RD_DQ49 | 99 | A1:5 | | RD_DQ17 | 25 | SC2:0 |
| | RD_DQ48 | 98 | A1:4 | | RD_DQ16 | 24 | SA2:2 |
| | RD_DQ47 | 215 | C3:4 | | RD_DQ15 | 141 | A3:7 |
| | RD_DQ46 | 214 | C3:2 | | RD_DQ14 | 140 | A3:5 |
| | RD_DQ45 | 209 | C3:1 | | RD_DQ13 | 132 | A3:2 |
| | RD_DQ44 | 208 | C2:7 | | RD_DQ12 | 131 | A3:1 |
| | RD_DQ43 | 96 | C3:5 | | RD_DQ11 | 22 | A3:6 |
| | RD_DQ42 | 95 | C3:3 | | RD_DQ10 | 21 | A3:4 |
| | RD_DQ41 | 90 | C3:0 | | RD_DQ9 | 13 | A3:3 |
| | RD_DQ40 | 89 | C2:6 | | RD_DQ8 | 12 | A2:7 |
| | RD_DQ39 | 206 | C2:4 | | RD_DQ7 | 129 | A2:6 |
| | RD_DQ38 | 205 | E2:5 | | RD_DQ6 | 128 | A2:3 |
| | RD_DQ37 | 200 | E2:2 | | RD_DQ5 | 123 | A2:1 |
| | RD_DQ36 | 199 | E2:3 | | RD_DQ4 | 122 | A2:0 |
| | RD_DQ35 | 87 | C2:5 | | RD_DQ3 | 10 | A3:0 |
| | RD_DQ34 | 86 | E2:4 | | RD_DQ2 | 9 | A2:5 |
| | RD_DQ33 | 81 | E2:0 | | RD_DQ1 | 4 | A2:4 |
| | RD_DQ32 | 80 | E2:1 | | RD_DQ0 | 3 | A2:2 |

Table 2- 400DDR2M (Write Masks) TLA700 Channel Grouping

Notes:

1. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
2. All signals are required for accurate post-processing of acquired data

| Group Name | Signal Name | DDRII Pin # | TLA700 Input | Group Name | Signal Name | DDRII Pin # | TLA700 Input |
|------------------|-------------|-------------|--------------|------------------|-------------|-------------|--------------|
| WrDatHi (Hex) | WR_DQ63 | 236 | D0:2 | WrDatLo (Hex) | WR_DQ31 | 159 | SD3:3 |
| | WR_DQ62 | 235 | D0:1 | | WR_DQ30 | 158 | SD3:5 |
| | WR_DQ61 | 230 | D0:5 | | WR_DQ29 | 153 | SD2:4 |
| | WR_DQ60 | 229 | D1:0 | | WR_DQ28 | 152 | SE1:0 |
| | WR_DQ59 | 117 | D0:0 | | WR_DQ27 | 40 | SD3:2 |
| | WR_DQ58 | 116 | D0:3 | | WR_DQ26 | 39 | SD3:4 |
| | WR_DQ57 | 111 | D0:4 | | WR_DQ25 | 34 | SC0:4 |
| | WR_DQ56 | 110 | D0:6 | | WR_DQ24 | 33 | SC0:2 |
| | WR_DQ55 | 227 | D1:1 | | WR_DQ23 | 150 | SD2:3 |
| | WR_DQ54 | 226 | D1:3 | | WR_DQ22 | 149 | SD2:1 |
| | WR_DQ53 | 218 | D1:6 | | WR_DQ21 | 144 | SE0:4 |
| | WR_DQ52 | 217 | D1:7 | | WR_DQ20 | 143 | SD2:0 |
| | WR_DQ51 | 108 | D0:7 | | WR_DQ19 | 31 | SE0:5 |
| | WR_DQ50 | 107 | D1:2 | | WR_DQ18 | 30 | SC0:1 |
| | WR_DQ49 | 99 | D1:5 | | WR_DQ17 | 25 | SC0:0 |
| | WR_DQ48 | 98 | D1:4 | | WR_DQ16 | 24 | SD2:2 |
| | WR_DQ47 | 215 | C1:4 | | WR_DQ15 | 141 | D3:7 |
| | WR_DQ46 | 214 | C1:2 | | WR_DQ14 | 140 | D3:5 |
| | WR_DQ45 | 209 | C1:1 | | WR_DQ13 | 132 | D3:2 |
| | WR_DQ44 | 208 | C0:7 | | WR_DQ12 | 131 | D3:1 |
| | WR_DQ43 | 96 | C1:5 | | WR_DQ11 | 22 | D3:6 |
| | WR_DQ42 | 95 | C1:3 | | WR_DQ10 | 21 | D3:4 |
| | WR_DQ41 | 90 | C1:0 | | WR_DQ9 | 13 | D3:3 |
| | WR_DQ40 | 89 | C0:6 | | WR_DQ8 | 12 | D2:7 |
| | WR_DQ39 | 206 | C0:4 | | WR_DQ7 | 129 | D2:6 |
| | WR_DQ38 | 205 | E0:5 | | WR_DQ6 | 128 | D2:3 |
| | WR_DQ37 | 200 | E0:2 | | WR_DQ5 | 123 | D2:1 |
| | WR_DQ36 | 199 | E0:3 | | WR_DQ4 | 122 | D2:0 |
| | WR_DQ35 | 87 | C0:5 | | WR_DQ3 | 10 | D3:0 |
| | WR_DQ34 | 86 | E0:4 | | WR_DQ2 | 9 | D2:5 |
| | WR_DQ33 | 81 | E0:0 | | WR_DQ1 | 4 | D2:4 |
| | WR_DQ32 | 80 | E0:1 | | WR_DQ0 | 3 | D2:2 |

Table 2 (cont'd) – 400DDR2M (Write Masks) TLA700 Channel Grouping

Notes:

1. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
2. All signals are required for accurate post-processing of acquired data

| Group Name | Signal Name | DDRII Pin # | TLA700 Input | Group Name | Signal Name | DDRII Pin # | TLA700 Input |
|------------------|------------------|-------------|--------------|------------------|-------------|-------------|--------------|
| Address (Hex) | BA1 | 190 | E3:4 | Command (Sym) | * S1~ | 76 | C2:3 |
| | BA0 | 71 | E3:6 | | * S0~ | 193 | C2:0 |
| | A16/BA2 | 54 | SC3:4 | | * RAS~ | 192 | Q3 |
| | A15 | 173 | SA3:6 | | * CAS~ | 74 | C2:2 |
| | A14 | 174 | SE3:6 | * WE~ | 73 | C2:1 | |
| | A13 | 196 | E3:3 | Strobes (Hex) | DQS7 + | 114 | SD0:3 |
| | A12 | 176 | SC3:3 | | DQS6 + | 105 | SD0:4 |
| | A11 | 57 | SC3:2 | | DQS5 + | 93 | SD1:4 |
| | A10 | 70 | E3:7 | | DQS4 + | 84 | SD1:7 |
| | A9 | 177 | SE3:3 | | DQS3 + | 37 | SA1:7 |
| | A8 | 179 | SE3:2 | | DQS2 + | 28 | SA1:0 |
| | A7 | 58 | SE3:4 | | DQS1 + | 16 | SA0:4 |
| | A6 | 180 | SA3:1 | | DQS0 + | 7 | SA0:0 |
| | A5 | 60 | SE2:7 | RDChkBts | DQS8 + | 46 | SCK3 |
| | A4 | 61 | SA2:7 | | RD_NC_CB7 | 168 | SC2:5 |
| | A3 | 182 | SA3:0 | | RD_NC_CB6 | 167 | SE3:1 |
| | A2 | 63 | SE2:6 | | RD_NC_CB5 | 162 | SC2:6 |
| A1 | 183 | SA2:6 | RD_NC_CB4 | | 161 | SC3:1 | |
| A0 | 188 | C3:6 | RD_NC_CB3 | | 49 | SA2:5 | |
| Ungrouped | CKE1 | 171 | SA3:7 | | RD_NC_CB2 | 48 | SC2:3 |
| | CKE0 | 52 | SC3:5 | | RD_NC_CB1 | 43 | SC3:0 |
| | ODT1 | 77 | E3:2 | RD_NC_CB0 | 42 | SC2:7 | |
| | ODT0 | 195 | E3:1 | WRChkBt s | DM8 | 164 | SQ3 |
| | RC1 | 18 | SC3:7 | | WR_NC_CB7 | 168 | SC0:5 |
| | RC0 | 55 | SE3:5 | | WR_NC_CB6 | 167 | SE1:1 |
| | SCL | 120 | SE2:1 | | WR_NC_CB5 | 162 | SC0:6 |
| | SDA | 119 | SE2:0 | | WR_NC_CB4 | 161 | SC1:1 |
| | SA2 | 101 | E3:0 | | WR_NC_CB3 | 49 | SD2:5 |
| | SA1 | 240 | SA1:3 | | WR_NC_CB2 | 48 | SC0:3 |
| SA0 | 239 | E2:6 | WR_NC_CB1 | | 43 | SC1:0 | |
| Misc | * DDRCK2 + /- | 220 / 221 | CK1 | WR_NC_CB0 | 42 | SC0:7 | |
| | * DDRCK1 + /- | 137 / 138 | CK0 | WrtMasks | DM7 | 232 | SD0:0 |
| | * DDRCK0 + /- | 185 / 186 | CK3 | | DM6 | 223 | SD1:0 |
| | | | | | DM5 | 211 | SCK2 |
| | | | | | DM4 | 202 | SD1:3 |
| | | | | | DM3 | 155 | SA1:4 |
| | | | | | DM2 | 146 | SA1:3 |
| | | | | | DM1 | 134 | SA0:7 |
| | | | | | DM0 | 125 | SA0:3 |

Table 2 (cont'd) – 400DDR2M (Write Masks) TLA700 Channel Grouping

Notes:

1. ‘ ~ ‘ denotes a low-true signal
2. The ‘S’ in front of a TLA channel denotes the Slave card of the merged pair
3. Signal names preceded by an asterisk (*) are required for accurate acquisition and post-processing of acquired data

4.0 CLOCK SELECTION

There are three clocking option fields available when using the DDRII400 support package. These select fields permit the user to setup the TLA acquisition as follows:

SDRAM Clocking: – Permits selecting the DDR Clock to be used to acquire data. Also allows user to use only Chip Select S0~ or Chip Selects S0~ and S1~ for acquisition. The field choices are:

DDR CK0; S0~ only active (default)

DDR CK0; S0~ & S1~ active

DDR CK1; S0~ only active

DDR CK1 S0~ & S1~ active

DDR CK2 S0~ only active

DDR CK2 S0~ & S1~ active

Clock Mode – Allows the user to choose the kind of data acquisition that will be made:

Selective Clocking (default) – This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS~ or CAS~ is asserted low along with S0~ or S1~. After every assertion of CAS~ (with either S0~ or S1~) a sample is taken on each edge of the next 13 DDR CLK cycles for a total of 26 samples. If CAS~ and a Chip Select are asserted during these 13 cycles the count is reset.

Every SDRAM Clock Edge – As the name implies this will cause the acquisition card to store data on every Rising and Falling edge of the selected SDRAM clock.

Refresh Cycles: – Permits choosing whether Refresh Cycles will be stored or not. The field choices are:

Do Not Acquire (default) – This mode will reduce the number of Refresh cycles stored by the acquisition card to provide optimum use of the acquisition memory.

Acquire – Refresh Cycles will be stored.

5.0 CONFIGURING FOR READ / WRITE DATA ACQUISITION

IMPORTANT !

Prior to configuring your NEX-DDRII400 support package it is *strongly* recommended that Appendix A (“How DDR Data is Clocked”), section 5.2 (“Selecting DDR Read Sample Points”) and section 5.3 (“Selecting DDR Write Sample Points”) be read. This background information is very helpful in properly configuring the support.

5.1 Adjusting Input Thresholds for Proper Data Acquisition

The voltage threshold must be properly set on the TLA for proper acquisition of the DDR bus. We recommend that you verify the center point of the SDRAM CK0, any DDR strobe, and any DDR data bit. The CLK threshold should be set close to 0v because the clock is a differential signal. The threshold setting can be verified that it is correct by taking a TLA acquisition and verifying a 50% duty cycle on the clock by looking at the DDRCK2, DDRCK1 or DDRCK0 MagniVu trace. All other signals should be set close to center of the voltage swing. Please note that synchronous acquisition using a TLA7AxA or TLA7ABx card requires a valid data window of approximately 625ps.

Although you should measure and set the thresholds as described, you can start with a 1.1V threshold value for all signals except for TLA CK3 (DDRCK0), CK1 (DDRCLK2), and CK0 (DDRCK1), which should be set to 0.07V because they are differential signals. These values can be used as a starting point.

5.2 Selecting DDRII Read Sample Points

For the DDRII400 post-processing software to accurately show valid data it is necessary to choose the proper sample points to ensure that valid data is acquired when the software expects it. Since valid DDR Read data is straddled by the Strokes (see Figures 1 and 2), and the Strokes are phase-aligned with the DDR clock for Reads, the Setup & Hold sample point must be set for the valid data that occurs after the clock edge. The correct clock edge is determined by adding the CAS Latency to the Additive Latency which equals the number of clock cycles that Read data will be delayed from the Read command.

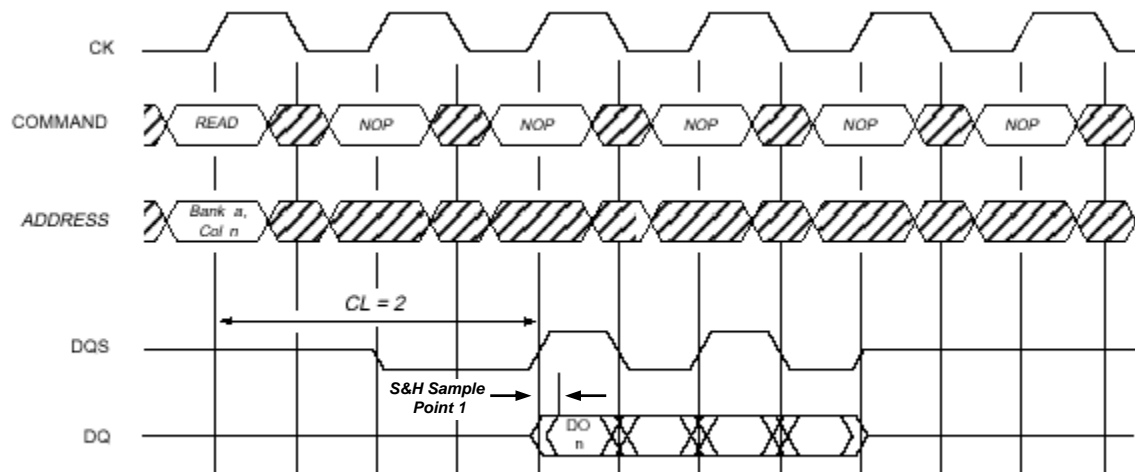


Figure 1- Read Cycle, CAS Latency = 2 cycles

For DDRII400 support data is acquired on both rising and falling clock edges so only one sample point (illustrated by *S&H Sample Point 1* in Figures 1 and 2) need be set.

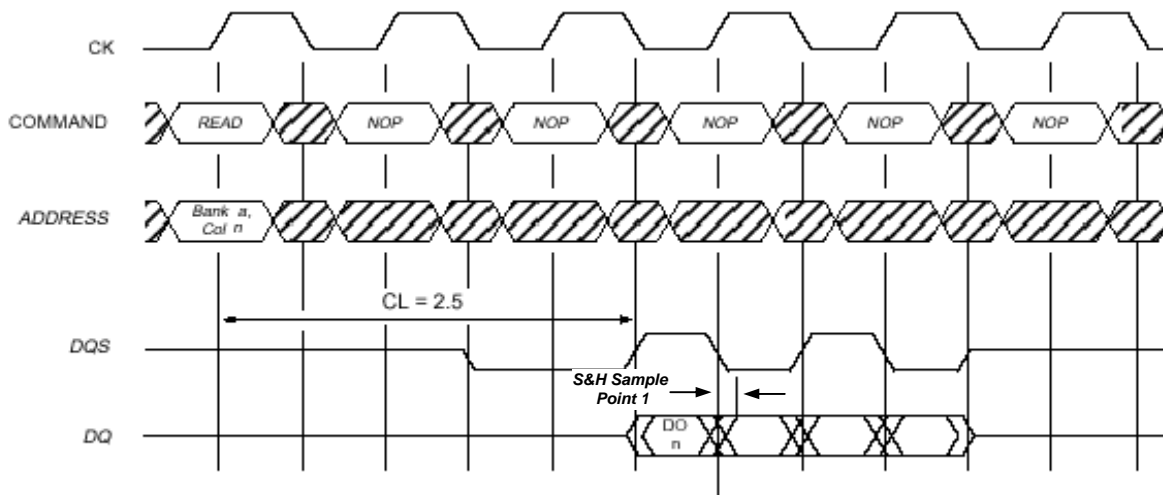


Figure 2- Read Cycle, CAS Latency = 2.5 cycles

5.3 Selecting DDRII Write Sample Points

Unlike valid DDR Read data, valid Write data is bisected by the Strobes. This is complicated by the delay from the Write command to the first Strobe rising edge varying anywhere from 75% to 125% of a clock cycle. These two extremes are illustrated in Figures 3 and 4.

IMPORTANT!

For valid Write data to be acquired and stored at the proper point for the DDRII400 software to interpret it, the Setup & Hold sample points ***must*** be determined relative to the appropriate rising clock edge after the Write command. The correct rising edge is determined by adding the CAS Latency and the Additive Latency and then subtracting one from their sum. If the Strobes transition from zeroes to ones before the clock edge then positive Setup and negative Hold values will be entered. If the Strobe transition after the edge then negative Setup and positive Hold values will be correct.

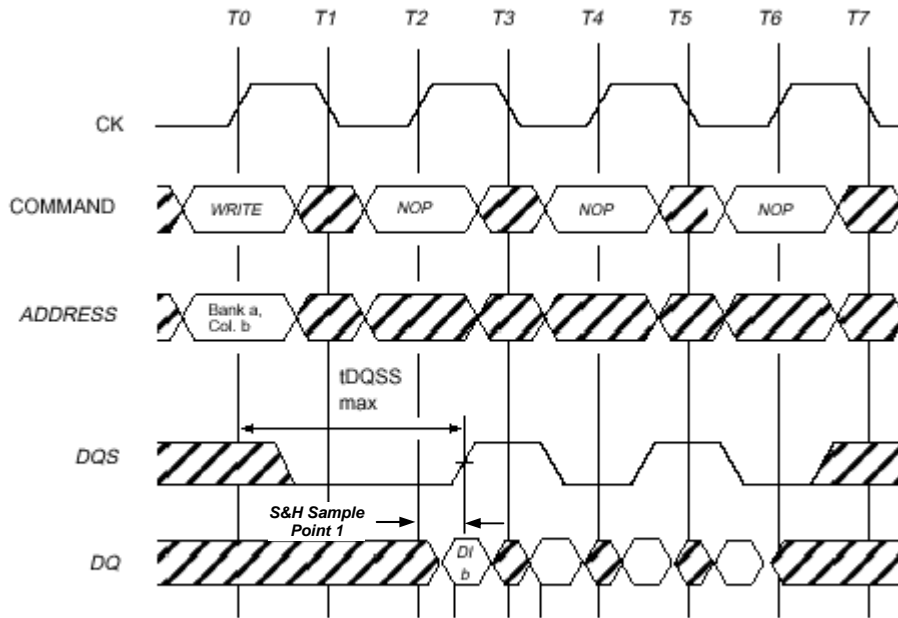


Figure 3- Write Cycle, Maximum Strobe Delay

For DDRII400 support data is acquired on the rising and falling clock edges so only one sample point (illustrated by *S&H Sample Point 1* in Figures 3 and 4 need be set. It is recommended that the Write Data sample points be set at or near the transition points of the Strobes. The sample point for the WrMasks group should also be set to the transition point of the Strobes (DQS signals) for proper acquisition, again as shown by *S&H Sample Point 1*.

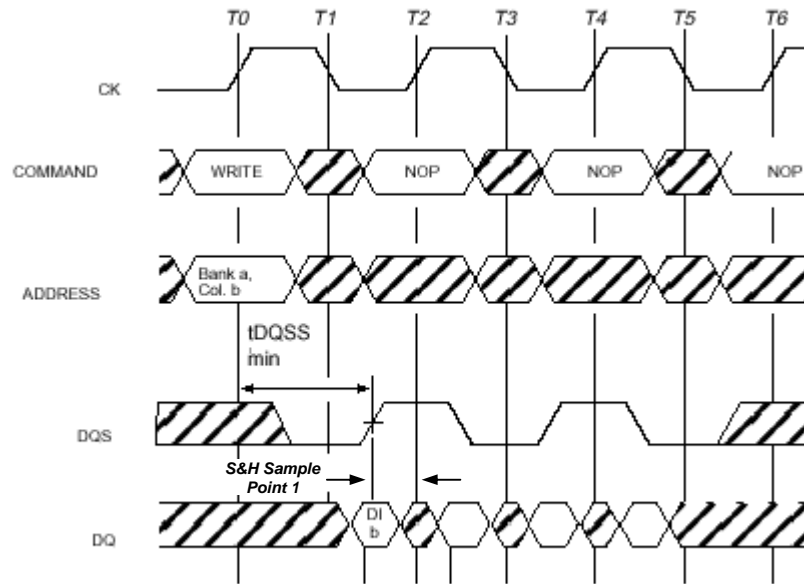


Figure 4- Write Cycle, Minimum Strobe Delay

5.4 DDRII400 Support

To adjust the Read Data group sample points first make an appropriate acquisition of Read data by triggering on a Read Command cycle. Then create a timing window display of MagniVu data and display the two 32-bit groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2). A sample waveform display of MagniVu Read data is shown in Figure 5. To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (note arrows in Figure 5).

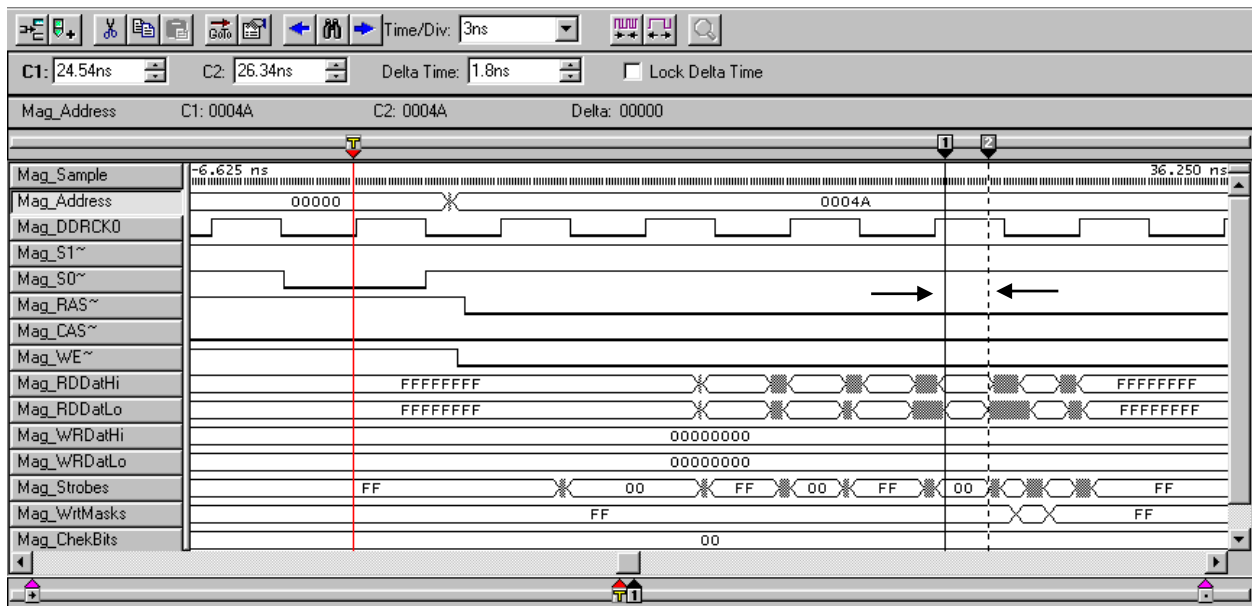


Figure 5- Locating Minimum Valid DDRII400 Read Data Window

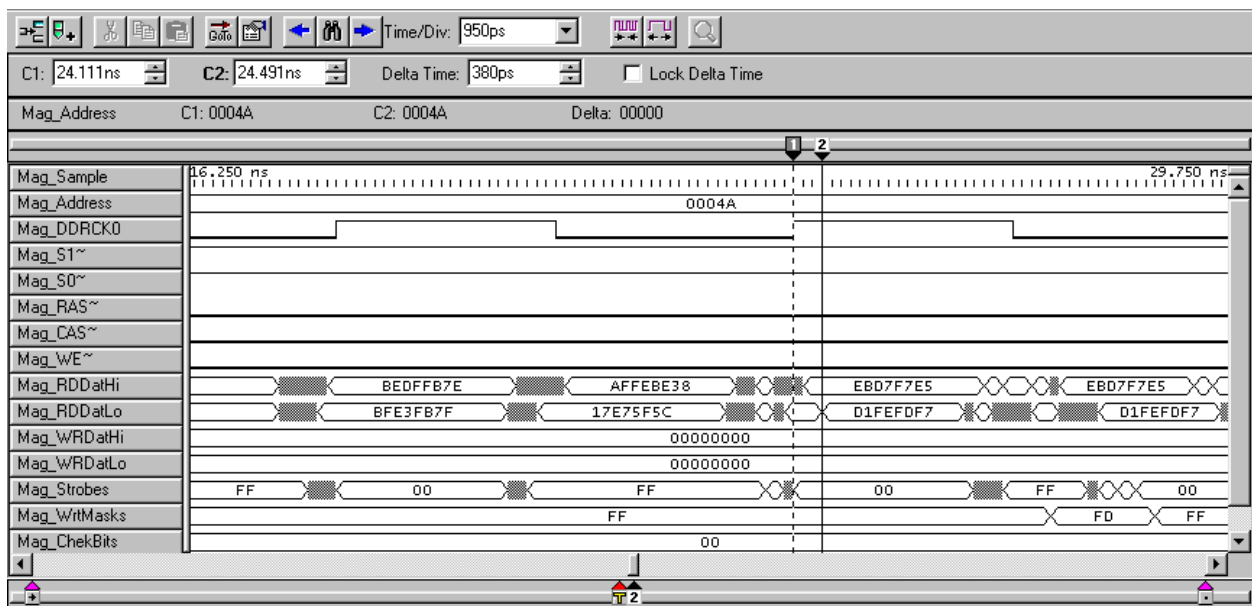


Figure 6- Measuring DDRII400 Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 6) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is ~380ps, meaning that a suitable Setup & Hold value would be -500ps/1.125ns. This sample point position must now be set for the RDDatHi and RDDatLo groups in the Setup window. This window is found by going to the LA Card's Setup window, then clicking on the **More** button to the right of the clock select field. The TLA acquisition cards require a valid data window of 625ps, and this window can be placed to begin from 16.25ns prior to the clock edge to 7.625ns after the edge in 125ps increments. Each 32-bit data group (RDDatHi and RDDatLo) will require its own value programmed from the measurements noted in the MagniVu window (Figure 7).

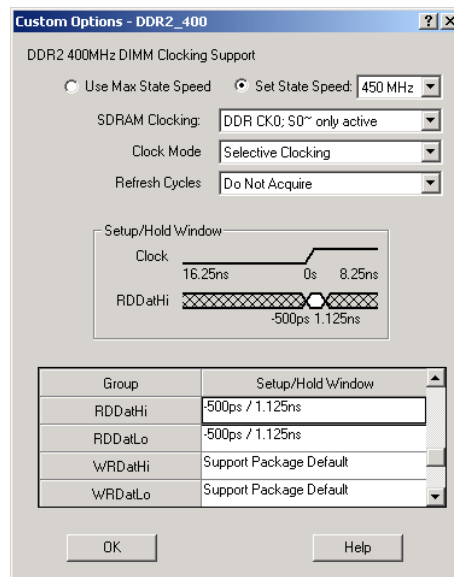


Figure 7- Setting DDRII400 Read Data Setup & Hold Sample Points

Setting the Setup & Hold values for acquiring Write data is similar, but the valid data point now more closely aligns with the Strobe edges. To adjust the Write Data group sample points first make an appropriate acquisition of Write data by triggering on a Write Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2).

Note: Because of the method used to acquire Write Data using the DDRII400 support, the Read Data group information must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A “How DDR Data is Clocked”.

A sample waveform display of MagniVu Write data is shown in Figure 8. To determine the sample point, locate the worst-case Setup & Hold timing of valid Write data during the acquired burst (note arrows in Figure 8). Refer to section 5.3 for important information on properly determining the Write data sample points.

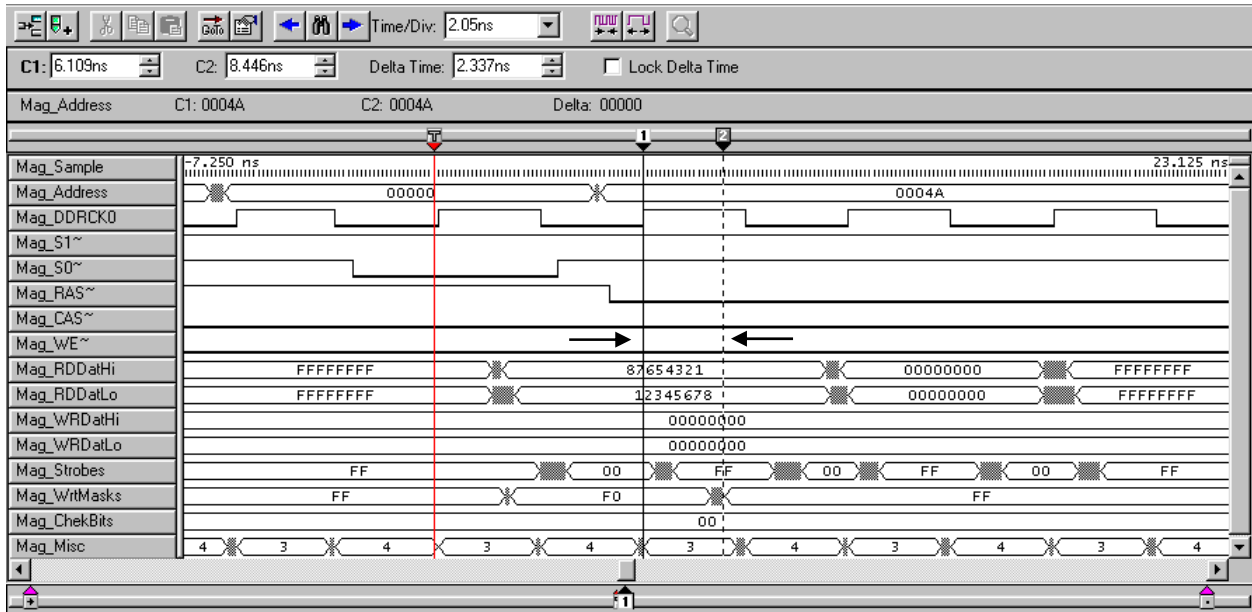


Figure 8- Locating Minimum Valid DDRII400 Write Data Window

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 9) and use the cursors to measure the time from the clock edge to the start of valid Write data. In this example the delay from edge to Strobe transition is ~875ps, meaning that a suitable Setup & Hold value would be $-875\text{ps}/1.5\text{ns}$. This sample point position must now be set for the WRDatHi and WRDatLo groups in the Setup window (Figure 10). Note that the WrtMasks group should have a Setup & Hold value that aligns with the transition of the Strobes.

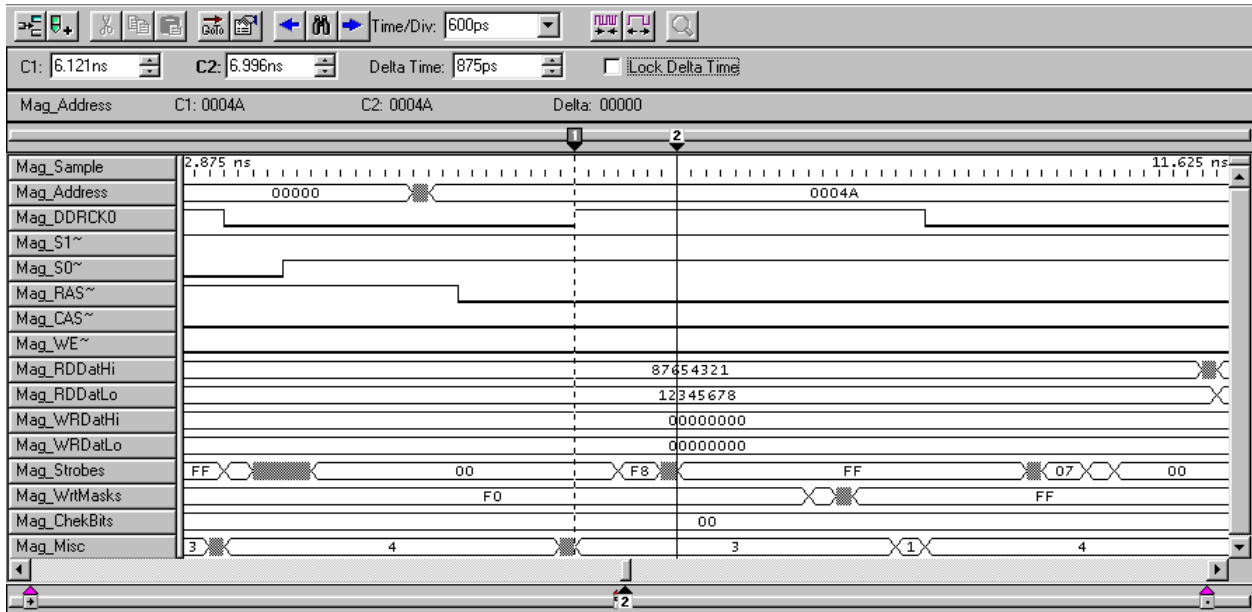


Figure 9- Measuring DDR2_400 Write Data Setup & Hold

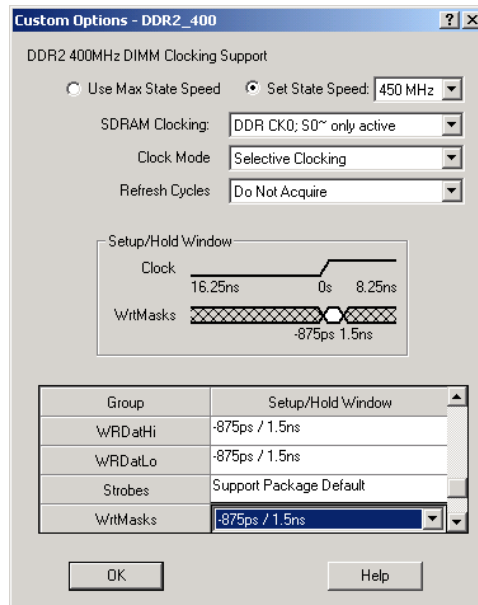


Figure 10- Setting DDR2_400 Write Data Setup & Hold Sample Points

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 11 shows these added data groups (DatByte7-0) added to the same Waveform display shown in Figure 8. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see Figure 12). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit or 4-bit groups make up a 32-bit group.

Note: Again, it is very important to remember that, because of the method used to acquire Write Data using the DDRII400 support, the Read Data group information must be used to determine the Write Data sample points. For further explanation of this process refer to Appendix A “How DDR Data is Clocked”.

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (RDDatHi, RDDatLo, WRDatHi or WRDatLo) be reset to “Support Package Default”. This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values – 625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

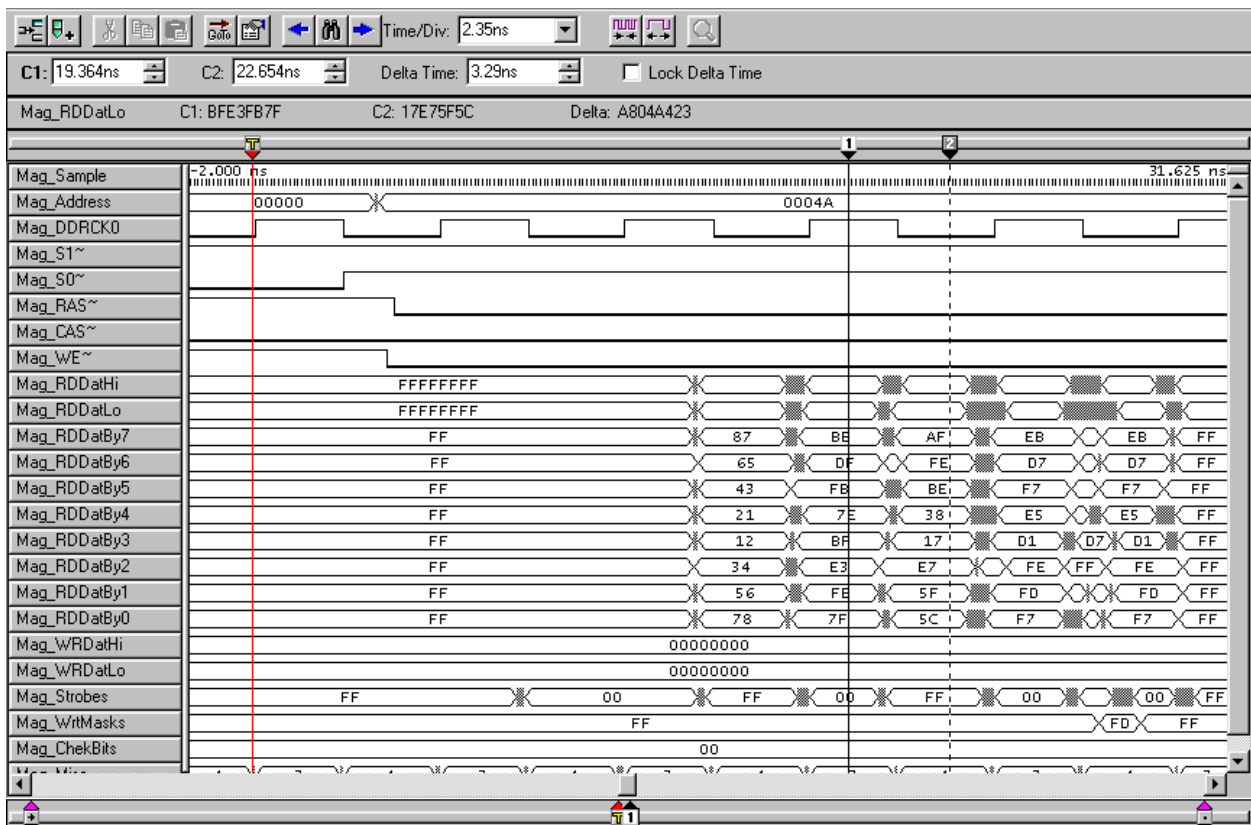


Figure 11- Viewing Individual 8-bit Read Data Groups

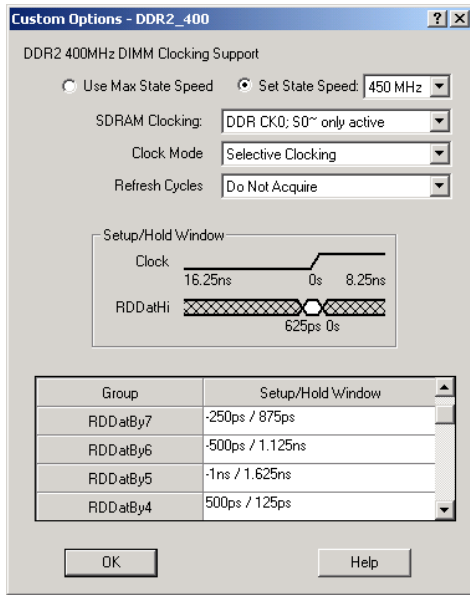


Figure 12- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

Note: Values shown are for illustration purposes only

6.0 VIEWING DATA

6.1 Viewing State Data on the TLA - General

After making an initial acquisition, the TLA will display the data in the Listing (State) format. A Symbol Table has been included in the support package for the Command data group (see Table 3). The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. The symbol file has been created to permit quickly showing the type of transaction that occurred on the DDR Bus - a Read, Write, Precharge, etc. This symbol information can also be used to trigger on a DDR cycle of interest.

It is important to note that changing the group, channel, or wiring of the Command group can result in incorrect symbol information being displayed.

| Symbol | Definition |
|------------------------------|-------------------|
| DESL--IGNORE_COMMAND--DATA? | 11 xxx |
| NOP--NO_OPERATION_(S0~) | x0 111 |
| NOP--NO_OPERATION_(S1~) | 0x 111 |
| BST--BURST_STOP_(S0~) | x0 110 |
| BST--BURST_STOP_(S1~) | 0x 110 |
| READ--COL_ADDR_READ_(S0~) | x0 101 |
| READ--COL_ADDR_READ_(S1~) | 0x 101 |
| WRITE--COL_ADDR_WRITE_(S0~) | x0 100 |
| WRITE--COL_ADDR_WRITE_(S1~) | 0x 100 |
| ACTV-- | x0 011 |
| ROW_ADDRESS_STROBE_(S0~) | |
| ACTV-- | 0x 011 |
| ROW_ADDRESS_STROBE_(S1~) | |
| PRE-- | x0 010 |
| PRECHARGE_SELECT_BANK_(S0~) | |
| PRE-- | 0x 010 |
| PRECHARGE_SELECT_BANK_(S1~) | |
| PALL-- | x0 010 |
| PRECHARGE_ALL_BANK_(S0~) | |
| PALL-- | 0x 010 |
| PRECHARGE_ALL_BANK_(S1~) | |
| REF--REFRESH_(S0~) | x0 001 |
| REF--REFRESH_(S1~) | 0x 001 |
| MRS--MODE_REGISTER_SET_(S0~) | x0 000 |
| MRS--MODE_REGISTER_SET_(S1~) | 0x 000 |

Table 3- 400DDR2S/M Command Symbol Table

Signals, left-to-right: S1~, S0~, RAS~, CAS~, WE~

6.2 Viewing DDRII400 Data

The DDRII400 support packages display the Address, RDDatHi, RDDatLo, WRDatHi, WRDatLo, WrtMsk, and Strobes group data in hexadecimal format; Command, ChekBits, Misc, and the Data Byte (RDDatByx and WRDatByx) or Data Nibble (RDDatNibx and WRDatNibx) groups default to OFF.

The Command group is suppressed because its function is replaced with a column labeled “DDRII400 Mnemonics”. The DDRII400 support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 13 shows the default display where all DDR data is displayed.

| Sample | DDRHS-RW Address | DDRHS-RW RDDatHi | DDRHS-RW RDDatLo | DDRHS-RW WRDatHi | DDRHS-RW WRDatLo | DDRHS-RW Mnemonics | DDRHS-RW Strobes | DDRHS-RW WrtMasks | Command | Timestamp |
|--------|------------------|------------------|------------------|------------------|------------------|-----------------------------------|------------------|-------------------|---------|--------------|
| 2015 | 003C8 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11100 | 2.875 ns |
| 2016 | 003C8 | FEFF66E | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11100 | 3.000 ns |
| 2017 | 003C8 | 6E4F646E | 65706544 | 6E4F646E | 65706544 | DESL - IGNORE COMMAND | FF | 00 | 11100 | 3.000 ns |
| 2018 | 0044A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 38.875 ns |
| 2019 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | REF - REFRESH (S0~) | FF | FF | 10001 | 17.875 ns |
| 2020 | 00000 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | ACTV - ROW ADDRESS STROBE (S0~) | FF | FF | 10011 | 395.000 ns |
| 2021 | 003D0 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | READ - COL ADDR READ (S0~) | FF | FF | 10101 | 18.000 ns |
| 2022 | 003D0 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | (UNKNOWN) | FF | FF | 10101 | 2.875 ns |
| 2023 | 003D4 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11101 | 3.125 ns |
| 2024 | 003D4 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11101 | 2.875 ns |
| 2025 | 003D4 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | READ - COL ADDR READ (S0~) | 00 | FF | 10101 | 3.125 ns |
| 2026 | 003D4 | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | 00 | FF | 10101 | 2.875 ns |
| 2027 | 0004A | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | FF | F9 | 11010 | 3.000 ns |
| 2028 | 0004A | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | 00 | FF | 11010 | 3.000 ns |
| 2029 | 0004A | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2030 | 0004A | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | 00 | FF | 11010 | 3.000 ns |
| 2031 | 0004A | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | 00 | FF | 11010 | 3.000 ns |
| 2032 | 0004A | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | 00 | FF | 11010 | 3.000 ns |
| 2033 | 0004A | 00000000 | 00000000 | 00000000 | 00000000 | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2034 | 0004A | FFFFFFFF | 7EF3FFFF | 00000000 | 00000000 | DESL - IGNORE COMMAND | 00 | FF | 11010 | 3.000 ns |
| 2035 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | 0E128C08 | DESL - IGNORE COMMAND | 02 | FF | 11010 | 3.000 ns |
| 2036 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2037 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2038 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 2.875 ns |
| 2039 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2040 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.125 ns |
| 2041 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 2.875 ns |
| 2042 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2043 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 4.590,000 us |
| 2044 | 0044A | 00000000 | 00000000 | 00000000 | 00000000 | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 731.625 ns |
| 2045 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | 3EC7DFFF | REF - REFRESH (S0~) | FF | FF | 10001 | 17.875 ns |
| 2046 | 00000 | FFFFFFFF | FFFFFFFF | FFFFFFFF | 3E032005 | ACTV - ROW ADDRESS STROBE (S0~) | FE | FF | 10011 | 197.625 ns |
| 2047 | 00088 | 006E0064 | 80FBFFFF | FFFFFFFF | FFFFFFFF | WRITE - COL ADDR WRITE (S0~) | FF | FF | 10100 | 18.000 ns |
| 2048 | 00088 | 006E0064 | 00690061 | 006E0064 | 00690061 | (UNKNOWN) | FF | 00 | 10100 | 3.000 ns |
| 2049 | 0008C | 006E0064 | 00690061 | 006E0064 | 00690061 | WRITE DATA | 00 | 00 | 11100 | 3.000 ns |
| 2050 | 0008C | 00070000 | 00540000 | 00070000 | 00540000 | WRITE DATA | FF | 00 | 11100 | 2.875 ns |
| 2051 | 0008C | 00004188 | 00070510 | 00004188 | 00570510 | WRITE - COL ADDR WRITE (S0~) | 00 | 00 | 10100 | 3.000 ns |
| 2052 | 0008C | 00004188 | 00070510 | 00004188 | 00570510 | WRITE DATA | 00 | 00 | 10100 | 3.000 ns |
| 2053 | 00080 | 00003948 | 00003968 | 00003948 | 000079EC | WRITE DATA | 00 | 00 | 11100 | 3.000 ns |
| 2054 | 00080 | 00004478 | 000043C8 | 00004478 | 000073E8 | WRITE DATA | FF | 00 | 11100 | 3.000 ns |
| 2055 | 00080 | 00003840 | 00003850 | 00003840 | 000078D8 | WRITE - COL ADDR WRITE (S0~) | 00 | 00 | 10100 | 3.000 ns |
| 2056 | 00080 | 00003840 | 00003850 | 00003840 | 000078D8 | WRITE DATA | 00 | 00 | 10100 | 3.000 ns |
| 2057 | 00084 | 00003968 | 000043AC | 00003968 | 000047EC | WRITE DATA | 00 | 00 | 11100 | 3.000 ns |
| 2058 | 00084 | 000043C8 | 00003948 | 000043C8 | 000038CC | WRITE DATA | FF | 00 | 11100 | 3.000 ns |
| 2059 | 00084 | 000039F4 | 000043F4 | 000039F4 | 000078FC | WRITE - COL ADDR WRITE (S0~) | 00 | 00 | 10100 | 3.000 ns |
| 2060 | 00084 | 000039F4 | 000043F4 | 000039F4 | 000078FC | WRITE DATA | 00 | 00 | 10100 | 3.000 ns |
| 2061 | 004CE | 0000384A | 000038B4 | 0000384A | 000038FC | WRITE DATA | 00 | 00 | 11010 | 3.000 ns |
| 2062 | 0044A | 00420076 | 00000053 | 00420076 | 000038F7 | WRITE DATA | FF | 00 | 11010 | 2.875 ns |
| 2063 | 0004A | 00070528 | 00080002 | 00070568 | 00080053 | WRITE DATA | 00 | 00 | 11010 | 3.000 ns |
| 2064 | 0004A | 00720073 | 00070528 | 00720073 | 000F052A | WRITE DATA | FF | 00 | 11010 | 3.125 ns |
| 2065 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | 00070528 | DESL - IGNORE COMMAND | 00 | 00 | 11010 | 3.000 ns |
| 2066 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 2.875 ns |
| 2067 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2068 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2069 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 3.000 ns |
| 2070 | 0004A | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | (UNKNOWN) | FF | FF | 10010 | 3.000 ns |

Figure 13- DDRII400 State Display - Show All Data? = Yes

To change the display it is necessary to bring up the window’s Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in Figure 14.

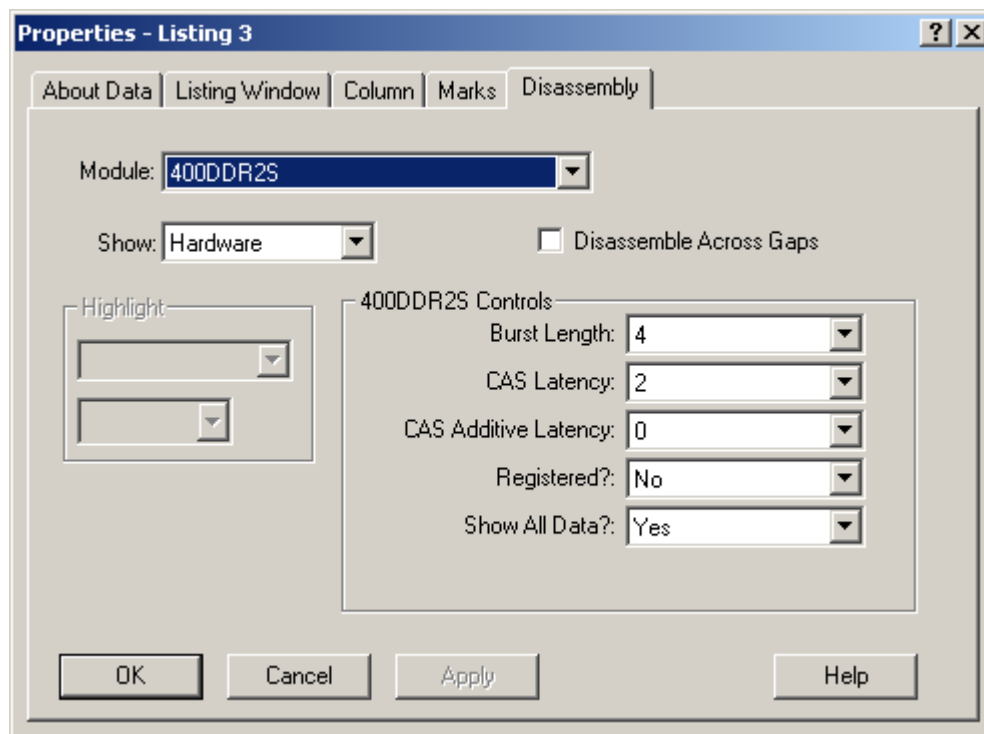


Figure 14- DDRII400 Disassembly Properties

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

Burst Length – permits setting the burst length for Read and Write data. Valid choices are 4 (the default) and 8. This value must be set properly for all valid Read and Write data to be displayed.

CAS Latency – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 2 (default), 3, 4, or 5 cycles.

CAS Additive Latency – additional latency for data cycles. This value must also be set properly for valid Read and Write Data to be displayed. Valid choices are 0 (default), 1, 2, 3, or 4 cycles.

Registered? – must be set to reflect whether or not Registered DDR memory is used. Default is No. When set to Yes an additional clock cycle delay is added to CAS Latency and to valid Read and Write Data tagging.

Show All Data? – permits choosing between displaying all DDR data (default), including Invalid Read / Write and Command data, and showing only valid Data and Command data.

When setting **Show All Data?** to No, the display in Figure 13 then becomes the display in Figure 15. This allows the user to see at a glance the valid information on the bus.

| Sample | DDRHS-RW Address | DDRHS-RW RDDatHi | DDRHS-RW RDDatLo | DDRHS-RW WRDAtHi | DDRHS-RW WRDAtLo | DDRHS-RW Memonics | DDRHS-RW Strokes | DDRHS-RW WrtMasks | Command | Timestamp |
|--------|------------------|------------------|------------------|------------------|------------------|-----------------------------------|------------------|-------------------|---------|--------------|
| 2015 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11100 | 2.875 ns |
| 2016 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11100 | 3.000 ns |
| 2017 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11100 | 3.000 ns |
| 2018 | 0004A | ----- | ----- | ----- | ----- | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 38.875 ns |
| 2019 | 00000 | ----- | ----- | ----- | ----- | REF - REFRESH (S0~) | FF | FF | 10001 | 17.875 ns |
| 2020 | 00000 | ----- | ----- | ----- | ----- | ACTV - ROW ADDRESS STROBE (S0~) | FF | FF | 10011 | 395.000 ns |
| 2021 | 003D0 | ----- | ----- | ----- | ----- | READ - COL ADDR READ (S0~) | FF | FF | 10101 | 18.000 ns |
| 2022 | ----- | ----- | ----- | ----- | ----- | (UNKNOWN) | FF | FF | 10101 | 2.875 ns |
| 2023 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11101 | 3.125 ns |
| 2024 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11101 | 2.875 ns |
| 2025 | 003D4 | ----- | ----- | ----- | ----- | READ - COL ADDR READ (S0~) | 00 | FF | 10101 | 3.125 ns |
| 2026 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | 00 | FF | 10101 | 2.875 ns |
| 2027 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | F9 | 11010 | 3.000 ns |
| 2028 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | 00 | FF | 11010 | 3.000 ns |
| 2029 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2030 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | 00 | FF | 11010 | 3.000 ns |
| 2031 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2032 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | 00 | FF | 11010 | 3.000 ns |
| 2033 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2034 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | 00 | FF | 11010 | 3.000 ns |
| 2035 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | 02 | FF | 11010 | 3.000 ns |
| 2036 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2037 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2038 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 2.875 ns |
| 2039 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2040 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.125 ns |
| 2041 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 2.875 ns |
| 2042 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2043 | 0004A | ----- | ----- | ----- | ----- | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 4.590,000 us |
| 2044 | 0044A | ----- | ----- | ----- | ----- | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 731.625 ns |
| 2045 | 0004A | ----- | ----- | ----- | ----- | REF - REFRESH (S0~) | FF | FF | 10001 | 17.875 ns |
| 2046 | 00000 | ----- | ----- | ----- | ----- | ACTV - ROW ADDRESS STROBE (S0~) | FF | FF | 10011 | 197.625 ns |
| 2047 | 00088 | ----- | ----- | ----- | ----- | WRITE - COL ADDR WRITE (S0~) | FF | FF | 10100 | 18.000 ns |
| 2048 | ----- | ----- | ----- | ----- | ----- | (UNKNOWN) | FF | 00 | 10100 | 3.000 ns |
| 2049 | ----- | ----- | 006E0064 | 00690061 | 00690061 | WRITE DATA | 00 | 00 | 11100 | 3.000 ns |
| 2050 | ----- | ----- | 00070000 | 00750061 | 00750061 | WRITE DATA | FF | 00 | 11100 | 2.875 ns |
| 2051 | 0008C | ----- | ----- | ----- | ----- | WRITE - COL ADDR WRITE (S0~) | 00 | 00 | 10100 | 3.000 ns |
| 2052 | ----- | ----- | 000041E8 | 00570510 | 00570510 | WRITE DATA | 00 | 00 | 10100 | 3.000 ns |
| 2053 | ----- | ----- | 000043AC | 000745B4 | 000745B4 | WRITE DATA | FF | 00 | 10100 | 3.000 ns |
| 2054 | ----- | ----- | 00003948 | 000079EC | 000079EC | WRITE DATA | 00 | 00 | 11100 | 3.000 ns |
| 2055 | 00080 | ----- | ----- | ----- | ----- | WRITE - COL ADDR WRITE (S0~) | 00 | 00 | 10100 | 3.000 ns |
| 2056 | ----- | ----- | 00003B40 | 00007BD8 | 00007BD8 | WRITE DATA | 00 | 00 | 10100 | 3.000 ns |
| 2057 | ----- | ----- | 00003B74 | 0000375C | 0000375C | WRITE DATA | FF | 00 | 10100 | 3.000 ns |
| 2058 | ----- | ----- | 00003968 | 000047EC | 000047EC | WRITE DATA | 00 | 00 | 11100 | 3.000 ns |
| 2059 | 00084 | ----- | ----- | ----- | ----- | WRITE - COL ADDR WRITE (S0~) | 00 | 00 | 10100 | 3.000 ns |
| 2060 | ----- | ----- | 000039F4 | 00007BFC | 00007BFC | WRITE DATA | 00 | 00 | 10100 | 3.000 ns |
| 2061 | ----- | ----- | 0000441C | 00007BFC | 00007BFC | WRITE DATA | FF | 00 | 11010 | 3.000 ns |
| 2062 | ----- | ----- | 000035A4 | 000038FC | 000038FC | WRITE DATA | 00 | 00 | 11010 | 2.875 ns |
| 2063 | ----- | ----- | 00420076 | 000038F7 | 000038F7 | WRITE DATA | FF | 00 | 11010 | 2.875 ns |
| 2064 | ----- | ----- | 00070568 | 00080053 | 00080053 | WRITE DATA | 00 | 00 | 11010 | 3.000 ns |
| 2065 | ----- | ----- | 00720073 | 000F052A | 000F052A | WRITE DATA | FF | 00 | 11010 | 3.125 ns |
| 2066 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | 00 | 00 | 11010 | 3.000 ns |
| 2067 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 2.875 ns |
| 2068 | ----- | ----- | ----- | ----- | ----- | DESL - IGNORE COMMAND | FF | FF | 11010 | 3.000 ns |
| 2069 | 0004A | ----- | ----- | ----- | ----- | PRE - PRECHARGE SELECT BANK (S0~) | FF | FF | 10010 | 3.000 ns |
| 2070 | ----- | ----- | ----- | ----- | ----- | (UNKNOWN) | FF | FF | 10010 | 3.000 ns |

Figure 15- 400DDR2S State Display - Show All Data? = No

In addition to the Disassembly Properties selections discussed earlier, changing the settings in the **Show** field result in display changes as well:

- Hardware** – displays all acquired cycles
- Software** – suppresses all idle or wait cycles
- Control Flow** – shows Address Command and valid Read / Write data cycles
- Subroutine** – shows valid Read / Write data cycles only

Changing the Show field setting in the display of Figure 15 from Hardware to Control Flow results in the display of Figure 16 where only Row and Column Address commands and valid

data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

| Sample | DDRHS-RW Address | DDRHS-RW RDDatHi | DDRHS-RW RDDatLo | DDRHS-RW WRDatHi | DDRHS-RW WRDatLo | DDRHS-RW Mnemonics | DDRHS-RW Strokes | DDRHS-RW WrtMasks | Command | Timestamp |
|--------|------------------|------------------|------------------|------------------|------------------|---------------------------------|------------------|-------------------|---------|--------------|
| 1993 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 10101 | 3.000 ns |
| 1994 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11101 | 3.000 ns |
| 1995 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11101 | 3.000 ns |
| 1996 | 003C8 | ----- | 00000000 | ----- | ----- | READ - COL ADDR READ (SO~) | FF | FF | 10101 | 3.000 ns |
| 1997 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 10101 | 3.000 ns |
| 1998 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11101 | 3.000 ns |
| 1999 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11101 | 3.000 ns |
| 2000 | 003CC | ----- | 00000000 | ----- | ----- | READ - COL ADDR READ (SO~) | FF | FF | 10101 | 3.000 ns |
| 2001 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 10101 | 2.875 ns |
| 2002 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2003 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2004 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 10010 | 3.000 ns |
| 2005 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 10010 | 3.000 ns |
| 2006 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11011 | 3.000 ns |
| 2007 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11011 | 3.000 ns |
| 2008 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11011 | 3.000 ns |
| 2009 | 00000 | ----- | 00000000 | ----- | ----- | ACTV - ROW ADDRESS STROBE (SO~) | FF | FF | 10011 | 478.500 ns |
| 2021 | 003D0 | ----- | 00000000 | ----- | ----- | READ - COL ADDR READ (SO~) | FF | FF | 10101 | 18.000 ns |
| 2025 | 003D4 | ----- | 00000000 | ----- | ----- | READ - COL ADDR READ (SO~) | FF | FF | 10101 | 12.000 ns |
| 2026 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 10101 | 2.875 ns |
| 2027 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2028 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2029 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2030 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2031 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2032 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2033 | ----- | 00000000 | 00000000 | ----- | ----- | READ DATA | FF | FF | 11010 | 3.000 ns |
| 2046 | 00000 | ----- | 00000000 | ----- | ----- | ACTV - ROW ADDRESS STROBE (SO~) | FF | FF | 10011 | 5.564,000 us |
| 2047 | 00088 | ----- | 00000000 | ----- | ----- | WRITE - COL ADDR WRITE (SO~) | FF | FF | 10100 | 18.000 ns |
| 2049 | ----- | 00E0064 | 0069064 | 0069064 | 0069064 | WRITE DATA | FF | FF | 11100 | 6.000 ns |
| 2050 | ----- | 00070000 | 00750061 | 00750061 | 00750061 | WRITE DATA | FF | FF | 11100 | 2.875 ns |
| 2051 | 0008C | ----- | 00000000 | ----- | ----- | WRITE - COL ADDR WRITE (SO~) | FF | FF | 10100 | 3.000 ns |
| 2052 | ----- | 000041B8 | 00570510 | 00570510 | 00570510 | WRITE DATA | FF | FF | 10100 | 3.000 ns |
| 2053 | ----- | 000043AC | 000745B4 | 000745B4 | 000745B4 | WRITE DATA | FF | FF | 11100 | 3.000 ns |
| 2054 | ----- | 00003948 | 000079EC | 000079EC | 000079EC | WRITE DATA | FF | FF | 11100 | 3.000 ns |
| 2055 | 00080 | ----- | 00004478 | 000073E8 | 000073E8 | WRITE DATA | FF | FF | 11100 | 3.000 ns |
| 2056 | ----- | 00003840 | 00007B08 | 00007B08 | 00007B08 | WRITE DATA | FF | FF | 10100 | 3.000 ns |
| 2057 | ----- | 00003874 | 0000375C | 0000375C | 0000375C | WRITE DATA | FF | FF | 11100 | 3.000 ns |
| 2058 | ----- | 00003968 | 000047EC | 000047EC | 000047EC | WRITE DATA | FF | FF | 11100 | 3.000 ns |
| 2059 | 00084 | ----- | 000043C8 | 00003BCC | 00003BCC | WRITE DATA | FF | FF | 10100 | 3.000 ns |
| 2060 | ----- | 000039F4 | 00007BFC | 00007BFC | 00007BFC | WRITE DATA | FF | FF | 10100 | 3.000 ns |
| 2061 | ----- | 0000441C | 00007BFC | 00007BFC | 00007BFC | WRITE DATA | FF | FF | 11010 | 3.000 ns |
| 2062 | ----- | 000038A4 | 000038FC | 000038FC | 000038FC | WRITE DATA | FF | FF | 11010 | 2.875 ns |
| 2063 | ----- | 00420076 | 000038F7 | 000038F7 | 000038F7 | WRITE DATA | FF | FF | 11010 | 3.000 ns |
| 2064 | ----- | 00070568 | 00080053 | 00080053 | 00080053 | WRITE DATA | FF | FF | 11010 | 3.125 ns |
| 2077 | 00000 | ----- | 00720073 | 000F052A | 000F052A | WRITE DATA | FF | FF | 10011 | 116.750 ns |
| 2078 | 00088 | ----- | ----- | ----- | ----- | ACTV - ROW ADDRESS STROBE (SO~) | FF | FF | 10100 | 18.000 ns |
| 2080 | ----- | 00000000 | 005D0050 | 005D0050 | 005D0050 | WRITE DATA | FF | FF | 11100 | 6.000 ns |
| 2081 | ----- | 00000000 | 005D0050 | 005D0050 | 005D0050 | WRITE DATA | FF | FF | 11100 | 3.000 ns |
| 2082 | 0008C | ----- | ----- | ----- | ----- | WRITE - COL ADDR WRITE (SO~) | FF | FF | 10100 | 3.000 ns |
| 2083 | ----- | 00000000 | 00000000 | 00000000 | 00000000 | WRITE DATA | FF | FF | 10100 | 3.000 ns |
| 2084 | ----- | 00000000 | 00000000 | 00000000 | 00000000 | WRITE DATA | FF | FF | 11100 | 3.000 ns |

Figure 16- 400DDR2S State Display - Show Control Flow

6.3 400DDR2S/M Mnemonics Description

Table 4 gives a brief description of each of the text lines displayed in the post-processing software display.

| Mnemonic | Description |
|-----------------------------------|---|
| ACTV - ROW ADDRESS STROBE (S0~) | Active command – activate a row in a bank for subsequent access (chip select 0) |
| ACTV - ROW ADDRESS STROBE (S1~) | Active command – activate a row in a bank for subsequent access (chip select 1) |
| BST - BURST STOP (S0~) | Burst Terminate command – truncate current Read burst (chip select 0) |
| BST - BURST STOP (S1~) | Burst Terminate command – truncate current Read burst (chip select 1) |
| DESL - IGNORE COMMAND | Deselect function – no new command |
| MRS - MODE REGISTER SET (S0~) | Mode Register Set command – mode register load (chip select 0) |
| MRS - MODE REGISTER SET (S1~) | Mode Register Set command – mode register load (chip select 1) |
| NOP - NO OPERATION (S0~) | No Operation command (chip select 0) |
| NOP - NO OPERATION (S1~) | No Operation command (chip select 1) |
| PRE - PRECHARGE SELECT BANK (S0~) | Precharge command (chip select 0) |
| PRE - PRECHARGE SELECT BANK (S1~) | Precharge command (chip select 1) |
| READ - COL ADDR READ (S0~) | Read command – initiates a burst read access to active row (chip select 0) |
| READ - COL ADDR READ (S1~) | Read command – initiates a burst read access to active row (chip select 1) |
| READ DATA | Valid Read data on the bus |
| REF - REFRESH (S0~) | Self Refresh command (chip select 0) |
| REF - REFRESH (S1~) | Self Refresh command (chip select 1) |
| WRITE - COL ADDR WRITE (S0~) | Write command – initiates a burst write access to active row (chip select 0) |
| WRITE - COL ADDR WRITE (S1~) | Write command – initiates a burst write access to active row (chip select 1) |
| WRITE DATA | Valid Write data on the bus |
| DDRCK0, DDRCK1, & DDRCK2 INACTIVE | No active clock detected by software |
| (UNKNOWN) | Command Cycle on falling edge of clock |

Table 4- 400DDR2S/M Mnemonics Definition

6.4 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: DDRHS (or DDRHS_RW) and DDR-MagniVu (or DDRII400-MagniVu). The first (DDRHS or DDRII400) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, DDR-MagniVu (or DDRII400-MagniVu), will show all of the channels in 8GHz MagniVu mode, so that edge relationships can be examined around the MagniVu trigger point. MagniVu is very useful and in some cases necessary to see/resolve DDR data. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

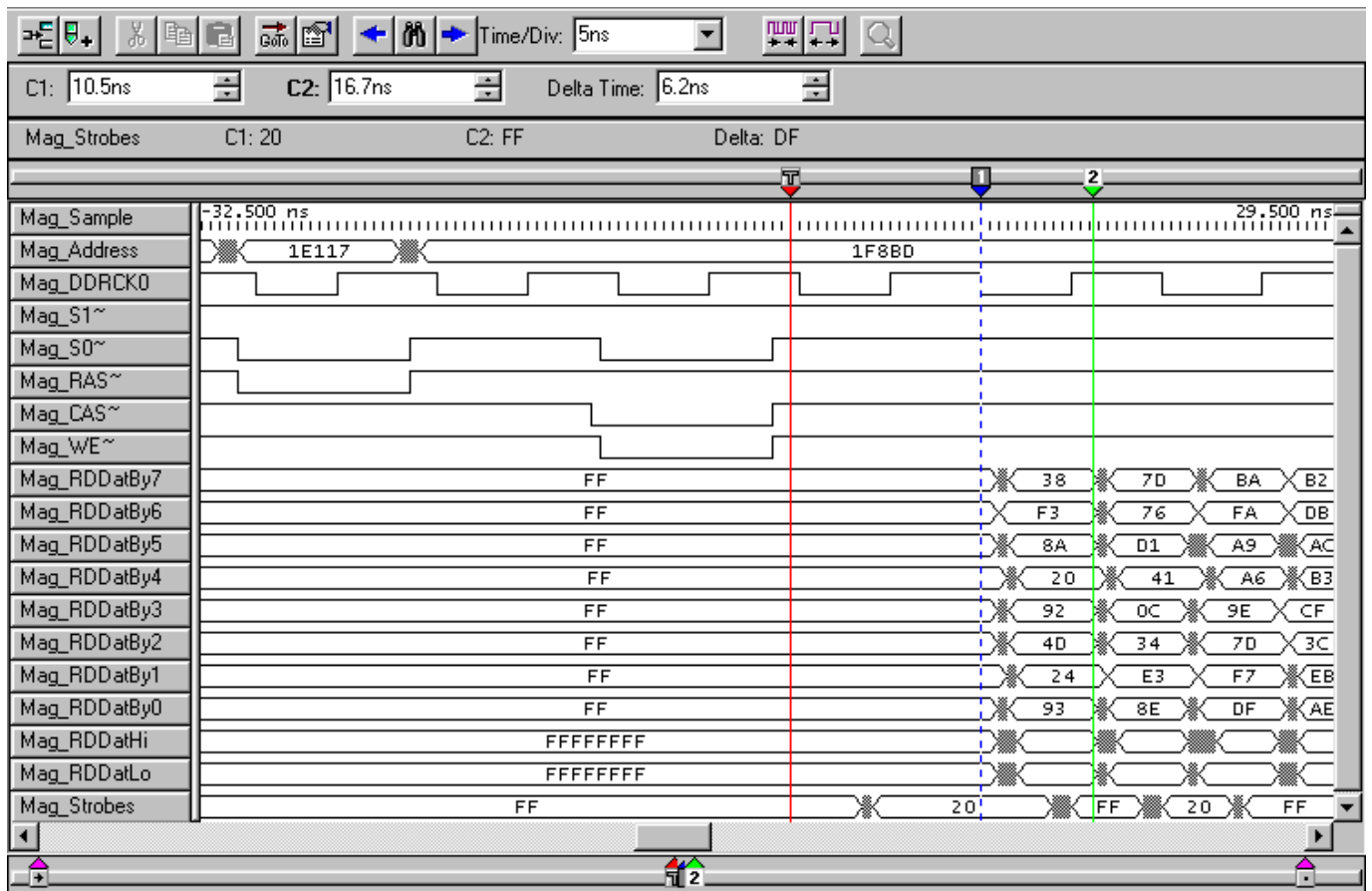


Figure 17- 400DDR2S MagniVu Display on TLA

7.0 HINTS & TIPS

7.1 Triggering on a Command using 400DDR2S/M

The DDRII400 support package clocks data into the logic analyzer on both the rising and falling edges of the selected DDR Clock. Command information is only valid on the rising edge of the clock, but it is very possible (even likely) that valid information is also available on the falling edge of the clock preceding the Command's valid rising edge. This can result in a false trigger of the TLA. With the DDRII400 post-processing software such a cycle (falling edge of DDR Clock with valid Command data) is labeled as an Unknown cycle. These cycles would be filtered out (suppressed) when changing the Disassembly Properties display mode to something other than Hardware, resulting in a Trigger position that is hidden from the user.

To eliminate this problem it is suggested that a trigger condition be defined that ANDs the desired Command with the DDR Clock channel being used for acquisition in a LOW state (see Figure 18). (Since the data stored by the TLA reflects its state before the acquisition clock occurs the DDR Clock is stored as a LOW for a rising clock edge and as a HIGH for a falling clock edge.) Figure 19 shows the actual Trigger Clause definition used in the trigger program shown in Figure 18.

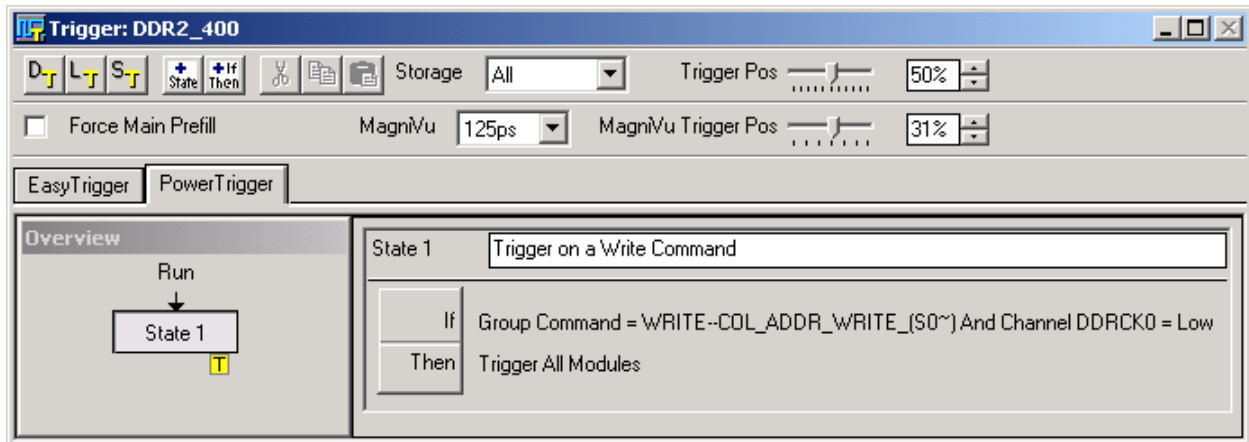


Figure 18- Recommended DDRII400 Command Trigger

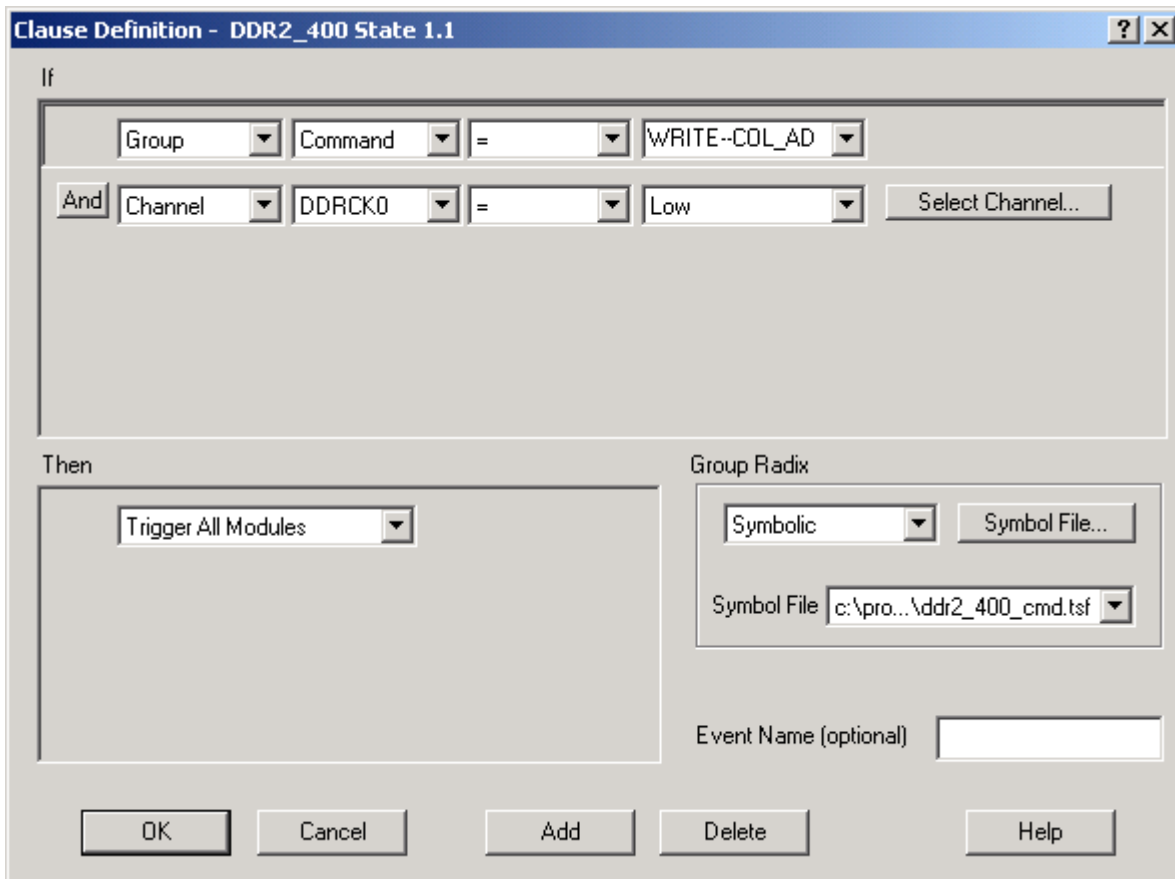


Figure 19- Recommended DDRII400 Command Trigger - Detail

7.2 Capturing MRS (Mode Register Set) Data

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the DDRII400 support for the post-processing software to properly decode the acquisitions. The TLA trigger shown in Figure 20 can be used to acquire the MRS cycles when using either of these supports.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

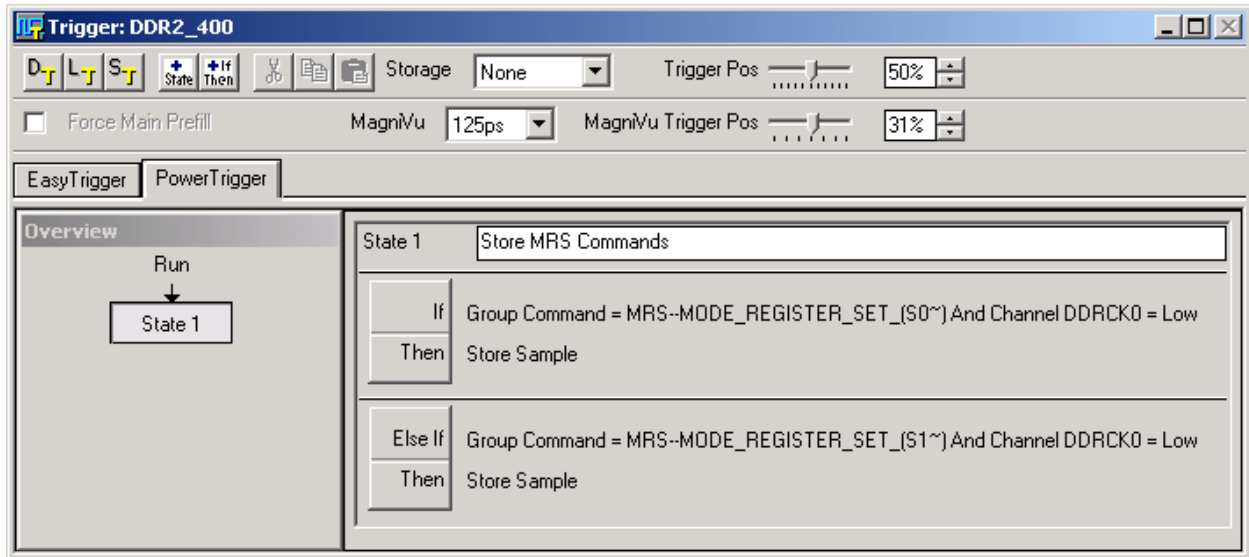


Figure 20- DDRII400 MRS Trigger

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in Figure 21. The last acquired MRS cycle will reflect the settings used in the DDR target – in this case, a CAS latency of 2 cycles with a Burst length of 8.

| Sample | DDRHS-RW Address | DDRHS-RW RDDatHi | DDRHS-RW RDDatLo | DDRHS-RW WRDatHi | DDRHS-RW WRDatLo | DDRHS-RW Mnemonics | DDRi Strc |
|--------|------------------|------------------|------------------|------------------|------------------|-------------------------------|-----------|
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Normal MRS | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Normal Operation | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Latency = 2 | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Burst Type = Interleaved | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Burst Length = 8 | FF |
| 35 | 04000 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | MRS - MODE REGISTER SET (S0~) | FF |
| | 04000 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Reserved | FF |
| 36 | 00400 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | MRS - MODE REGISTER SET (S0~) | FF |
| | 00400 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Normal MRS | FF |
| | 00400 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Operating Mode = Reserved | FF |
| | 00400 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Latency = Reserved | FF |
| | 00400 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Burst Type = Sequential | FF |
| | 00400 | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Burst Length = Reserved | FF |
| 37 | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | MRS - MODE REGISTER SET (S0~) | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Normal MRS | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Normal Operation | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Latency = 2 | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Burst Type = Interleaved | FF |
| | 0002B | FFFFFFFF | FFFFFFFF | FFFFFFFF | FFFFFFFF | Burst Length = 8 | FF |

Figure 21- MRS Cycle Acquisition Disassembly

APPENDIX A - How DDRII Data is Clocked

A.1 Background

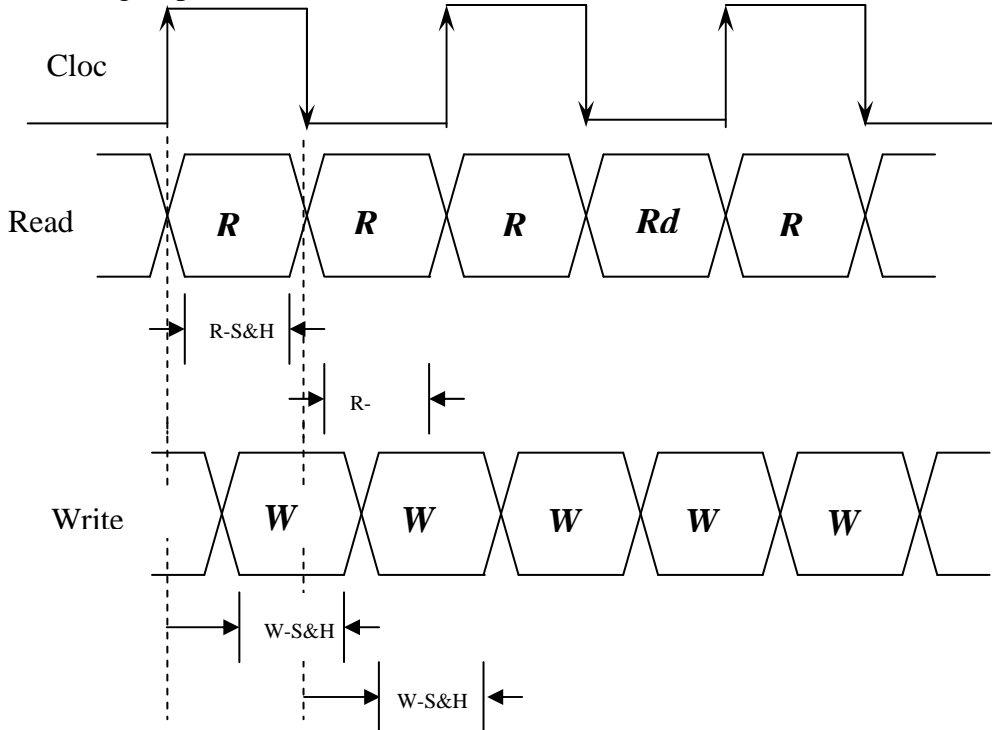
Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section *and* the D3 section. Through the User Interface of the TLA, demux can be performed by connecting the A0-A3 sections and storing the data in both the A0-A3 and D0-D3 data sections. More extensive demux capabilities are possible using the software tools that were used to create the various DDR packages. A very useful side benefit of using demux is that, since only one set of TLA data channels have to be connected, only one probe load is added to the target, even though data is stored in two different locations of the acquisition card.

A.2 DDR Acquisition - General

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. The speeds of DDRII (400MHz and higher) require different setups to enable proper data acquisition. In addition, instead of trying to use the Data Strobes to acquire data our solution uses one of the DDRII SDRAM Clocks (DDRCK0, DDRCK1, or DDRCK2 user selectable) and all data acquisition is adjusted in relation to the clock edges. The 8 or 16 Data Strobes cannot be easily used to acquire data as some TLA configurations only support that number of Clock Inputs. Also, the Strobes cannot be used to acquire Address and Command information.

A.3 DDRII400 Support

This support requires two (2) merged 136-channel 450MHz TLA7AA4 or TLA7AB4 acquisition cards used in a TLA7XX. The merged cards enable both Read and Write data to be acquired simultaneously from a DDR system. Data is acquired using both edges of the DDR clock, and demultiplexing is done to permit acquiring both Read and Write data on every clock edge. One Sample Point must be adjusted to acquire valid Read data in reference to the clock edge; a second Sample Point must be set to acquire valid Write data in relation to the edge. Again, different Sample Points must be set for each of the Read / Write data groups (RDDatHi, RDDatLo, WRDatHi, and WRDatLo), and if necessary, sample points can be set for any of the 8-bit data groups.



| Sample | Address | RDDatHi | RDDatLo | WRDatHi | WRDatLo | Command | Strobes | Timestamp |
|--------|---------|----------|----------|----------|----------|----------------------------------|---------|------------|
| 19 | 10011 | 20528000 | 008E0000 | 20528000 | 00070000 | DESL--IGNORE_COMMAND--DATA? | 20 | -25.000 ns |
| 20 | 142F3 | 20528004 | 0DC60000 | 20528000 | 0DC60000 | ACTV--ROW_ADDRESS_STROBE_(S0~) | 2C | -19.500 ns |
| 21 | 142F3 | 20528004 | 0C460000 | 20528004 | 0DC60000 | ACTV--ROW_ADDRESS_STROBE_(S0~) | 2C | -15.000 ns |
| 22 | 10011 | 20528000 | 00040000 | 20528000 | 00040000 | DESL--IGNORE_COMMAND--DATA? | 20 | -9.500 ns |
| 23 | 10011 | 20528000 | 010C0000 | 20528000 | 00040000 | DESL--IGNORE_COMMAND--DATA? | 20 | -5.000 ns |
| 24 | 14031 | 2052800C | 050C0000 | 20528000 | 050C0000 | READ--COL_ADDR_READ_(S0~) | 20 | 0 ps |
| 25 | 14031 | 20528008 | 040C0000 | 2052800C | 050C0000 | READ--COL_ADDR_READ_(S0~) | 28 | 5.000 ns |
| 26 | 10011 | 20528000 | 040C0000 | 20528000 | 040C0000 | DESL--IGNORE_COMMAND--DATA? | 20 | 10.500 ns |
| 27 | 10011 | 20528000 | 040C0000 | 20528000 | 040C0000 | DESL--IGNORE_COMMAND--DATA? | 20 | 15.000 ns |
| 28 | 10011 | 20528000 | 040C0000 | 20528000 | 040C0000 | DESL--IGNORE_COMMAND--DATA? | 20 | 20.500 ns |
| 29 | 10011 | 20D38C30 | C30C20A2 | 20528000 | 040C0000 | DESL--IGNORE_COMMAND--DATA? | 20 | 25.000 ns |
| 30 | 10011 | 2C528082 | 08248208 | 20D38C30 | C30C20A2 | DESL--IGNORE_COMMAND--DATA? | B4 | 30.500 ns |
| 31 | 10011 | 7D77F7DF | FFDF3C7 | 2C528082 | 08248208 | DESL--IGNORE_COMMAND--DATA? | 60 | 35.500 ns |
| 32 | 10011 | BA739659 | 65155555 | 7D77F7DF | FFDF3C7 | DESL--IGNORE_COMMAND--DATA? | FF | 40.000 ns |
| 33 | 10011 | 2EFAEBBE | FBAE39E7 | BA739659 | 65155555 | DESL--IGNORE_COMMAND--DATA? | 20 | 45.000 ns |
| 34 | 10011 | E3DEB4D3 | 4D3492C8 | 2EFAEBBE | FBAE39E7 | DESL--IGNORE_COMMAND--DATA? | FF | 50.500 ns |
| 35 | 10011 | F8FBBCF7 | DF6D9618 | E3DEB4D3 | 4D3492C8 | DESL--IGNORE_COMMAND--DATA? | 20 | 55.500 ns |
| 36 | 10011 | A6DBEDB4 | D75D65B6 | F8FBBCF7 | DF6D9618 | DESL--IGNORE_COMMAND--DATA? | 3C | 60.500 ns |
| 37 | 10011 | A252A1B4 | 00044482 | A6DBEDB4 | D75D65B6 | DESL--IGNORE_COMMAND--DATA? | 20 | 65.000 ns |
| 38 | 10011 | AEDBADB6 | 0E0761B6 | A6DBEDB4 | D75D65B6 | DESL--IGNORE_COMMAND--DATA? | 20 | 70.500 ns |
| 39 | 10011 | A8D2AC30 | 08040010 | AEDBADB6 | 0E0761B6 | DESL--IGNORE_COMMAND--DATA? | 21 | 75.000 ns |
| 40 | 10011 | 2652A024 | 00054010 | ADD2A030 | 00040010 | PRE--PRECHARGE_SELECT_BANK_(S0~) | 20 | 80.000 ns |
| 41 | 14411 | 24528004 | 08044010 | 2652A024 | 08054010 | PRE--PRECHARGE_SELECT_BANK_(S0~) | 20 | 85.000 ns |
| 42 | 10011 | 20528000 | 00040000 | 20528000 | 00040000 | DESL--IGNORE_COMMAND--DATA? | 20 | 90.500 ns |
| 43 | 10011 | 20528000 | 00040000 | 20528000 | 00040000 | DESL--IGNORE_COMMAND--DATA? | 20 | 95.000 ns |
| 44 | 10011 | 20528000 | 00040000 | 20528000 | 00040000 | DESL--IGNORE_COMMAND--DATA? | 22 | 100.500 ns |

APPENDIX B - Considerations

B.1 DDRII Bus Loading

It must be noted that the NEX-DDRII Bus Adapter does not provide any buffering of the DDRII memory signals. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using this adapter, to see the exact timing relationships and signal waveforms from the system. It is important to note that the NEX-DDRII is an impedance controlled, matched trace length design. This adds greatly to its ability to maintain signal integrity and timing relationships of the DDRII bus.

APPENDIX C - DDRII DIMM 240-pin Pinout

APPENDIX D - NEX-DDR_{II} P6860/P6880 Compression Pinouts

For further information on the P6860/P6880 Connectorless probe compression footprint please refer to the “P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

| Pad # | TLA Channel | DDR _{II} Pin # | DDR _{II} Signal |
|-------|-------------|-------------------------|--------------------------|
| A15 | Q3- | 45 | DQS8- |
| A13 | Q3+ | 46 | DQS8+ |
| B12 | E3:7 | --- | --- |
| B10 | E3:6 | 174 | A14 |
| A12 | E3:5 | 55 | RC0 |
| A10 | E3:4 | 58 | A7 |
| B9 | E3:3 | 177 | A9 |
| B7 | E3:2 | 179 | A8 |
| A9 | E3:1 | 167 | NC_CB6 |
| A7 | E3:0 | 152 | DQ28 |
| B6 | E2:7 | 60 | A5 |
| B4 | E2:6 | 63 | A2 |
| A6 | E2:5 | 31 | DQ19 |
| A4 | E2:4 | 144 | DQ21 |
| B3 | E2:3 | --- | --- |
| B1 | E2:2 | --- | --- |
| A3 | E2:1 | 120 | SCL |
| A1 | E2:0 | 119 | SDA |

P6860 Probe Connection SL - E2 / E3

| Pad # | TLA Channel | DDR _{II} Pin # | DDR _{II} Signal |
|-------|-------------|-------------------------|--------------------------|
| A15 | CK1- | 221 | CK2~ |
| A13 | CK1+ | 220 | CK2 |
| B12 | A1:7 | 217 | DQ52 |
| B10 | A1:6 | 218 | DQ53 |
| A12 | A1:5 | 99 | DQ49 |
| A10 | A1:4 | 98 | DQ48 |
| B9 | A1:3 | 226 | DQ54 |
| B7 | A1:2 | 107 | DQ50 |
| A9 | A1:1 | 227 | DQ55 |
| A7 | A1:0 | 229 | DQ60 |
| B6 | A0:7 | 108 | DQ51 |
| B4 | A0:6 | 110 | DQ56 |
| A6 | A0:5 | 230 | DQ61 |
| A4 | A0:4 | 111 | DQ57 |
| B3 | A0:3 | 116 | DQ58 |
| B1 | A0:2 | 236 | DQ63 |
| A3 | A0:1 | 235 | DQ62 |
| A1 | A0:0 | 117 | DQ59 |

P6860 Probe Connection MA - A0 / A1

| Pad # | TLA Channel | DDR _{II} Pin # | DDR _{II} Signal |
|-------|-------------|-------------------------|--------------------------|
| A15 | CK3- | 165 | DQS17- |
| A13 | CK3+ | 164 | DQS17+ |
| B12 | C3:7 | 18 | RC1 |
| B10 | C3:6 | 19 | NC19 |
| A12 | C3:5 | 52 | CKE0 |
| A10 | C3:4 | 54 | A16_BA2 |
| B9 | C3:3 | 176 | A12 |
| B7 | C3:2 | 57 | A11 |
| A9 | C3:1 | 161 | NC_CB4 |
| A7 | C3:0 | 43 | NC_CB1 |
| B6 | C2:7 | 42 | NC_CB0 |
| B4 | C2:6 | 162 | NC_CB5 |
| A6 | C2:5 | 168 | NC_CB7 |
| A4 | C2:4 | 34 | DQ25 |
| B3 | C2:3 | 48 | NC_CB2 |
| B1 | C2:2 | 33 | DQ24 |
| A3 | C2:1 | 30 | DQ18 |
| A1 | C2:0 | 25 | DQ17 |

P6860 Probe Connection SL - C2 / C3

| Pad # | TLA Channel | DDR _{II} Pin # | DDR _{II} Signal |
|-------|-------------|-------------------------|--------------------------|
| A15 | CK0- | 138 | CK1~ |
| A13 | CK0+ | 137 | CK1 |
| B12 | A3:7 | 141 | DQ15 |
| B10 | A3:6 | 22 | DQ11 |
| A12 | A3:5 | 140 | DQ14 |
| A10 | A3:4 | 21 | DQ10 |
| B9 | A3:3 | 13 | DQ9 |
| B7 | A3:2 | 132 | DQ13 |
| A9 | A3:1 | 131 | DQ12 |
| A7 | A3:0 | 10 | DQ3 |
| B6 | A2:7 | 12 | DQ8 |
| B4 | A2:6 | 129 | DQ7 |
| A6 | A2:5 | 9 | DQ2 |
| A4 | A2:4 | 4 | DQ1 |
| B3 | A2:3 | 128 | DQ6 |
| B1 | A2:2 | 3 | DQ0 |
| A3 | A2:1 | 123 | DQ5 |
| A1 | A2:0 | 122 | DQ4 |

P6860 Probe Connection MA - A2 / A3

APPENDIX D - NEX-DDRII P6860/P6880 Compression Pinouts (cont'd.)

| Pad # | TLA Channel | DDRII Pin # | DDRII Signal |
|-------|-------------|-------------|--------------|
| A15 | CK0- | --- | --- |
| A13 | CK0+ | --- | --- |
| B12 | A3:7 | 171 | CKE1 |
| B10 | A3:6 | 173 | A15 |
| A12 | A3:5 | 158 | DQ30 |
| A10 | A3:4 | 39 | DQ26 |
| B9 | A3:3 | 159 | DQ31 |
| B7 | A3:2 | 40 | DQ27 |
| A9 | A3:1 | 180 | A6 |
| A7 | A3:0 | 182 | A3 |
| B6 | A2:7 | 61 | A4 |
| B4 | A2:6 | 183 | A1 |
| A6 | A2:5 | 49 | NC_CB3 |
| A4 | A2:4 | 153 | DQ29 |
| B3 | A2:3 | 150 | DQ23 |
| B1 | A2:2 | 24 | DQ16 |
| A3 | A2:1 | 149 | DQ22 |
| A1 | A2:0 | 143 | DQ20 |

P6860 Probe Connection SL - A2 / A3

| Pad # | TLA Channel | DDRII Pin # | DDRII Signal |
|-------|-------------|-------------|--------------|
| A15 | Q3- | --- | GND |
| A13 | Q3+ | 192 | RAS~ |
| B12 | E3:7 | 70 | A10_AP |
| B10 | E3:6 | 71 | BA0 |
| A12 | E3:5 | 68 | NC68 |
| A10 | E3:4 | 190 | BA1 |
| B9 | E3:3 | 196 | A13 |
| B7 | E3:2 | 77 | ODT1 |
| A9 | E3:1 | 195 | ODT0 |
| A7 | E3:0 | 101 | SA2 |
| B6 | E2:7 | 102 | NC_TEST |
| B4 | E2:6 | 239 | SA0 |
| A6 | E2:5 | 205 | DQ38 |
| A4 | E2:4 | 86 | DQ34 |
| B3 | E2:3 | 199 | DQ36 |
| B1 | E2:2 | 200 | DQ37 |
| A3 | E2:1 | 80 | DQ32 |
| A1 | E2:0 | 81 | DQ33 |

P6860 Probe Connection MA – E2 / E3

| Pad # | TLA Channel | DDRII Pin # | DDRII Signal |
|-------|-------------|-------------|--------------|
| A15 | CK3- | 186 | CK0~ |
| A13 | CK3+ | 185 | CK0 |
| B12 | C3:7 | --- | --- |
| B10 | C3:6 | 188 | A0 |
| A12 | C3:5 | 96 | DQ43 |
| A10 | C3:4 | 215 | DQ47 |
| B9 | C3:3 | 95 | DQ42 |
| B7 | C3:2 | 214 | DQ46 |
| A9 | C3:1 | 209 | DQ45 |
| A7 | C3:0 | 90 | DQ41 |
| B6 | C2:7 | 208 | DQ44 |
| B4 | C2:6 | 89 | DQ40 |
| A6 | C2:5 | 87 | DQ35 |
| A4 | C2:4 | 206 | DQ39 |
| B3 | C2:3 | 76 | S1~ |
| B1 | C2:2 | 74 | CAS~ |
| A3 | C2:1 | 73 | WE~ |
| A1 | C2:0 | 193 | S0~ |

P6860 Probe Connection MA – C2 / C3

APPENDIX D - NEX-DDRII P6860/P6880 Compression Pinouts (cont'd.)

| Pad # | TLA Channel | DDRII Pin # | DDRII Signal |
|-------|-------------|-------------|--------------|
| A15 | --- | --- | --- |
| A13 | --- | --- | --- |
| B12 | A0:7+ | 37 | DQS3+ |
| B10 | A0:7- | 36 | DQS3- |
| A12 | A0:6- | 156 | DQS12- |
| A10 | A0:6+ | 155 | DQS12+ |
| B9 | A0:5+ | 146 | DQS11+ |
| B7 | A0:5- | 147 | DQS11- |
| A9 | A0:4- | 27 | DQS2- |
| A7 | A0:4+ | 28 | DQS2+ |
| B6 | A0:3+ | 134 | DQS10+ |
| B4 | A0:3- | 135 | DQS10- |
| A6 | A0:2- | 15 | DQS1- |
| A4 | A0:2+ | 16 | DQS1+ |
| B3 | A0:1+ | 125 | DQS9+ |
| B1 | A0:1- | 126 | DQS9- |
| A3 | A0:0- | 6 | DQS0- |
| A1 | A0:0+ | 7 | DQS0+ |

For use with 400DDR2S support
P6880 Probe Connection SL – A0

| Pad # | TLA Channel | DDRII Pin # | DDRII Signal |
|-------|-------------|-------------|--------------|
| A15 | CK1- | 212 | DQS14- |
| A13 | CK1+ | 211 | DQS14+ |
| B12 | A1:7+ | 84 | DQS4+ |
| B10 | A1:7- | 83 | DQS4- |
| A12 | A1:6- | 92 | DQS5- |
| A10 | A1:6+ | 93 | DQS5+ |
| B9 | A1:5+ | 202 | DQS13+ |
| B7 | A1:5- | 203 | DQS13- |
| A9 | A1:4- | 224 | DQS15- |
| A7 | A1:4+ | 223 | DQS15+ |
| B6 | A1:3+ | 240 | SA1 |
| B4 | A1:3- | --- | GND |
| A6 | A1:2- | 104 | DQS6- |
| A4 | A1:2+ | 105 | DQS6+ |
| B3 | A1:1+ | 114 | DQS7+ |
| B1 | A1:1- | 113 | DQS7- |
| A3 | A1:0- | 233 | DQS16- |
| A1 | A1:0+ | 232 | DQS16+ |

For use with 400DDR2S support
P6880 Probe Connection SL - A1

| Pad # | TLA Channel | DDRII Pin # | DDRII Signal |
|-------|-------------|-------------|--------------|
| A15 | CK1- | --- | --- |
| A13 | CK1+ | --- | --- |
| B12 | A1:7 | 37 | DQS3+ |
| B10 | A1:6 | --- | --- |
| A12 | A1:5 | --- | --- |
| A10 | A1:4 | 155 | DM3 |
| B9 | A1:3 | 146 | DM2 |
| B7 | A1:2 | --- | --- |
| A9 | A1:1 | --- | --- |
| A7 | A1:0 | 28 | DQS2+ |
| B6 | A0:7 | 134 | DM1 |
| B4 | A0:6 | --- | --- |
| A6 | A0:5 | --- | --- |
| A4 | A0:4 | 16 | DQS1+ |
| B3 | A0:3 | 125 | DM0 |
| B1 | A0:2 | --- | --- |
| A3 | A0:1 | --- | --- |
| A1 | A0:0 | 7 | DQS0+ |

For use with 400DDR2M support
P6860 Probe Connection SL – A1 / A0

| Pad # | TLA Channel | DDRII Pin # | DDRII Signal |
|-------|-------------|-------------|--------------|
| A15 | CK2- | --- | --- |
| A13 | CK2+ | 211 | DM5 |
| B12 | D1:7 | 84 | DQS4+ |
| B10 | D1:6 | --- | --- |
| A12 | D1:5 | --- | --- |
| A10 | D1:4 | 93 | DQS5+ |
| B9 | D1:3 | 202 | DM4 |
| B7 | D1:2 | --- | --- |
| A9 | D1:1 | --- | --- |
| A7 | D1:0 | 223 | DM6 |
| B6 | D0:7 | 240 | SA1 |
| B4 | D0:6 | --- | GND |
| A6 | D0:5 | --- | --- |
| A4 | D0:4 | 105 | DQS6+ |
| B3 | D0:3 | 114 | DQS7+ |
| B1 | D0:2 | --- | --- |
| A3 | D0:1 | --- | --- |
| A1 | D0:0 | 232 | DM7 |

For use with 400DDR2M support
P6860 Probe Connection SL – D1 / D0

APPENDIX E – NEX-DDRII Silkscreen

APPENDIX F – Data Group / Data Byte / Strobe Cross-Reference

| 32-bit Data Group | 4-bit Data Group | Strobe | Data Bits |
|--------------------------|-------------------------|---------------|------------------|
| RDDatHi | RDDatNib16 | DQS16 | 63,62,61,60 |
| | RDDatNib7 | DQS7 | 59,58,57,56 |
| | RDDatNib15 | DQS15 | 55,54,53,52 |
| | RDDatNib6 | DQS6 | 51,50,49,48 |
| | RDDatNib14 | DQS14 | 47,46,45,44 |
| | RDDatNib5 | DQS5 | 43,42,41,40 |
| | RDDatNib13 | DQS13 | 39,38,37,36 |
| | RDDatNib4 | DQS4 | 35,34,33,32 |
| RDDatLo | RDDatNib12 | DQS12 | 31,30,29,28 |
| | RDDatNib3 | DQS3 | 27,26,25,24 |
| | RDDatNib11 | DQS11 | 23,22,21,20 |
| | RDDatNib2 | DQS2 | 19,18,17,16 |
| | RDDatNib10 | DQS10 | 15,14,13,12 |
| | RDDatNib1 | DQS1 | 11,10,9,8 |
| | RDDatNib9 | DQS9 | 7,6,5,4 |
| | RDDatNib0 | DQS0 | 3,2,1,0 |
| WRDatHi | WRDatNib16 | DQS16 | 63,62,61,60 |
| | WRDatNib7 | DQS7 | 59,58,57,56 |
| | WRDatNib15 | DQS15 | 55,54,53,52 |
| | WRDatNib6 | DQS6 | 51,50,49,48 |
| | WRDatNib14 | DQS14 | 47,46,45,44 |
| | WRDatNib5 | DQS5 | 43,42,41,40 |
| | WRDatNib13 | DQS13 | 39,38,37,36 |
| | WRDatNib4 | DQS4 | 35,34,33,32 |
| WRDatLo | WRDatNib12 | DQS12 | 31,30,29,28 |
| | WRDatNib3 | DQS3 | 27,26,25,24 |
| | WRDatNib11 | DQS11 | 23,22,21,20 |
| | WRDatNib2 | DQS2 | 19,18,17,16 |
| | WRDatNib10 | DQS10 | 15,14,13,12 |
| | WRDatNib1 | DQS1 | 11,10,9,8 |
| | WRDatNib9 | DQS9 | 7,6,5,4 |
| | WRDatNib0 | DQS0 | 3,2,1,0 |

400DDR2S Groups/Bytes/Strobes Cross Reference

APPENDIX F – Data Group / Data Byte / Strobe Cross-Reference (cont'd)

| 32-bit Data Group | 8-bit Data Group | Strobe | Data Bits |
|--------------------------|-------------------------|---------------|-------------------------|
| RdDatHi | RDDatBy7 | DQS7 | 63,62,61,60,59,58,57,56 |
| | RDDatBy6 | DQS6 | 55,54,53,52,51,50,49,48 |
| | RDDatBy5 | DQS5 | 47,46,45,44,43,42,41,40 |
| | RDDatBy4 | DQS4 | 39,38,37,36,35,34,33,32 |
| RdDatLo | RDDatBy3 | DQS3 | 31,30,29,28,27,26,25,24 |
| | RDDatBy2 | DQS2 | 23,22,21,20,19,18,17,16 |
| | RDDatBy1 | DQS1 | 15,14,13,12,11,10,9,8 |
| | RDDatBy0 | DQS0 | 7,6,5,4,3,2,1,0 |
| WrDatHi | WRDatBy7 | DQS7 | 63,62,61,60,59,58,57,56 |
| | WRDatBy6 | DQS6 | 55,54,53,52,51,50,49,48 |
| | WRDatBy5 | DQS5 | 47,46,45,44,43,42,41,40 |
| | WRDatBy4 | DQS4 | 39,38,37,36,35,34,33,32 |
| WrDatLo | WRDatBy3 | DQS3 | 31,30,29,28,27,26,25,24 |
| | WRDatBy2 | DQS2 | 23,22,21,20,19,18,17,16 |
| | WRDatBy1 | DQS1 | 15,14,13,12,11,10,9,8 |
| | WRDatBy0 | DQS0 | 7,6,5,4,3,2,1,0 |

400DDR2M Groups/Bytes/Strobes Cross Reference

APPENDIX G - References

Tektronix TLA700 System User's Manual

Tektronix TLA700 Logic Analyzer User's Manual

P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual
Tektronix part number 071-1059-00

Elpida 1GB Unbuffered DDR2 SDRAM DIMM
Document #E0365E10, March 2003

Elpida 1GB Registered DDR2 SDRAM DIMM
Document #E0366E20, April 2003

APPENDIX H - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

Support Contact Information

| | |
|---------------------|---|
| Technical Support | techsupport@nexustechnology.com |
| General Information | support@nexustechnology.com |
| Quote Requests | quotes@nexustechnology.com |

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.