



# NEX-IXP1200

## IXP1200 Disassembly Software Users Manual

Including these Software Support packages:  
IXP1200                      IXP1200E

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## **1.0 OVERVIEW**

### **1.1 General Information**

The NEX-IXP1200 disassembly software provides disassembly of acquired IXP1200 bus cycles using a TLA600/TLA700 with a 102- or 136-channel acquisition module. A 100MHz TLA acquisition card is sufficient unless the core clock frequency is expected to approach or exceed 200MHz. The NEX-IXP1200 support is software only. Please see Section 3.0 “Connecting to a IXP1200 Target” for information on probing.

The NEX-IXP1200 provides full instruction decoding of ARM, through Architecture v4. Thumb instructions are not supported at this time.

This manual assumes that the user is familiar with the IXP1200 processor specification and the Tektronix TLA600/TLA700 Logic Analyzers. It is also expected that the user is familiar with Windows 98. The TLA700 Application must also be at V1.1 or later for the NEX-IXP1200 support to work properly.

## **2.0 SOFTWARE INSTALLATION**

One 3½” diskette has been included with the NEX-IXP1200 disassembly product. The NEX-IXP1200 software is loaded in the same method as other Windows programs. Place the NEX-IXP1200 Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the Selected support in its proper place on the hard disk.

To load IXP1200 support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose IXP1200 and click on **Okay**.

## **3.0 CONNECTING TO AN IXP1200 TARGET**

### **3.1 General Information**

It is recommended that the user add Mictor connectors to their target for the interface to the TLA700 using Tektronix P6434 high-density probes. Compression pads should be added to the target if Tektronix P6860 probes will be used. We are unaware of a clip to permit acquiring the signals directly from the micro. Table 1 shows the wiring and Channel Grouping required for NEX-IXP1200 support.

**IMPORTANT:** Specific wiring must be followed when routing the IXP1200 signals to Mictor connectors if the NEX-IXP1200 support is going to be used. Appendix A “NEX-IXP1200 Mictor Pinout” and Appendix B “NEX-IXP1200 P6860 Compression Pinouts” provides this information.

Group Name	Signal Name	IXP1200 Pin #	TLA700 input	Group Name	Signal Name	IXP1200 Pin #	TLA700 input
HiData (Hex)	MDATA63		A3:7	LoData (Hex)	MDATA31		D3:7
	MDATA62		A3:6		MDATA30		D3:6
	MDATA61		A3:5		MDATA29		D3:5
	MDATA60		A3:4		MDATA28		D3:4
	MDATA59		A3:3		MDATA27		D3:3
	MDATA58		A3:2		MDATA26		D3:2
	MDATA57		A3:1		MDATA25		D3:1
	MDATA56		A3:0		MDATA24		D3:0
	MDATA55		A2:7		MDATA23		D2:7
	MDATA54		A2:6		MDATA22		D2:6
	MDATA53		A2:5		MDATA21		D2:5
	MDATA52		A2:4		MDATA20		D2:4
	MDATA51		A2:3		MDATA19		D2:3
	MDATA50		A2:2		MDATA18		D2:2
	MDATA49		A2:1		MDATA17		D2:1
	MDATA48		A2:0		MDATA16		D2:0
	MDATA47		A1:7		MDATA15		D1:7
	MDATA46		A1:6		MDATA14		D1:6
	MDATA45		A1:5		MDATA13		D1:5
	MDATA44		A1:4		MDATA12		D1:4
	MDATA43		A1:3		MDATA11		D1:3
	MDATA42		A1:2		MDATA10		D1:2
	MDATA41		A1:1		MDATA9		D1:1
	MDATA40		A1:0		MDATA8		D1:0
	MDATA39		A0:7		MDATA7		D0:7
	MDATA38		A0:6		MDATA6		D0:6
	MDATA37		A0:5		MDATA5		D0:5
	MDATA36		A0:4		MDATA4		D0:4
	MDATA35		A0:3		MDATA3		D0:3
	MDATA34		A0:2		MDATA2		D0:2
	MDATA33		A0:1		MDATA1		D0:1
	MDATA32		A0:0		MDATA0		D0:0
Address (Hex) Synthesized	---	---	---	DRAMAddr	MADR[13]		C1:7
	---	---	---		MADR[12]		C1:6
	---	---	---		MADR[11]		C3:7
Control (Sym)	RAS#		C2:0		MADR[10]		C3:6
	CAS#		C2:1		MADR[9]		C3:5
	DQM		C2:3		MADR[8]		C3:4
	WE#		C2:2		MADR[7]		C3:3
Misc (Bin)	SDCLK		Clock:3		MADR[6]		C3:2
	PARITY		C0:0		MADR[5]		C3:1
					MADR[4]		C3:0
					MADR[3]		C2:7
					MADR[2]		C2:6
					MADR[1]		C2:5
				MADR[0]		C2:4	
			DRAM_A1	ground	C0:3		
			DRAM_A0	ground	C0:2		

Table 1- IXP1200 TLA600/700 Wiring

## **4.0 CLOCK SELECTION**

### **4.1 General Information**

There are four clocking options available when using the NEX-IXP1200 support package. Each is explained in detail below.

The selections are made by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

### **4.2 Clocking Options - Explanation**

**Clocking Mode - Bus Cycles Only** is the default mode, and will setup the logic analyzer to acquire all but DESL and NOP cycles. An optional selection is Rising Edge of SDCK, which will setup the analyzer to acquire and store data on every SDCK rising edge.

**Read Cycle Latency** - This sets the number of clock cycles to wait before valid Read data is available. The default setting a latency of 2 clock cycles, but this can be set to 3.

**Burst Read Length** - By default this is set to a burst length of 1. Can be set to 2, 4, 8, or Full Page.

**Burst Write Length** - By default this is set to a burst length of 1. Can be set to 2, 4, 8, or Full Page.

## **5.0 VIEWING DATA**

### **5.1 Viewing Timing Data on the TLA700**

By default, the TLA700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: IXP1200 and IXP1200-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, IXP1200-MagniVu, will show all of the channels in 2GHz MagniVu mode when using a TLA7X3/4 module and 8GHz MagniVu mode when using a TLA7AX3/4 module, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA700 System User's Manual for additional information on formatting the Waveform display.

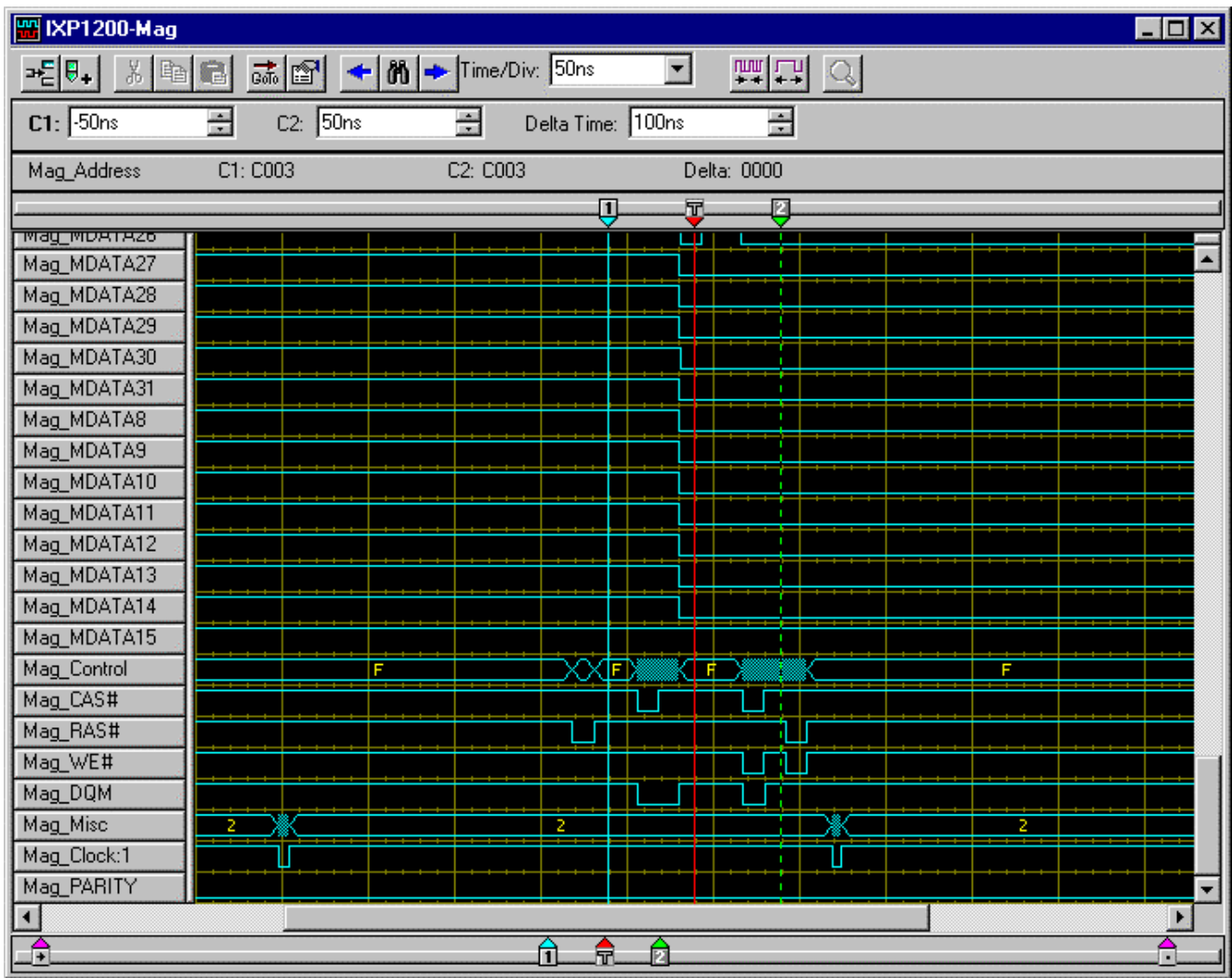


Figure 1- IXP1200 MagniVu Display on TLA700

## 6.0 USING THE DISASSEMBLY SOFTWARE

**NOTE:** For the IXP1200 support to acquire all cycles in proper order, instruction prefetch caching **MUST BE DISABLED**. Please refer to the IXP1200 Manual for information on disabling the instruction and data caches.

### 6.1 General

The NEX-IXP1200 support software acquires and decodes IXP1200 bus activity and displays the information as assembly language mnemonics (machine code) - see Figure 3. This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types of interest to the software engineer (Figure 4). The user can choose to display the acquired data in Hardware, Software, Control Flow, or Subroutine modes.

A major feature of the NEX-IXP1200 software is its ability to intelligently acquire bus cycle information. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the IXP1200 software is able to acquire only the valid IXP1200 bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more microprocessor bus cycles. For debug purposes, the user also has the ability to override this function and acquire data on every SDCLK edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps when using a TLA7X3/4 module and 125ps when using a TLA7AX3/4 module, permits precise measurements of microprocessor bus activity. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

## 6.2 IXP1200 Modes

To support variations in target configurations, several modes have been designed into the IXP1200 support. These are "Number of Row Bits", "Number of Column Bits", "High/Low Instruction" and "Suppress SDRAM cycles". Figure 1 shows the Properties-Disassembly window, with these modes. Each mode is explained below.

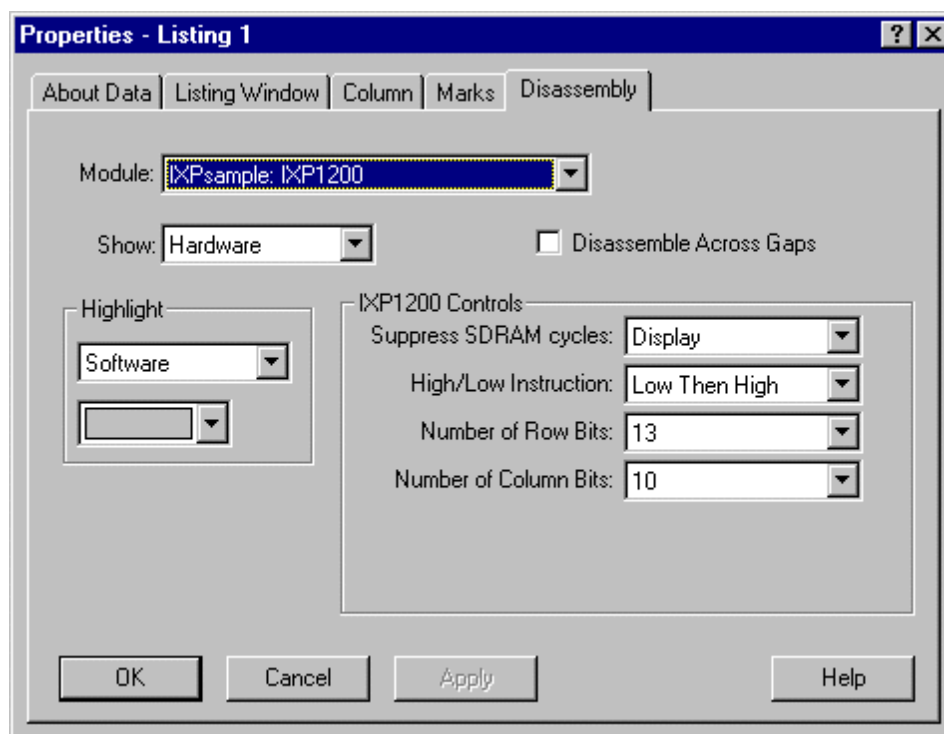


Figure 2- Disassembly Modes in the Properties-Disassembly Window

### 6.3 "Number of Row Bits" and "Number of Column Bits"

The IXP1200 microprocessor supports the use of DRAM for code execution memory. However, because DRAM is accessed by Row and Column address cycles it becomes necessary to translate those two cycles into a physical address equivalent which is necessary for tracking the flow of program code. The Address group is used by the IXP1200 support to reconstruct the physical address from Row and Column information contained in the DRAMAddr group. The DRAMAddr group in the IXP1200 support is configured by default for 13 Row and 10 Column address bits. The number of bits used in this group may need to be adjusted to reflect a given target. The disassembler supports 13, 12 or 11 RAS bits and 10, 9 or 8 CAS bits. These settings determine how the Physical address is reconstructed into the Address display group. A DOS executable named Readdress.exe is present on the installation diskette (although it is not automatically installed). This executable will encode and decode between RAS/CAS bits and a Physical address and is included for convenience.

### 6.4 "High/Low Instruction"

Because the IXP1200 microprocessor acquires two instructions in each fetch, the IXP1200 support contains a mode for controlling how these values are displayed. If the choice "Both" is selected, then high and low instructions are displayed. If the choice "Low then High" is selected, then the Low instruction is displayed during the first fetch at a given 64 bit location. The High instruction is displayed during the next fetch to the same location. AS MENTIONED ABOVE, CACHE MUST BE DISABLED.

### 6.5 "Suppress SDRAM cycles"

Because the IXP1200 microprocessor support acquires all cycle types, RAS, CAS and PRECHARGE cycles will be interspersed with instruction reads, data reads and data writes. When "Suppress SDRAM cycles" mode is set to "Display", all cycles are visible. Setting "Suppress SDRAM cycles" to "Suppress" will display only instruction, data read and data write cycles.

### 6.6 Disassembly Using the TLA700

The TLA700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size

- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

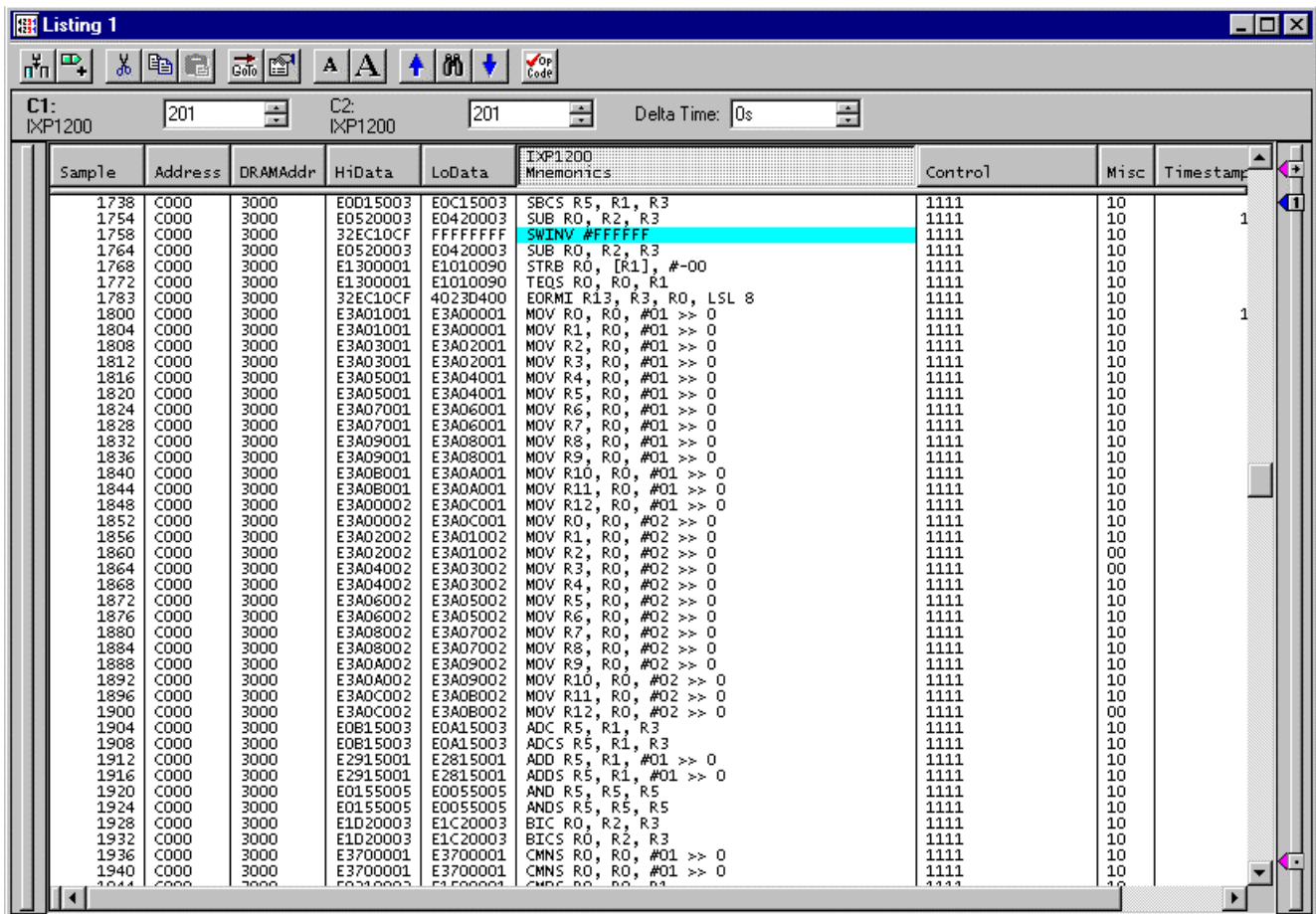


Figure 3- IXP1200 Disassembly

The other column of interest is the Mnemonics column, where the IXP1200 disassembly information is displayed. As mentioned previously, it is possible to filter the IXP1200 instructions that are displayed. This is done via selections made in the Disassembly tab of the Properties window (see Figure 4). By default the display is in Hardware mode, where all bus cycles are displayed (Memory Reads, Memory Writes, Instructions, etc.). Other choices are: Software (only executed instructions are displayed), Control Flow (display of instructions affecting code flow such as Jumps, Branches, etc.), and Subroutine (only instructions such as Calls, Returns, etc. are displayed).

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

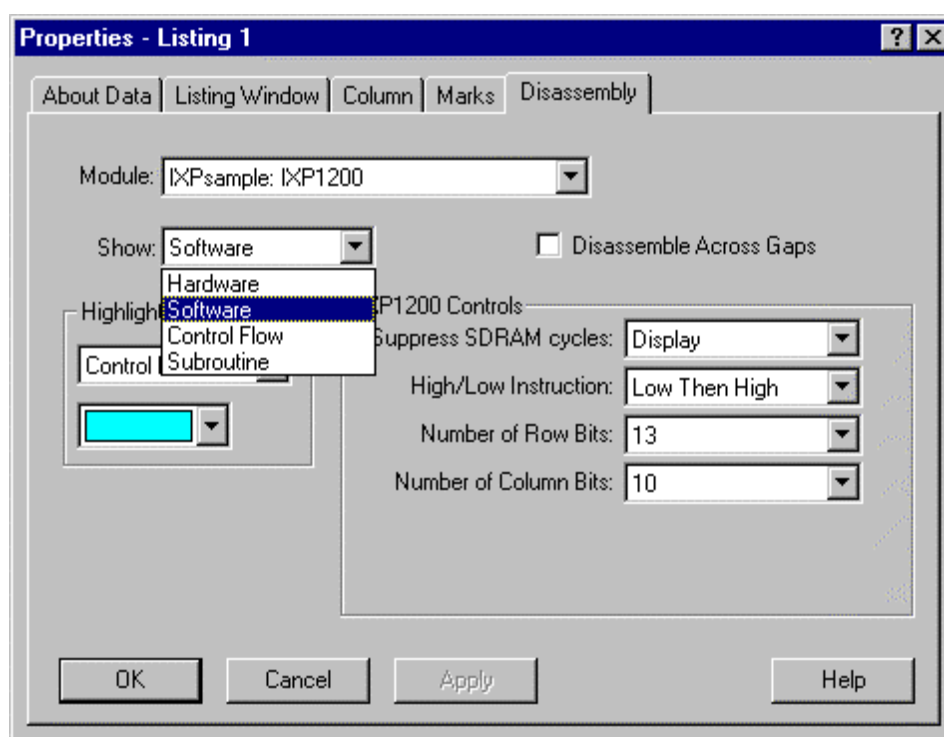
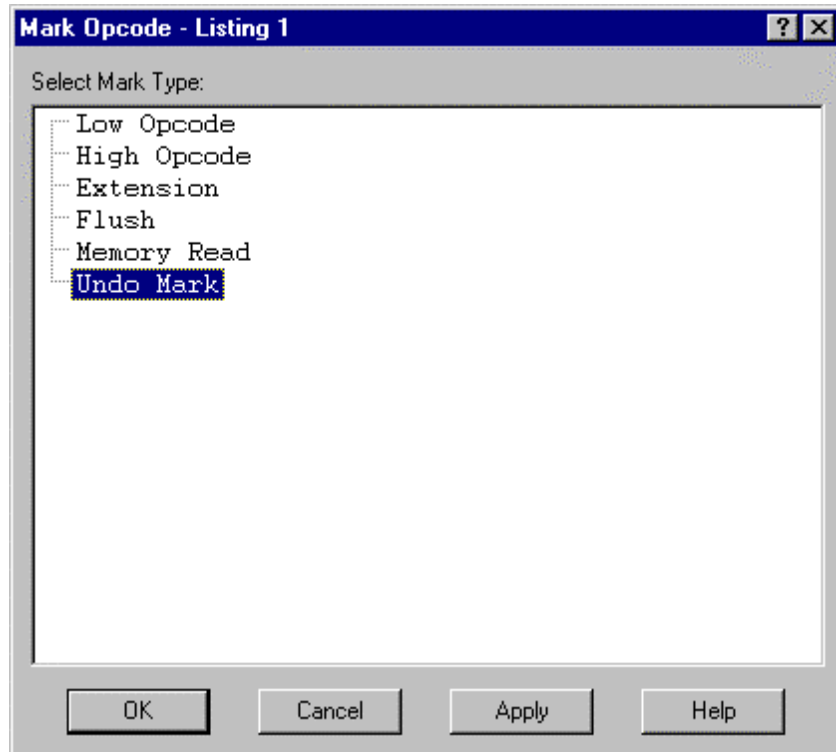


Figure 4- Disassembly Display Filter Window

## 6.7 Help! The Disassembler's Confused (or: Using Mark Opcode)

Because the IXP1200 does not have a signal to denote an opcode fetch, it is difficult to distinguish between a Read cycle and an Opcode Fetch. The disassembly software does the best it can to figure this out, but it assumes that every Read from contiguous memory cycles is a Fetch, and this may not always be the case. When this happens the user can Mark an Opcode (a Sample or Cycle in the List display) to help the disassembler re-synchronize. To do this, the user first moves the mouse cursor to

the cycle that is to be marked. Click on the right mouse button to bring up the menu selections, then click on Mark Opcode. Another window will appear (see Figure 5) which permits selecting the type of cycle that is to be marked (Opcode Fetch, Memory Read, etc.). Select the desired cycle and then click on Okay. To remove an existing Mark, select Undo Mark and then click on OK. Low Opcode and High Opcode fetches may also be marked in this manner.



**Figure 5- Mark Opcode Window**

## 6.8 Instruction Decoding/Addressing Modes Supported

The following lists the particular feature sets that the NEX-IXP1200 disassembler packages supports.

**IMPORTANT:** The Thumb instruction set is not supported at this time.

Architecture v4 Level Instructions and Addressing modes

- Load data read cycle detection
- LDM and LDC multiple load read cycle detection
- Branch Prefetch Instruction flush detection
- Mark-Opcode support

All five addressing modes:

Addressing Mode 1

- Shifter operands
- Immediate
- Register

- Logical shift left by immediate
- Logical shift left by register
- Logical shift right by immediate
- Logical shift right by register
- Arithmetic shift right by immediate
- Arithmetic shift right by register
- Rotate right by immediate
- Rotate right by register
- Rotate right with extend

#### Addressing Mode 2

- Immediate offset
- Register offset
- Scaled register offset
- Immediate pre-indexed
- Register pre-indexed
- Scaled register pre-indexed
- Immediate post-indexed
- Register post-indexed
- Scaled register post-indexed

#### Addressing Mode 3

- Immediate offset
- Register offset
- Immediate pre-indexed
- Register pre-indexed
- Immediate post-indexed
- Register post-indexed

#### Addressing Mode 4

- Increment after
- Increment before
- Decrement after
- Decrement before

#### Addressing Mode 5

- Immediate offset
- Immediate pre-indexed
- Immediate post-indexed

## 6.9 IXP1200 Instructions Supported

ADC	{<cond>}{S} Rd, Rn, <shifter_operand>
ADD	{<cond>}{S} Rd, Rn, <shifter_operand>
AND	{<cond>}{S} Rd, Rn, <shifter_operand>
B{L}	{<cond>} <target address>
BIC	{<cond>}{S} Rd, Rn, <shifter_operand>
BX	{<cond>} Rm
CDP	{<cond>} p<cp#>, <opcode_1>, CRd, CRn, CRm, <opcode_2>
CMN	{<cond>} Rn, <shifter_operand>
CMP	{<cond>} Rn, <shifter_operand>

EOR	{<cond>} {S} Rd, Rn, <shifter_operand>	
LDC	{<cond>} p<cp_num>, CRd, <addressing_mode>	
LDM	{<cond>} <addressing_mode> Rn{!}, <registers>	LDM(1)
LDM	{<cond>} <addressing_mode> Rn, <registers>^	LDM(2)
LDM	{<cond>} <addressing_mode> Rn{!}, <registers_and_pc>^	LDM(3)
LDR	{<cond>} Rd, <addressing_mode>	
LDR	{<cond>}B Rd, <addressing_mode>	
LDR	{<cond>}BT Rd, <post_indexed_addressing_mode>	
LDR	{<cond>}H Rd, <addressing_mode>	
LDR	{<cond>}SB Rd, <addressing_mode>	
LDR	{<cond>}SH Rd, <addressing_mode>	
LDR	{<cond>}T Rd, <post_indexed_addressing_mode>	
MCR	{<cond>} p<cp#>, <opcode_1>, Rd, CRn, CRm, <opcode_2>	
MLA	{<cond>} {<S>} Rd, Rm, Rs, Rn	
MOV	{<cond>} {S} Rd, <shifter_operand>	
MRC	{<cond>} p<cp#>, <opcode_1>, Rd, CRn, CRm, <opcode_2>	
MRS	{<cond>} Rd, CPSR	
MRS	{<cond>} Rd, SPSR	
MSR	{<cond>} Rd, CPSR_f, #32bit immediate	
MSR	{<cond>} Rd, CPSR_<fields>, Rm	
MSR	{<cond>} Rd, SPSR_f, #32bit immediate	
MSR	{<cond>} Rd, SPSR_<fields>, Rm	
MUL	{<cond>} {<S>} Rd, Rm, Rs	
MVN	{<cond>} {<S>} Rd, <shifter_operand>	
ORR	{<cond>} {S} Rd, Rn, <shifter_operand>	
RSB	{<cond>} {S} Rd, Rn, <shifter_operand>	
RSC	{<cond>} {S} Rd, Rn, <shifter_operand>	
SBC	{<cond>} {S} Rd, Rn, <shifter_operand>	
SMLAL	{<cond>} {<S>} RdLo, RdHi, Rm, Rs	
SMULL	{<cond>} {<S>} RdLo, RdHi, Rm, Rs	
STC	{<cond>} p<cp_num>, CRd, <addressing_mode>	
STM	{<cond>} <addressing_mode> Rn{!}, <registers>	STM(1)
STM	{<cond>} <addressing_mode> Rn{!}, <registers>^	STM(2)
STR	{<cond>} Rd, <addressing_mode>	
STR	{<cond>}B Rd, <addressing_mode>	
STR	{<cond>}BT Rd, <post_indexed_addressing_mode>	
STR	{<cond>}H Rd, <addressing_mode>	
STR	{<cond>}T Rd, <post_indexed_addressing_mode>	
SUB	{<cond>} {<S>} Rd, Rn, <shifter_operand>	
SWI	{<cond>} <24_bit_immediate>	
SWP	{<cond>} Rd, Rm, [Rn]	
SWP	{<cond>}B Rd, Rm, [Rn]	
TEQ	{<cond>} Rn, <shifter_operand>	
TST	{<cond>} Rn, <shifter_operand>	
UMLAL	{<cond>} {<S>} RdLo, RdHi, Rm, Rs	
UMULL	{<cond>} {<S>} RdLo, RdHi, Rm, Rs	

## **7.0 THE NEX-IXP1200 CONTROL GROUP SYMBOL TABLE**

The use of Symbol Tables when displaying state data and defining a trigger enables the user to quickly determine the type of bus cycle that occurred or is desired. A symbol table for the Control group (IXP1200\_Ctrl, Table 3) has been provided to quickly show the type of bus transaction acquired when viewing data in Listing display. This same symbol table can be used in the Trigger area of the TLA to easily define the sort of bus cycle that is to be triggered on.

<b>Pattern</b>	<b>TLA700 Symbols</b>	<b>Meaning</b>
01x1	RAS_CYCLE	RAS Address cycle
01x0	PRECHARGE	SD RAM Precharge cycle
10x1	CAS_CYCLE-READ	CAS Address (Read) cycle
10x0	CAS_CYCLE-WRITE	CAS Address (Write) cycle
xx00	WRITE	Write Cycle
xx01	READ/FETCH	Instruction Fetch/Data Read cycle

**Table 2- NEX-IXP1200 Control Symbol Table**

Signals, from left to right: RAS#,CAS#,DQM,WR#

## APPENDIX A - Mictor Pin Assignments

**IMPORTANT:** Refer to the Tektronix P6434 Mass Termination Probe Manual for complete information on properly adding Mictor connectors to a target design.

Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #
3	5	CLK:0			36	6	CLK:1		
4	7	A3:7	MDATA[63]	AH6	35	8	A1:7	MDATA[47]	AE2
5	9	A3:6	MDATA[62]	AJ5	34	10	A1:6	MDATA[46]	AE1
6	11	A3:5	MDATA[61]	AL4	33	12	A1:5	MDATA[45]	U4
7	13	A3:4	MDATA[60]	AK4	32	14	A1:4	MDATA[44]	V2
8	15	A3:3	MDATA[59]	AH5	31	16	A1:3	MDATA[43]	U3
9	17	A3:2	MDATA[58]	AH2	30	18	A1:2	MDATA[42]	U2
10	19	A3:1	MDATA[57]	AH1	29	20	A1:1	MDATA[41]	U1
11	21	A3:0	MDATA[56]	AG3	28	22	A1:0	MDATA[40]	T4
12	23	A2:7	MDATA[55]	AF4	27	24	A0:7	MDATA[39]	T3
13	25	A2:6	MDATA[54]	AG2	26	26	A0:6	MDATA[38]	T2
14	27	A2:5	MDATA[53]	AG1	25	28	A0:5	MDATA[37]	T1
15	29	A2:4	MDATA[52]	AF3	24	30	A0:4	MDATA[36]	R3
16	31	A2:3	MDATA[51]	AF2	23	32	A0:3	MDATA[35]	R4
17	33	A2:2	MDATA[50]	AF1	22	34	A0:2	MDATA[34]	P2
18	35	A2:1	MDATA[49]	AE3	21	36	A0:1	MDATA[33]	P3
19	37	A2:0	MDATA[48]	AD4	20	38	A0:0	MDATA[32]	N1

### Mictor Group A

Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #
3	5	CLK:3	SDCLK	AD2	36	6	QUAL:1	do not use	---
4	7	C3:7	MADR[11]	AC2	35	8	C1:7	MADR[13]	AD1
5	9	C3:6	MADR[10]	AC1	34	10	C1:6	MADR[12]	AC3
6	11	C3:5	MADR[9]	AB3	33	12	C1:5	do not use	---
7	13	C3:4	MADR[8]	AA4	32	14	C1:4	do not use	---
8	15	C3:3	MADR[7]	AB2	31	16	C1:3	do not use	---
9	17	C3:2	MADR[6]	AB1	30	18	C1:2	do not use	---
10	19	C3:1	MADR[5]	AA3	29	20	C1:1	do not use	---
11	21	C3:0	MADR[4]	AA1	28	22	C1:0	do not use	---
12	23	C2:7	MADR[3]	Y3	27	24	C0:7	do not use	---
13	25	C2:6	MADR[2]	W4	26	26	C0:6	do not use	---
14	27	C2:5	MADR[1]	Y2	25	28	C0:5	do not use	---
15	29	C2:4	MADR[0]	Y1	24	30	C0:4	do not use	---
16	31	C2:3	DQM	V3	23	32	C0:3		
17	33	C2:2	WE#	W1	22	34	C0:2		
18	35	C2:1	CAS#	W3	21	36	C0:1		
19	37	C2:0	RAS#	W2	20	38	C0:0	PARITY	AK5

### Mictor Group C

Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ TLA700 Channel	IXP1200 Signal Name	IXP1200 Pin #
3	5	QUAL:0	do not use	---	36	6	CLK:2		
4	7	D3:7	MDATA[31]	N2	35	8	D1:7	MDATA[15]	H2
5	9	D3:6	MDATA[30]	N3	34	10	D1:6	MDATA[14]	J4
6	11	D3:5	MDATA[29]	M1	33	12	D1:5	MDATA[13]	H3
7	13	D3:4	MDATA[28]	M2	32	14	D1:4	MDATA[12]	G1
8	15	D3:3	MDATA[27]	N4	31	16	D1:3	MDATA[11]	G2
9	17	D3:2	MDATA[26]	M3	30	18	D1:2	MDATA[10]	H4
10	19	D3:1	MDATA[25]	L1	29	20	D1:1	MDATA[9]	G3
11	21	D3:0	MDATA[24]	L2	28	22	D1:0	MDATA[8]	F1
12	23	D2:7	MDATA[23]	M4	27	24	D0:7	MDATA[7]	F2
13	25	D2:6	MDATA[22]	L3	26	26	D0:6	MDATA[6]	F3
14	27	D2:5	MDATA[21]	K1	25	28	D0:5	MDATA[5]	E1
15	29	D2:4	MDATA[20]	K3	24	30	D0:4	MDATA[4]	E2
16	31	D2:3	MDATA[19]	J1	23	32	D0:3	MDATA[3]	F4
17	33	D2:2	MDATA[18]	J2	22	34	D0:2	MDATA[2]	E3
18	35	D2:1	MDATA[17]	J3	21	36	D0:1	MDATA[1]	D1
19	37	D2:0	MDATA[16]	H1	20	38	D0:0	MDATA[0]	D2

### Mictor Group D

## **APPENDIX B – IXP1200 P6860 Compression Pinouts**

For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00..

Pad #	TLA Channel	IXP1200 Signal Name	IXP1200 Pin #
A15	CK1-		
A13	CK1+		
B12	A1:7	MDATA[47]	AE2
B10	A1:6	MDATA[46]	AE1
A12	A1:5	MDATA[45]	U4
A10	A1:4	MDATA[44]	V2
B9	A1:3	MDATA[43]	U3
B7	A1:2	MDATA[42]	U2
A9	A1:1	MDATA[41]	U1
A7	A1:0	MDATA[40]	T4
B6	A0:7	MDATA[39]	T3
B4	A0:6	MDATA[38]	T2
A6	A0:5	MDATA[37]	T1
A4	A0:4	MDATA[36]	R3
B3	A0:3	MDATA[35]	R4
B1	A0:2	MDATA[34]	P2
A3	A0:1	MDATA[33]	P3
A1	A0:0	MDATA[32]	N1

**Probe Connection A0/A1**

Pad #	TLA Channel	IXP1200 Signal Name	IXP1200 Pin #
A15	CK0-		
A13	CK0+		
B12	A3:7	MDATA[63]	AH6
B10	A3:6	MDATA[62]	AJ5
A12	A3:5	MDATA[61]	AL4
A10	A3:4	MDATA[60]	AK4
B9	A3:3	MDATA[59]	AH5
B7	A3:2	MDATA[58]	AH2
A9	A3:1	MDATA[57]	AH1
A7	A3:0	MDATA[56]	AG3
B6	A2:7	MDATA[55]	AF4
B4	A2:6	MDATA[54]	AG2
A6	A2:5	MDATA[53]	AG1
A4	A2:4	MDATA[52]	AF3
B3	A2:3	MDATA[51]	AF2
B1	A2:2	MDATA[50]	AF1
A3	A2:1	MDATA[49]	AE3
A1	A2:0	MDATA[48]	AD4

**Probe Connection A2/A3**

Pad #	TLA Channel	IXP1200 Signal Name	IXP1200 Pin #
A15	Q1-		
A13	Q1+	do not use	---
B12	C1:7	MADR[13]	AD1
B10	C1:6	MADR[12]	AC3
A12	C1:5	do not use	---
A10	C1:4	do not use	---
B9	C1:3	do not use	---
B7	C1:2	do not use	---
A9	C1:1	do not use	---
A7	C1:0	do not use	---
B6	C0:7	do not use	---
B4	C0:6	do not use	---
A6	C0:5	do not use	---
A4	C0:4	do not use	---
B3	C0:3		
B1	C0:2		
A3	C0:1		
A1	C0:0	PARITY	AK5

**Probe Connection C0/C1**

Pad #	TLA Channel	IXP1200 Signal Name	IXP1200 Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	SDCLK	AD2
B12	C3:7	MADR[11]	AC2
B10	C3:6	MADR[10]	AC1
A12	C3:5	MADR[9]	AB3
A10	C3:4	MADR[8]	AA4
B9	C3:3	MADR[7]	AB2
B7	C3:2	MADR[6]	AB1
A9	C3:1	MADR[5]	AA3
A7	C3:0	MADR[4]	AA1
B6	C2:7	MADR[3]	Y3
B4	C2:6	MADR[2]	W4
A6	C2:5	MADR[1]	Y2
A4	C2:4	MADR[0]	Y1
B3	C2:3	DQM	V3
B1	C2:2	WE#	W1
A3	C2:1	CAS#	W3
A1	C2:0	RAS#	W2

**Probe Connection C2/C3**

Pad #	TLA Channel	IXP1200 Signal Name	IXP1200 Pin #
A15	CK2-		
A13	CK2+		
B12	D1:7	MDATA[15]	H2
B10	D1:6	MDATA[14]	J4
A12	D1:5	MDATA[13]	H3
A10	D1:4	MDATA[12]	G1
B9	D1:3	MDATA[11]	G2
B7	D1:2	MDATA[10]	H4
A9	D1:1	MDATA[9]	G3
A7	D1:0	MDATA[8]	F1
B6	D0:7	MDATA[7]	F2
B4	D0:6	MDATA[6]	F3
A6	D0:5	MDATA[5]	E1
A4	D0:4	MDATA[4]	E2
B3	D0:3	MDATA[3]	F4
B1	D0:2	MDATA[2]	E3
A3	D0:1	MDATA[1]	D1
A1	D0:0	MDATA[0]	D2

**Probe Connection D0/D1**

Pad #	TLA Channel	IXP1200 Signal Name	IXP1200 Pin #
A15	Q0-		
A13	Q0+	do not use	---
B12	D3:7	MDATA[31]	N2
B10	D3:6	MDATA[30]	N3
A12	D3:5	MDATA[29]	M1
A10	D3:4	MDATA[28]	M2
B9	D3:3	MDATA[27]	N4
B7	D3:2	MDATA[26]	M3
A9	D3:1	MDATA[25]	L1
A7	D3:0	MDATA[24]	L2
B6	D2:7	MDATA[23]	M4
B4	D2:6	MDATA[22]	L3
A6	D2:5	MDATA[21]	K1
A4	D2:4	MDATA[20]	K3
B3	D2:3	MDATA[19]	J1
B1	D2:2	MDATA[18]	J2
A3	D2:1	MDATA[17]	J3
A1	D2:0	MDATA[16]	H1

**Probe Connection D2/D3**

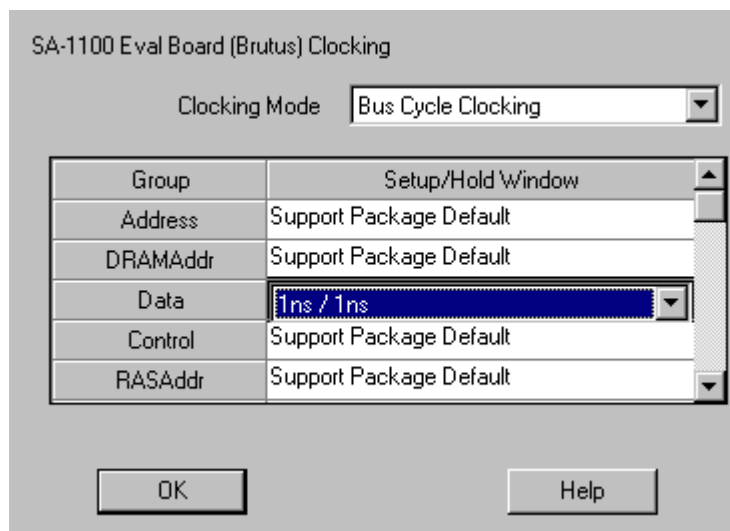
## **APPENDIX C - Necessary Signals for Clocking**

To properly acquire IXP1200 bus activity in Bus Cycle Clocking mode (see Section 5.0 for further information on this mode), the following signals must be provided: SDCLK, RAS#, CAS#, DQM, and WE#. If Bus Cycle Clocking does not work, move to the Activity Indicator window of the TLA and observe that all of these signals are toggling.

When using the NEX-IXP1200 support in Every Edge of SDCLK mode, the only signal that is required is SDCLK, and this signal must show activity in the Activity Indicator window of the TLA.

## APPENDIX D – Clocking Considerations

Because of timing differences between versions of IXP1200 micros, and also due to design of the target, it may be necessary to adjust the sample point of some of the acquisition groups for ensure proper data acquisition. The TLA7X3/4 Logic Analyzer cards require a 2ns stable data window to guarantee data acquisition, and by default this window is defined as 2ns Setup / 0ns Hold (for all groups) relative to the SDCLK clock edge. The TLA7AX3/4 Logic Analyzer cards require a 625ps typical stable data window to guarantee data acquisition. However, this Setup and Hold value can be adjusted on a group-by-group basis to meet the target's timing requirements. This is done by moving to the LA card's Setup window and clicking on the **More** button next to the right of the Clocking field. A window similar to that shown in Figure 6 will appear. In this example the Address, DRAMAddr, Control and RASAddr groups have been left at the Support Package Defaults selection, which is defined as 2ns Setup / 0ns Hold. The Data group has been adjusted to 1ns Setup / 1ns Hold. When using a TLA running V3.0 software these adjustments are made by left-clicking on the Setup/Hold Window field and then choosing the desired Setup value from the menu field. The process may be slightly different when using earlier versions of TLA software.



**Figure 6- Setup & Hold Adjustment**

## **APPENDIX E – IXP1200 Pinout**

<b>Signal Name</b>	<b>Pin Number</b>	<b>Signal Name</b>	<b>Pin Number</b>	<b>Signal Name</b>	<b>Pin Number</b>
A[0]	J28	FDAT[42]	AK26	RDYCTL#[4]	AK5
A[1]	H29	FDAT[43]	AJ26	REQ#[0]	A21
A[10]	E30	FDAT[44]	AL27	REQ#[1]	D19
A[11]	F28	FDAT[45]	AK27	RESET_IN#	C6
A[12]	E29	FDAT[46]	AH26	RESET_OUT	A5
A[13]	D31	FDAT[47]	AJ27	RXD	D23
A[14]	D30	FDAT[48]	AL28	RXFAIL	AK10
A[15]	E28	FDAT[49]	AK28	SACLK	B24
A[16]	D27	FDAT[5]	AL16	SCAN_EN	C5
A[17]	B28	FDAT[50]	AH27	SCLK	W31
A[18]	A28	FDAT[51]	AH30	SDCLK	AD2
A[2]	G31	FDAT[52]	AH31	SERR#	B11
A[3]	G30	FDAT[53]	AG29	SLOW_EN#	Y29
A[4]	H28	FDAT[54]	AF28	SLOW_RD#	Y31
A[5]	G29	FDAT[55]	AG30	SLOW_WE#	W28
A[6]	F31	FDAT[56]	AG31	SOE#	W30
A[7]	F30	FDAT[57]	AF29	SOP	AH12
A[8]	F29	FDAT[58]	AF30	SOP32	AJ6
A[9]	E31	FDAT[59]	AF31	SP_CE#	W29
AD[0]	B6	FDAT[6]	AK16	STOP#	C12
AD[1]	A6	FDAT[60]	AE30	SWE#	Y30
AD[10]	B9	FDAT[61]	AE31	TCK	A23
AD[11]	A9	FDAT[62]	AD29	TCK_BYP	D6
AD[12]	C10	FDAT[63]	AC28	TDI	B22
AD[13]	D11	FDAT[7]	AJ16	TDO	D21
AD[14]	B10	FDAT[8]	AH16	TK_IN	AB31
AD[15]	A10	FDAT[9]	AL17	TK_OUT	AA29
AD[16]	A13	FPS[0]	AD30	TMS	C22
AD[17]	C14	FPS[1]	AD31	TRDY#	B12
AD[18]	D15	FPS[2]	AC29	TRST#	B23
AD[19]	B14	FRAME#	C13	TSTCLK	B5
AD[2]	C7	GNT#[0]	B21	TXASIS	AL10
AD[20]	C15	GNT#[1]	C20	TXD	C24
AD[21]	B15	GPIO[0]	C26	VDD	A19
AD[22]	A15	GPIO[1]	D24	VDD	B19

## IXP1200 Pinout (cont'd)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
AD[23]	D16	GPIO[2]	B25	VDD	B27
AD[24]	A16	GPIO[3]	A25	VDD	H31
AD[25]	C17	HIGH_EN#	C27	VDD	J29
AD[26]	D17	IDSEL	C16	VDD	K2
AD[27]	B18	IRDY#	A12	VDD	L4
AD[28]	C18	LOW_EN#	D26	VDD	Y4
AD[29]	C19	MADR[0]	Y1	VDD	AA2
AD[3]	D8	MADR[1]	Y2	VDD	AA30
AD[30]	A20	MADR[10]	AC1	VDD	AA31
AD[31]	B20	MADR[11]	AC2	VDD	AC4
AD[4]	B7	MADR[12]	AC3	VDD	AD3
AD[5]	A7	MADR[13]	AD1	VDD	AD28
AD[6]	C8	MADR[2]	W4	VDD	AE29
AD[7]	D9	MADR[3]	Y3	VDD	AG4
AD[8]	A8	MADR[4]	AA1	VDD	AG28
AD[9]	C9	MADR[5]	AA3	VDD_REF	E4
CAS#	W3	MADR[6]	AB1	VDDP1	D5
CBE#[0]	B8	MADR[7]	AB2	VDDX	A1
CBE#[1]	C11	MADR[8]	AA4	VDDX	A31
CBE#[2]	B13	MADR[9]	AB3	VDDX	B2
CBE#[3]	B16	MDATA[0]	D2	VDDX	B30
CE#[0]	A27	MDATA[1]	D1	VDDX	C3
CE#[1]	C26	MDATA[10]	H4	VDDX	C29
CE#[2]	B26	MDATA[11]	G2	VDDX	D4
CE#[3]	A26	MDATA[12]	G1	VDDX	D7
CINT#	Y28	MDATA[13]	H3	VDDX	D10
DEVSEL#	D13	MDATA[14]	J4	VDDX	D14
DQ[0]	V29	MDATA[15]	H2	VDDX	D18
DQ[1]	V30	MDATA[16]	H1	VDDX	D22
DQ[10]	R29	MDATA[17]	J3	VDDX	D25
DQ[11]	P30	MDATA[18]	J2	VDDX	D28
DQ[12]	R28	MDATA[19]	J1	VDDX	G4
DQ[13]	P29	MDATA[2]	E3	VDDX	G28
DQ[14]	N31	MDATA[20]	K3	VDDX	K4
DQ[15]	N30	MDATA[21]	K1	VDDX	K28
DQ[16]	N29	MDATA[22]	L3	VDDX	P4
DQ[17]	M31	MDATA[23]	M4	VDDX	P28
DQ[18]	M30	MDATA[24]	L2	VDDX	V4

## **IXP1200 Pinout (cont'd)**

<b>Signal Name</b>	<b>Pin Number</b>	<b>Signal Name</b>	<b>Pin Number</b>	<b>Signal Name</b>	<b>Pin Number</b>
DQ[19]	N28	MDATA[25]	L1	VDDX	V26
DQ[2]	U28	MDATA[26]	M3	VDDX	AB4
DQ[20]	M29	MDATA[27]	N4	VDDX	AB28
DQ[21]	L31	MDATA[28]	M2	VDDX	AE4
DQ[22]	L30	MDATA[29]	M1	VDDX	AE28
DQ[23]	M28	MDATA[3]	F4	VDDX	AH4
DQ[24]	L29	MDATA[30]	N3	VDDX	AH7
DQ[25]	K31	MDATA[31]	N2	VDDX	AH10
DQ[26]	K30	MDATA[32]	N1	VDDX	AH14
DQ[27]	L28	MDATA[33]	P3	VDDX	AH18
DQ[28]	K29	MDATA[34]	P2	VDDX	AH22
DQ[29]	J31	MDATA[35]	R4	VDDX	AH25
DQ[3]	U29	MDATA[36]	R3	VDDX	AH28
DQ[30]	J30	MDATA[37]	T1	VDDX	AJ3
DQ[31]	H30	MDATA[38]	T2	VDDX	AJ29
DQ[4]	T31	MDATA[39]	T3	VDDX	AK2
DQ[5]	T30	MDATA[4]	E2	VDDX	AK30
DQ[6]	T29	MDATA[40]	T4	VDDX	AL1
DQ[7]	T28	MDATA[41]	U1	VDDX	AL31
DQ[8]	R31	MDATA[42]	U2	VSS	A2
DQ[9]	R30	MDATA[43]	U3	VSS	A3
DQM	V3	MDATA[44]	V2	VSS	A14
EDP	AJ11	MDATA[45]	U4	VSS	A17
EOP32	AL5	MDATA[46]	AE1	VSS	A18
FAST_RX1	AH11	MDATA[47]	AE2	VSS	A29
FAST_RX2	AJ10	MDATA[48]	AD4	VSS	A30
FBE#[0]	AK11	MDATA[49]	AE3	VSS	B1
FBE#[1]	AL11	MDATA[5]	E1	VSS	B3
FBE#[2]	AJ12	MDATA[50]	AF1	VSS	B17
FBE#[3]	AH13	MDATA[51]	AF2	VSS	B29
FBE#[4]	AK12	MDATA[52]	AF3	VSS	B31
FBE#[5]	AL12	MDATA[53]	AG1	VSS	C1
FBE#[6]	AJ13	MDATA[54]	AG2	VSS	C2
FBE#[7]	AK13	MDATA[55]	AF4	VSS	C4
FCLK	AB30	MDATA[56]	AG3	VSS	C28
FDAT[0]	AL13	MDATA[57]	AH1	VSS	C30
FDAT[1]	AJ14	MDATA[58]	AH2	VSS	C31
FDAT[10]	AK17	MDATA[59]	AH5	VSS	D3

## IXP1200 Pinout (cont'd)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
FDAT[11]	AJ17	MDATA[6]	F3	VSS	D29
FDAT[12]	AK18	MDATA[60]	AK4	VSS	P1
FDAT[13]	AH17	MDATA[61]	AL4	VSS	P31
FDAT[14]	AJ18	MDATA[62]	AJ5	VSS	R1
FDAT[15]	AL19	MDATA[63]	AH6	VSS	R2
FDAT[16]	AK19	MDATA[7]	F2	VSS	U30
FDAT[17]	AJ19	MDATA[8]	F1	VSS	U31
FDAT[18]	AL20	MDATA[9]	G3	VSS	V1
FDAT[19]	AK20	PAR	D12	VSS	V31
FDAT[2]	AK14	PARITY	AK5	VSS	AH3
FDAT[20]	AH19	PCI_CFN[0]	A24	VSS	AH29
FDAT[21]	AJ20	PCI_CFN[1]	C23	VSS	AJ1
FDAT[22]	AL21	PCI_CLK	D20	VSS	AJ2
FDAT[23]	AK21	PCI_IRQ#	A22	VSS	AJ4
FDAT[24]	AH20	PCI_RST#	C21	VSS	AJ28
FDAT[25]	AJ21	PERR#	A11	VSS	AJ30
FDAT[26]	AL22	PORTCTL#[0]	AA28	VSS	AJ31
FDAT[27]	AK22	PORTCTL#[1]	AB29	VSS	AK1
FDAT[28]	AH21	PORTCTL#[2]	AC31	VSS	AK3
FDAT[29]	AJ22	PORTCTL#[3]	AC30	VSS	AK15
FDAT[3]	AH15	PXTAL	B4	VSS	AK29
FDAT[30]	AL23	RAS#	W2	VSS	AK31
FDAT[31]	AK23	RDYBUS[0]	AL7	VSS	AL2
FDAT[32]	AJ23	RDYBUS[1]	AJ8	VSS	AL3
FDAT[33]	AL24	RDYBUS[2]	AH9	VSS	AL14
FDAT[34]	AK24	RDYBUS[3]	AK8	VSS	AL15
FDAT[35]	AH23	RDYBUS[4]	AL8	VSS	AL18
FDAT[36]	AJ24	RDYBUS[5]	AJ9	VSS	AL29
FDAT[37]	AL25	RDYBUS[6]	AK9	VSS	AL30
FDAT[38]	AK25	RDYBUS[7]	AL9	VSSP1	A4
FDAT[39]	AH24	RDYCTL#[0]	AK7	WE#	W1
FDAT[4]	AJ15	RDYCTL#[1]	AH8	RDYCTL#[4]	AK6
FDAT[40]	AJ25	RDYCTL#[2]	AJ7		
FDAT[41]	AL26	RDYCTL#[3]	AL6		

## **APPENDIX F - Support**

### **About Nexus Technology, Inc.**



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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### **Support Contact Information**

Technical Support	<b><a href="mailto:techsupport@nexustechnology.com">techsupport@nexustechnology.com</a></b>
General Information	<b><a href="mailto:support@nexustechnology.com">support@nexustechnology.com</a></b>
Quote Requests	<b><a href="mailto:quotes@nexustechnology.com">quotes@nexustechnology.com</a></b>

We will try to respond within one business day.

### **If Problems Are Found**

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

## **APPENDIX G - References**

Tektronix TLA700 System User's Manual

Tektronix TLA700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

“Advanced RISC Machines Architectural Reference Manual”

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