NEX-MINIPCIT3A
MiniPCI Type 3A Bus Adapter Users Manual

Including these Software Support packages:
MINIPCI

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1.0 OVERVIEW

1.1 General Information

The NEX-MiniPCIT3A adapter has been designed to provide quick and easy connections to interface a 102, or 136-channel TLA700/600 acquisition module to a 32-bit mini-PCIT3A socket. (The PCI designation refers to the Peripheral Component Interconnect Local Bus specification.) Connections are made through P6434 probes when using a TLA700/600. The P6434 probes are available from Tektronix.

The included NEX-MINIPCI SW permits the acquisition of all PCI bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. For instance, references to the TLA700 apply to a TLA600 or TLA700 system with one or more TLA7*3/4 acquisition cards.

Appendix D is a silk-screen print of the NEX-MINIPCIT3A Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the Mini-PCI Local Bus specification and the Tektronix TLA700 Logic Analyzer. Also, it is expected that the user is familiar with Windows.

2.0 SOFTWARE INSTALLATION

One 3½" diskette has been included with the NEX-MINIPCIT3A Bus Adapter. It is for use with the TLA700/600 series.

2.1 TLA700

The NEX-MINIPCIT3A software is loaded in the same method as other Windows programs. Choose which support is to be loaded: use the disk labeled 102-channel support with a 102- or 136-channel card. Place the NEX-MINIPCIT3A Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the MiniPCI support in its proper place on the hard disk.

To load MiniPCI support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select **Load Support Package** from the File pull-down, then choose **MiniPCI** and click on **Okay**.

3.0 CONFIGURING the NEX- MINIPCIT3A BUS ADAPTER

3.1 General Information

Not all 32-bit PCI signals are monitored by the TLA700 (Refer to Table 1 or Table 2 for a list of acquired signals.) The remaining signals have been brought to a 2x14 header so that they can be monitored, if desired, simply by connecting unused data channels to them. The signals are on the pins nearest the signal names. The leftmost row of pins (opposite the signals) are all connected to signal ground.

3.2 Pad Area

There is a pad area on the top left of the NEX-MINIPCIT3A adapter. This is provided to connect Mini-PCI "reserve" signals to mictor inputs for acquisition with the TLA. Up to two signals can be connected to mictor inputs. This is accomplished by soldering a wire from the pads labeled R1, R2, R3, R4, R5, R6, R7, R8, RW1 or RW2 to mictor input pads labeled P1 and P2. The following defines the signal definition of the pads.

Input to Mictor C Connector

Pad on NEXMiniPCIT3A	Mictor "C" Input Pin
P1	4
P2	5

Pad Definition For Reserve Signals

Pad on NEXMINIPCIT3A	MiniPCI Signal/Pin #
R1	Reserved1 / **21**
R2	Reserved2 / **43**
R3	Reserved3 / **16**
R4	Reserved4 / **22**
R5	Reserved5 / **36**
R6	Reserved6 / **93**
R7	Reserved7 / **121**
R8	Reserved8 / **112**
RW1	Reserved_WIP1 / **98**
RW2	Reserved_WIP2 / **100**

4.0 CONNECTING to the NEX-MINPCIT3A ADAPTER

4.1 General

The NEX-MINIPCIT3A is an extender card that is also designed to permit monitoring of the Mini-PCI bus signals. This allows the user to see exactly what is happening at the target. It is important to note that using this card as an extender will violate the PCI specification for stub length. Every effort has been taken to keep trace length as short as possible. It is entirely possible, however, that placing a target card onto the NEX-MINIPCIT3A extender will result in improper operation of the target card.

The NEX-MINIPCIT3A adapter is a rigid/flex/rigid design. When connecting it to the target, care should be used so the flex is not stressed. The adapter was designed so the flex can be carefully lifted relative to the bottom rigid board. This provides mechanical clearance for the adapter. The flex can be carefully lifted a maximum of 90 degrees relative to the bottom rigid board. The flex bend should never exceed 90 degrees. Pulling the flex away from either rigid board can permanently damage the adapter.

4.2 TLA700

When using a TLA700 with the NEX-MINIPCIT3A adapter board it is necessary to use the P6434 high-density probes for connecting to the board. Each P6434 probe consists of one high-density probe tip (which connects to the adapter board) and two module ends (which connect to the acquisition card). It is important to note that where the module ends connect to the acquisition card will depend on how many channels the acquisition card has. Be very careful in

noting where Pin 1 is on each probe tip, and follow the P6434 Mass Termination Probe manual for instructions on applying the labels.

When using a TLA7*3/4 102/136-channel acquisition module, the necessary acquisition data sections are A0-A3 and C0-C3. One P6434 plugs onto the Group A connector on the MiniPCI adapter and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434 plugs onto the Group C connector on the MiniPCI adapter and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. Table 1 shows the wiring and Channel Grouping for the 102/136-channel TLA700 NEX-MINIPCIT3A connection.

Group Name	Signal Name	MiniPCI Pin #	TLA700 input	Group Name	Signal Name	MiniPCI Pin #	TLA700 Input
Addr_Dat	AD[31]	33	A3:7	Control	RST#	26	QUAL1
(Hex)	AD[30]	38	A3:6	(Sym)	FRAME#	64	C2:0
	AD[29]	35	A3:5		DEVSEL#	72	CLK1
	AD[28]	42	A3:4		STOP#	68	C2:3
	AD[27]	39	A3:3		IRDY#	61	C2:1
	AD[26]	44	A3:2		TRDY#	66	C2:2
	AD[25]	41	A3:1		C/BE#[3]	45	C2:7
	AD[24]	46	A3:0		C/BE#[2]	59	C2:6
	AD[23]	47	A2:7		C/BE#[1]	73	C2:5
	AD[22]	52	A2:6		C/BE#[0]	86	C2:4
	AD[21]	51	A2:5	Intrpt	INTB#	17	C0:1
	AD[20]	54	A2:4	(Off)	INTA#	20	C0:0
	AD[19]	53	A2:3	Misc	REQ#	29	C1:5
	AD[18]	58	A2:2	(Off)	GNT#	30	C1:6
	AD[17]	57	A2:1		IDSEL	48	C1:4
	AD[16]	60	A2:0		PERR#	71	C3:3
	AD[15]	76	A1:7		PAR	56	C3:2
	AD[14]	75	A1:6		SERR#	67	C3:1
	AD[13]	78	A1:5		CLKRUN#	65	C1:1
	AD[12]	79	A1:4		CLK	25	CLK3
	AD[11]	80	A1:3	AC_Sigs	AC_BIT_CLK	107	CLK0
	AD[10]	81	A1:2	(Off)	AC_SDATAOUT	106	C3:0
	AD[09]	84	A1:1		AC_SDATA_IN	105	C1:0
	AD[08]	85	A1:0		AC_SYNC	103	C3:5
	AD[07]	87	A0:7		AC_RESET#	110	C3:4
	AD[06]	90	A0:6		AC_CODEC_1#	109	C0:3
	AD[05]	91	A0:5		AC_CODEX_0#	108	C0:2
	AD[04]	92	A0:4	Other	M66EN	104	C1:7
	AD[03]	95	A0:3		MPCIACT#	122	C1:3
	AD[02]	94	A0:2		PME#	34	C1:2
	AD[01]	99	A0:1				
	AD[00]	96	A0:0				

Table 1- NEX-MINIPCIT3A TLA700 (102/136-channel) Wiring

5.0 CLOCK SELECTION

5.1 General Information

There are three clocking options available when using the NEX-MINIPCIT3A support package. Each is explained in detail below.

When using a TLA700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.2 Clocking Options - Explanation

Bus Cycle Acquisition - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will ***not*** be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge - In this mode, data will be acquired on every rising edge of the PCI CLK signal. The disassembly will filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

6.0 VIEWING DATA

6.1 Viewing Timing Data on the TLA700

By default, the TLA700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: MiniPCI and MiniPCI-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, MiniPCI-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA700 System User's Manual for additional information on formatting the Waveform display.

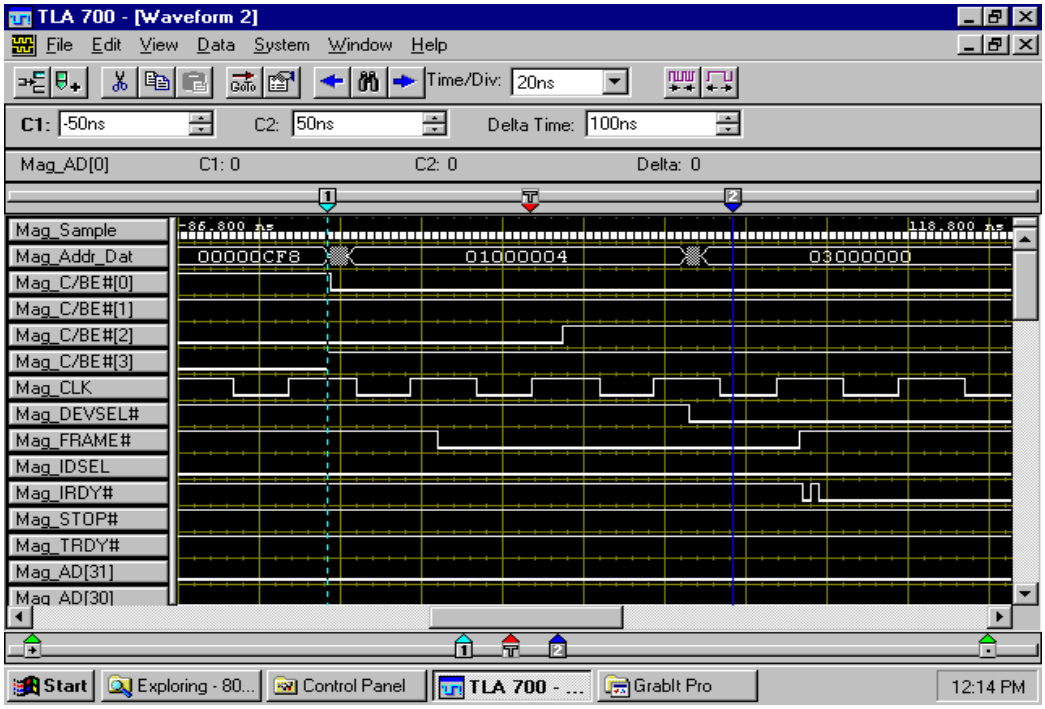


Figure 1- MiniPCI MagniVu Display on TLA700

Pattern	TLA700 Symbols	Meaning
0xxxxxxxxx	RESET	Reset
1011110000	INTERRUPT ACK	Interrupt Acknowledge
1011110001	SPECIAL CYCLE	Special Cycle
1011110010	I/O READ ADDRESS	I/O Read
1011110011	I/O WRITE ADDRESS	I/O Write
101111010x	RESERVED	Reserved
1011110110	MEMORY READ ADDRESS	Memory Read
1011110111	MEMORY WRITE ADDRESS	Memory Write
101111100x	RESERVED	Reserved
1011111010	CONFIG READ ADDRESS	Configuration Read
1011111011	CONFIG WRITE ADDRESS	Configuration Write
1011111100	MEMORY READ MULTIPLE	Memory Read Multiple
1011111101	DUAL ADDRESS	Dual Address Cycle
1011111110	MEMORY READ LINE	Memory Read Line
1011111111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
100x001111	ZERO_BYTE_OPERATION	Zero Byte Operation
1x0x001110	DATA - BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA - BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA - BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA - BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA - BYTES 0 & 1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA - BYTES 2 & 3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA - BYTES 0-3	Bytes 0-3 valid (D0-31)
110x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo
xxxxxxxxxx	UNDEFINED	Undefined

Table 2- NEX-MINIPCI32T3A Control Symbol Table

Signals, from left to right: RST#,
FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#,
C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

7.0 USING the DISASSEMBLY SOFTWARE

7.1 General

The MiniPCI support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the MiniPCI software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the MiniPCI software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes. the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps in the TLA700 series, permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Using the TLA700

The TLA700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

Add Column - Adds a column to the display
Add Mark - Adds a user mark to the display
Cut - (may be grayed out) - Cuts the selection to the Clipboard

Copy - (may be grayed out) - Copies the selection to the Clipboard
Paste - (may be grayed out) - Inserts the contents of the Clipboard
Go To - Moves the display to the item of interest
Properties - Edits the current Listing Display properties
Smaller Font - Decreases the displayed font size
Larger Font - Increases the displayed font size
Search Backward - Moves to a previous data match
Define Search - Define data to be matched
Search Forward - Moves to the next data match
Mark Opcode - Permits placing an opcode mark (disabled in MiniPCI)

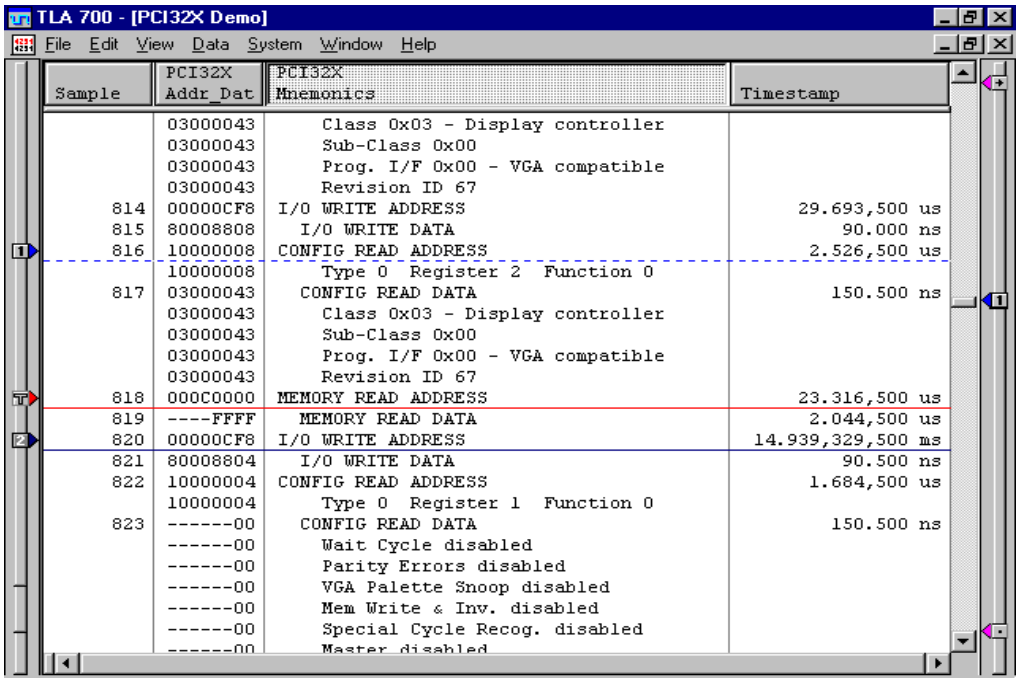


Figure 2- MiniPCI Disassembly

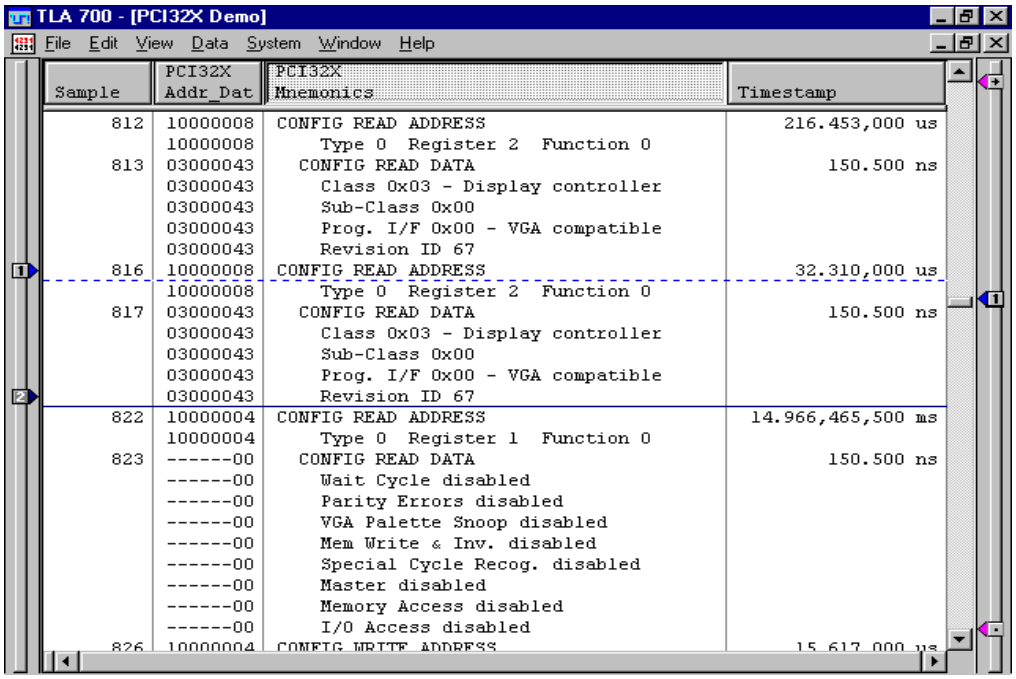


Figure 3- MiniPCI Disassembly with suppressed Memory and I/O Cycles

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the MiniPCI disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display

only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

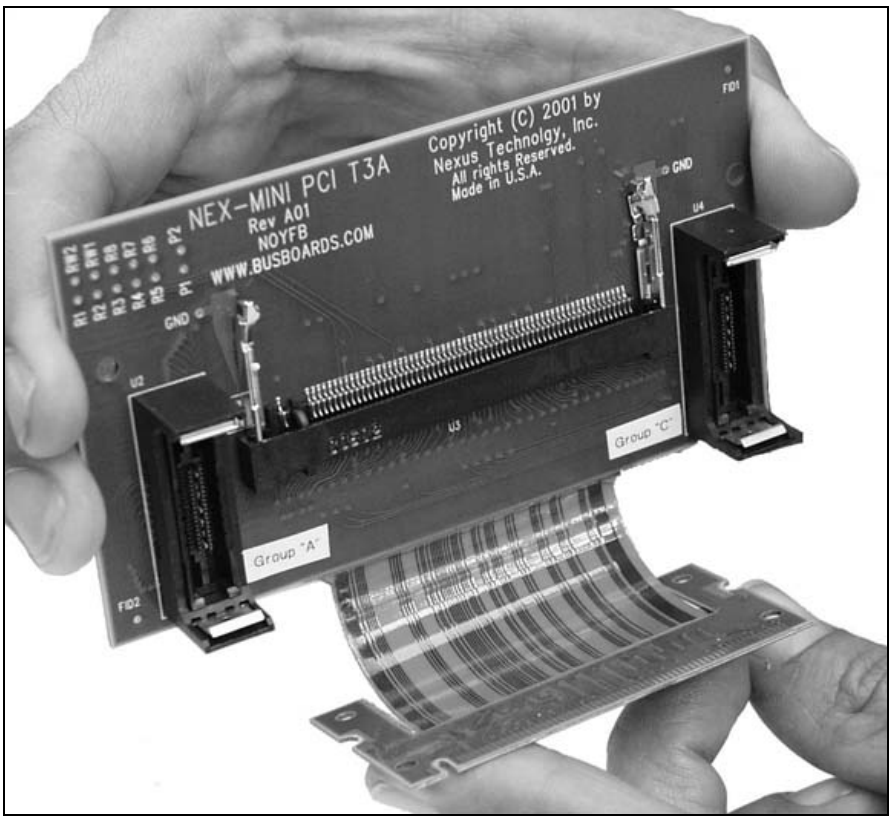
APPENDIX A - Necessary Signals for Clocking

To properly acquire Mini-PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

APPENDIX B - Considerations

The NEX-MINIPCIT3A is an extender card that is also designed to permit monitoring the PCI bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will violate the PCI specification for stub length. Every effort has been taken to keep trace length as short as possible. It is entirely possible, however, that placing a target card onto the NEX-MINIPCIT3A extender will result in improper operation of the target card.

The NEX-MINIPCIT3A adapter is a rigid/flex/rigid design. When connecting it to the target, care should be used so the flex is not stressed. The adapter was designed so the flex can be carefully lifted relative to the bottom rigid board. This provides mechanical clearance for the adapter. The flex can be carefully lifted a maximum of 90 degrees relative to the bottom rigid board. The flex bend should never exceed 90 degrees. Pulling the flex away from either rigid board can permanently damage the adapter.



The flex portion of the NEX-MINIPCIT3A can be bent for mechanical clearance in a target

APPENDIX C – MiniPCI Local Bus Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TIP	**2**	RING	**63**	3.3V	**64**	FRAME#
	Key		Key	**65**	CLKRUN#	**66**	TRDY#
3	8PMJ-3[3,4]	**4**	8PMJ-1[3,4]	**67**	SERR#	**68**	STOP#
5	8PMJ-6[3,4]	**6**	8PMJ-2[3,4]	**69**	GROUND	**70**	3.3V
7	8PMJ-7[3,4]	**8**	8PMJ-4[3,4]	**71**	PERR#	**72**	DEVSEL#
9	8PMJ-8[3,4]	**10**	8PMJ-5[3,4]	**73**	C/BE[1]#	**74**	GROUND
11	LED1_GRNP	**12**	LED2_YELP	**75**	AD[14]	**76**	AD[15]
13	LED1_GRNN	**14**	LED2_YELN	**77**	GROUND	**78**	AD[13]
15	CHSGND	**16**	RESERVED	**79**	AD[12]	**80**	AD[11]
17	INTB#	**18**	5V	**81**	AD[10]	**82**	GROUND
19	3.3V	**20**	INTA#	**83**	GROUND	**84**	AD[09]
21	RESERVED	**22**	RESERVED	**85**	AD[08]	**86**	C/BE[0]#
23	GROUND	**24**	3.3VAUX	**87**	AD[07]	**88**	3.3V
25	CLK	**26**	RST#	**89**	3.3V	**90**	AD[06]
27	GROUND	**28**	3.3V	**91**	AD[05]	**92**	AD[04]
29	REQ#	**30**	GNT#	**93**	RESERVED	**94**	AD[02]
31	3.3V	**32**	GROUND	**95**	AD[03]	**96**	AD[00]
33	AD[31]	**34**	PME#	**97**	5V	**98**	RESERVED_WIP[5]
35	AD[29]	**36**	RESERVED	**99**	AD[01]	**100**	RESERVED_WIP[5]
37	GROUND	**38**	AD[30]	**101**	GROUND	**102**	GROUND
39	AD[27]	**40**	3.3V	**103**	AC_SYNC	**104**	M66EN
41	AD[25]	**42**	AD[28]	**105**	AC_SDATA_IN	**106**	AC_SDATA_OUT
43	RESERVED	**44**	AD[26]	**107**	AC_BIT_CLK	**108**	AC_CODEC_ID0#
45	C/BE[3]#	**46**	AD[24]	**109**	AC_CODEC_ID1#	**110**	AC_RESET#
47	AD[23]	**48**	IDSEL	**111**	MOD_AUDIO_MON	**112**	RESERVED
49	GROUND	**50**	GROUND	**113**	AUDIO_GND	**114**	GROUND
51	AD[21]	**52**	AD[22]	**115**	SYS_AUDIO_OUT	**116**	SYS_AUDIO_IN
53	AD[19]	**54**	AD[20]	**117**	SYS_AUDIO_OUT_GND	**118**	SYS_AUDIO_IN_GND
55	GROUND	**56**	PAR	**119**	AUDIO_GND	**120**	AUDIO_GND
57	AD[17]	**58**	AD[18]	**121**	RESERVED	**122**	MPCIACT#
59	C/BE[2]#	**60**	AD[16]	**123**	VCC5VA	**124**	3.3VAUX
61	IRDY#	**62**	GROUND				

APPENDIX D - MINIPCI32T3A Mictor Pin Assignments

Assignments for the A-Group Mictor connector.

Mictor Pin Number	TLA700 Channel	PCI Signal Name	PCI Pin #	Mictor Pin Number	TLA700 Channel	PCI Signal Name	PCI Pin #
3	CLK0	AC_BIT_CLK	107	36	CLK:1	DEVSEL#	72
4	A3:7	AD[31]	33	35	A1:7	AD[15]	76
5	A3:6	AD[30]	38	34	A1:6	AD[14]	75
6	A3:5	AD[29]	35	33	A1:5	AD[13]	78
7	A3:4	AD[28]	42	32	A1:4	AD[12]	79
8	A3:3	AD[27]	39	31	A1:3	AD[11]	80
9	A3:2	AD[26]	44	30	A1:2	AD[10]	81
10	A3:1	AD[25]	41	29	A1:1	AD[09]	84
11	A3:0	AD[24]	46	28	A1:0	AD[08]	85
12	A2:7	AD[23]	47	27	A0:7	AD[07]	87
13	A2:6	AD[22]	52	26	A0:6	AD[06]	90
14	A2:5	AD[21]	51	25	A0:5	AD[05]	91
15	A2:4	AD[20]	54	24	A0:4	AD[04]	92
16	A2:3	AD[19]	53	23	A0:3	AD[03]	95
17	A2:2	AD[18]	58	22	A0:2	AD[02]	94
18	A2:1	AD[17]	57	21	A0:1	AD[01]	99
19	A2:0	AD[16]	60	20	A0:0	AD[00]	96

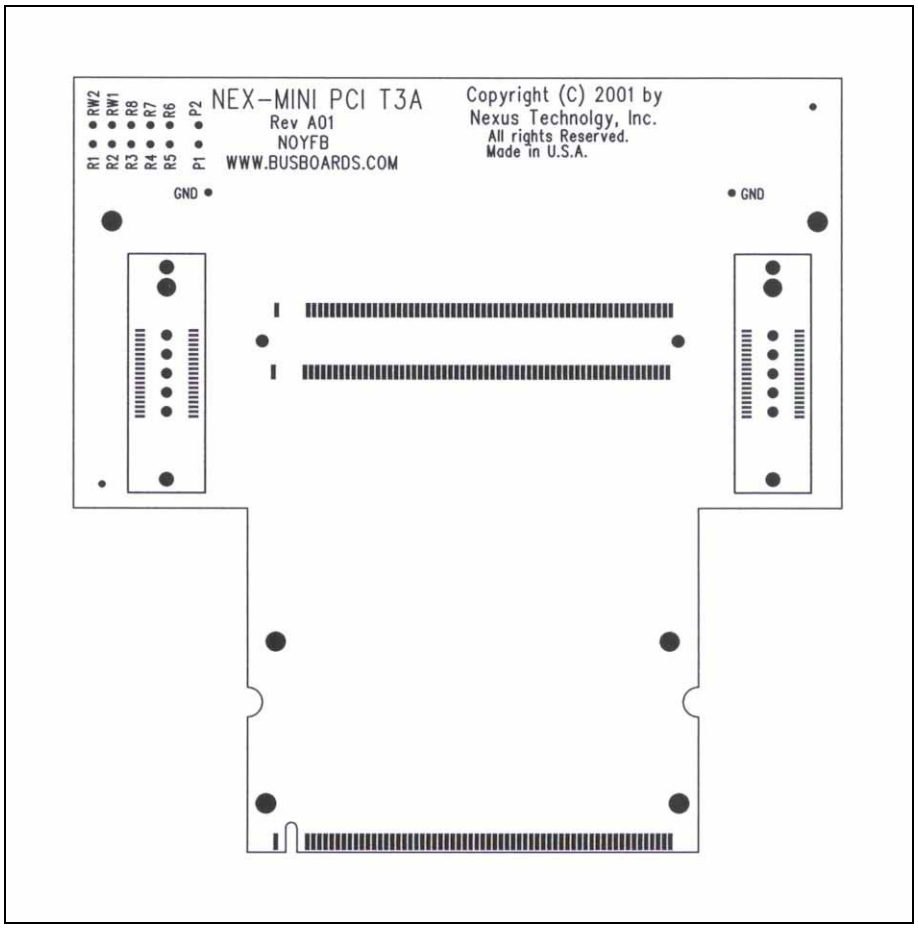
MINIPCI32T3A Mictor Pin Assignments (cont.)

Assignments for the C-Group Mictor connector

Mictor Pin Number	TLA700 Channel	PCI Signal Name	PCI Pin #	Mictor Pin Number	TLA700 Channel	PCI Signal Name	PCI Pin #
3	CLK:3	CLK	25	36	QUAL:1	RST#	26
4	C3:7	*	---	35	C1:7	M66EN	104
5	C3:6	*	---	34	C1:6	GNT#	30
6	C3:5	AC_SYNC	103	33	C1:5	REQ#	29
7	C3:4	AC_RESET#	110	32	C1:4	IDSEL	48
8	C3:3	PERR#	71	31	C1:3	MPCIACT#	122
9	C3:2	PAR	56	30	C1:2	PME#	34
10	C3:1	SERR#	67	29	C1:1	CLKRUN#	65
11	C3:0	AC_SDATA_OUT	106	28	C1:0	AC_SDATA_IN	105
12	C2:7[2]	C/BE[3]#	45	27	C0:7	unused	---
13	C2:6[2]	C/BE[2]#	59	26	C0:6	unused	---
14	C2:5[2]	C/BE[1]#	73	25	C0:5	unused	---
15	C2:4[2]	C/BE[0]#	86	24	C0:4	unused	---
16	C2:3	STOP#	68	23	C0:3	AC_CODEC_1#	109
17	C2:2	TRDY#	66	22	C0:2	AC_CODEC_0#	108
18	C2:1	IRDY#	61	21	C0:1	INTB#	17
19	C2:0	FRAME#	64	20	C0:0	INTA#	20

***Note**: These two pin assignments are not mini PCI signals. These two pins are used as general inputs from the PAD area on the NEX-MINIPCIT3A adapter.

APPENDIX E - NEX- MINIPCI32T3A Silk Screen



APPENDIX F - References

Tektronix TLA700 System User's Manual

Tektronix TLA700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

PCI Local Bus Specification
Production Version; Revision 2.1s - June 1, 1995
Published by:
PCI Special Interest Group
PO Box 14070
Portland OR 97214
800-433-5177 (U.S.)
503-797-4207 (International)
503-234-6762 (FAX)

PCI System Architecture
Third Edition
Mindshare, Inc. (Tom Shanley / Don Anderson)
Published by Addison Wesley
ISBN 0-201-40993-3

Mini PCI Specification
Revision 1.0 – October 25, 1999

APPENDIX G - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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FAX: 877-595-8118

Web site: http://**www.nexustechnology.com**

Support Contact Information

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General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.