



NEX-MPC824X

MPC824X Disassembly Software Users Manual

Including these Software Support packages:
MPC8240 MPC8245 SANDPNT

Copyright © 2008 Nexus Technology, Inc. All rights reserved.

Contents of this publication may not be reproduced in any form without the written permission of Nexus Technology, Inc.

Brand and product names used throughout this manual are the trademarks of their respective holders.

Warranty Terms and License Agreement

For warranty terms, refer to the Terms and Conditions of Sale document that was included in the product shipment. The Software License Agreement is displayed during installation. A hardcopy of that agreement may be obtained from Nexus Technology.

All Nexus Technology products to which this manual refers are subject to the Terms and Conditions of Sale document and the Software License Agreement, as appropriate.

Compliance with WEEE and RoHS Directives

This product is subject to European Union regulations on Waste Electrical and Electronics Equipment. Return to Nexus Technology for recycle at end of life. Costs associated with the return to Nexus Technology are the responsibility of the sender.

TABLE OF CONTENTS

1.0 OVERVIEW	4
1.1 General Information.....	4
2.0 SOFTWARE INSTALLATION.....	4
3.0 CONNECTING TO AN MPC824X TARGET	5
3.1 General.....	5
3.2 Motorola Sandpoint Evaluation Board	5
4.0 CLOCK SELECTION	12
4.1 General Information.....	12
4.2 Clocking Options - Explanation	12
5.0 VIEWING DATA.....	13
5.1 Viewing Timing Data on the TLA700.....	13
6.0 USING THE DISASSEMBLY SOFTWARE	13
6.1 General.....	13
6.2 Configuring the MPC-824X Disassembler.....	14
6.3 Disassembly Using the TLA700.....	15
7.0 THE MPC824X CONTROL GROUP SYMBOL TABLE	18
APPENDIX A - NEX-MPC8240 Mictor Pinout	19
APPENDIX B – NEX-MPC8240 P6860 Compression Pinouts.....	21
APPENDIX C - NEX-MPC8241/5 Mictor Pinout	24
APPENDIX D – NEX-MPC8241/5 P6860 Compression Pinouts	26
APPENDIX E - Necessary Signals for Clocking	29
APPENDIX F – Support for Simplified Mnemonics	30
APPENDIX G - Support.....	32
APPENDIX H - References.....	33

TABLE OF FIGURES

Figure 1- MPC824X MagniVu Display on TLA700.....	13
Figure 2- MPC824X Disassembly Controls	15
Figure 3- MPC824X Disassembly.....	16
Figure 4- Disassembly Display Filter Window	17

TABLE OF TABLES

Table 1- MPC8240 Generic TLA600/700 Wiring.....	7
Table 2- MPC8240 Sandpoint TLA600/700 Wiring.....	9
Table 3- MPC8241/5 TLA600/700Wiring.....	11
Table 4- NEX-824X Control Symbol Table.....	18

1.0 OVERVIEW

1.1 General Information

The NEX-824X disassembly software provides disassembly of acquired Motorola MPC824X bus cycles. The TLA acquisition module must have the appropriate state speed to acquire the MPC824X memory cycles. The state speed must be greater than or equal to the memory interface. For example the 133MHz memory bus of the MPC8245 would need a TLA acquisition module with 133MHz capability or greater. The NEX-824X support is software only. Please see Section 3.0 “Connecting to an MPC8240 Target” for information on probing.

There are two methods of connecting the TLA Logic Analyzer to the MPC824X target.

Mictor connectors can be designed onto the target and Tektronix P6434 probes are then used to connect the TLA to the target. Please refer to Appendix A or C for the required pinout information. Please refer to the “Tektronix P6434 Mass Termination Probe Instruction Manual” for mechanical information on the connector layout.

If Tektronix P6860 probes are used then a pad layout is required for interfacing the Tektronix Logic Analyzer to the MPC824X target. The required pinout can be found in Appendix B or D. Please refer to the “Tektronix P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual” for information on the mechanical pad layout.

The NEX-824X provides full instruction decoding of the PowerPC instruction set. Note that three different supports are included. One, NEX-8240, is to be used with generic MPC8240 designs. The second, NEX-SANDPNT, is to be used with the Motorola Sandpoint MPC8240 Evaluation Board. The third, the NEX8245 supports generic MPC8241 and MPC8245 designs. All versions shall be referred to as NEX-824X support except when particular distinctions need to be pointed out. In addition to the NEX-SANDPNT software, two (2) NEX-HDSWIZ signal swizzlers will be needed to properly route some 8240 signals so that data can be acquired from the Sandpoint target (see Section 3.2 for further information).

This manual assumes that the user is familiar with the Motorola MPC8240/MPC8241/MPC8245 processor specifications and the Tektronix TLA600/TLA700 Logic Analyzer. It is also expected that the user is familiar with Windows O.S. The TLA Application Software must be at V1.1 or later for the NEX-824X support to work properly.

2.0 SOFTWARE INSTALLATION

Three 3½” diskettes have been included with the NEX-824X disassembly product. Included are diskettes for generic MPC8240, MPC8241, MPC8245 support and another specifically developed for the Motorola Sandpoint (MPC8240) development board. The NEX-824X software is loaded in the same method as other Windows programs. Place the NEX-824X or NEX-SANDPNT Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the Selected support in its proper place on the hard disk.

To load MPC824X support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose either MPC824X or Sandpnt and click on **Okay**.

3.0 CONNECTING TO AN MPC824X TARGET

3.1 General

It is recommended that the user add Mictor connectors or Compression pads to their target for the interface to the TLA700 using Tektronix P6434 high-density probes or Tektronix P6860 Compression probes as we are unaware of a clip or interposer available to permit acquiring the signals directly from the micro. Table 1 shows the wiring and Channel Grouping required for NEX-8240 support.

IMPORTANT: Specific wiring must be followed when routing the MPC8240/MPC8241/MPC8245 signals to Mictor connectors if the NEX-824X support is going to be used. Appendix A and C “NEX-824X Mictor Pinout” and Appendix B and D “NEX-MPC824X P6860 Compression Pinouts” provides this information.

3.2 Motorola Sandpoint Evaluation Board

The Motorola Sandpoint evaluation board has Mictor connectors placed on it for easy access to the MPC8240 signals. However, in order for our Sandpoint support package to function properly several signals must be moved using two Nexus Technology NEX-HDSWIZ adapters. One HDSWIZ is used with the TLA’s ‘E’ Mictor cable; the second is used with the ‘C’ Mictor probe.

The Target end of the HDSWIZ is considered to be the connector that plugs into the Mictor on the Sandpoint target. The TLA end of the HDSWIZ is the connector and latch housing mounted on the larger PC board that receives the P6434 probe from the TLA.

The ‘E’ Mictor HDSWIZ must be modified as follows.

- Cut the HDSWIZ PC board traces for Pins 3 and 8

- Connect the following:

- Target pin 8 to TLA pin 3 (MIV*)

The ‘C’ Mictor HDSWIZ must be modified as follows:

- Cut the HDSWIZ PC board traces for Pins 3, 14, 18, 19, 20, and 21

- Connect the following:

- Target pin 14 to TLA pin 3 (WE*)

- Target pin 20 to TLA pin 19 (SDRAS*)

- Target pin 21 to TLA pin 18 (SDCAS*)

- Target pin 18 to TLA pin 21 (DQM4*)

- Target pin 19 to TLA pin 20 (DQM3*)

Then the TLA P6434s should be connected to the Sandpoint board as follows:

TLA 'A' Group Mictor to J7

TLA 'D' Group Mictor to J10

TLA 'E' Group Mictor to J9 (via Group E HDSWIZ)

TLA 'C' Group Mictor to J6 (via the Group C HDSWIZ)

Group Name	MPC8240 Signal Name	TLA700 input	Group Name	MPC8240 Signal Name	TLA700 input
HiData (Hex)	DH0	D3:7	LoData (Hex)	DL0	A3:7
	DH1	D3:6		DL1	A3:6
	DH2	D3:5		DL2	A3:5
	DH3	D3:4		DL3	A3:4
	DH4	D3:3		DL4	A3:3
	DH5	D3:2		DL5	A3:2
	DH6	D3:1		DL6	A3:1
	DH7	D3:0		DL7	A3:0
	DH8	D2:7		DL8	A2:7
	DH9	D2:6		DL9	A2:6
	DH10	D2:5		DL10	A2:5
	DH11	D2:4		DL11	A2:4
	DH12	D2:3		DL12	A2:3
	DH13	D2:2		DL13	A2:2
	DH14	D2:1		DL14	A2:1
	DH15	D2:0		DL15	A2:0
	DH16	D1:7		DL16	A1:7
	DH17	D1:6		DL17	A1:6
	DH18	D1:5		DL18	A1:5
	DH19	D1:4		DL19	A1:4
	DH20	D1:3		DL20	A1:3
	DH21	D1:2		DL21	A1:2
	DH22	D1:1		DL22	A1:1
	DH23	D1:0		DL23	A1:0
	DH24	D0:7		DL24	A0:7
	DH25	D0:6		DL25	A0:6
	DH26	D0:5		DL26	A0:5
	DH27	D0:4		DL27	A0:4
	DH28	D0:3		DL28	A0:3
	DH29	D0:2		DL29	A0:2
	DH30	D0:1		DL30	A0:1
	DH31	D0:0		DL31	A0:0
DRAMAddr (Hex)	SDBA0	E3:5	Control (Sym)	WE*	C2:1
	SDMA12	E3:4		SDRAS*	C2:3
	SDMA11	E3:3		SDCAS*	C2:2
	SDMA10	E3:2		MIV*	C2:0
	SDMA9	E3:1		MAA0	C2:4
	SDMA8	E3:0		MAA1	C2:5
	SDMA7	E2:7		MAA2	C2:6
	SDMA6	E2:6			
	SDMA5	E2:5			
	SDMA4	E2:4			
	SDMA3	E2:3			
	SDMA2	E2:2			
	SDMA1	E2:1			
SDMA0	E2:0				

Table 1- MPC8240 Generic TLA600/700 Wiring

Note: All signals in this table are required for disassembly

DebugAdd (Hex)	QACK*/DA0	C0:0	RAS_CS (Bin)	RAS/CS7*	C2:7
	CKO/DA1	C0:1		RAS/CS6*	CK2
	DA2	C0:2		RAS/CS5*	CK0
	PCI_CLK4/DA3	C0:3		RAS/CS4*	CK1
	REQ4*/DA4	C0:4		RAS/CS3*	Q3
	GNT4*/DA5	C0:5		RAS/CS2*	Q2
	PLL_CFG4/DA6	C0:6		RAS/CS1*	Q1
	PLL_CFG3/DA7	C0:7		RAS/CS0*	Q0
	PLL_CFG2/DA8	C1:0	CAS_DQM (Bin)	CAS/DQM7* ¹	C3:7
	PLL_CFG1/DA9	C1:1		CAS/DQM6* ¹	C3:6
	PLL_CFG0/DA10	C1:2		CAS/DQM5* ¹	C3:5
	DA11	C1:3		CAS/DQM4* ¹	C3:4
	DA12	C1:4		CAS/DQM3* ¹	C3:3
	DA13	C1:5		CAS/DQM2* ¹	C3:2
	DA14	C1:6		CAS/DQM1* ¹	C3:1
	DA15	C1:7	CAS/DQM0* ¹	C3:0	
				ROMFlash (Bin)	RCS1*
				RCS0*	E3:6
			Ungrouped	SDRAM_CLK ¹	CK3

Table 1 (cont'd.) – MPC8240 Generic TLA600/700 Wiring

Note: 1) Signal required for disassembly

Group Name	Sandpoint Signal Name	TLA700 input	Group Name	Sandpoint Signal Name	TLA700 input
HiData (Hex)	D0	D3:7	LoData (Hex)	D32	A3:7
	D1	D3:6		D33	A3:6
	D2	D3:5		D34	A3:5
	D3	D3:4		D35	A3:4
	D4	D3:3		D36	A3:3
	D5	D3:2		D37	A3:2
	D6	D3:1		D38	A3:1
	D7	D3:0		D39	A3:0
	D8	D2:7		D40	A2:7
	D9	D2:6		D41	A2:6
	D10	D2:5		D42	A2:5
	D11	D2:4		D43	A2:4
	D12	D2:3		D44	A2:3
	D13	D2:2		D45	A2:2
	D14	D2:1		D46	A2:1
	D15	D2:0		D47	A2:0
	D16	D1:7		D48	A1:7
	D17	D1:6		D49	A1:6
	D18	D1:5		D50	A1:5
	D19	D1:4		D51	A1:4
	D20	D1:3		D52	A1:3
	D21	D1:2		D53	A1:2
	D22	D1:1		D54	A1:1
	D23	D1:0		D55	A1:0
	D24	D0:7		D56	A0:7
	D25	D0:6		D57	A0:6
	D26	D0:5		D58	A0:5
	D27	D0:4		D59	A0:4
	D28	D0:3		D60	A0:3
	D29	D0:2		D61	A0:2
	D30	D0:1		D62	A0:1
	D31	D0:0		D63	A0:0
DRAMAddr (Hex)	MA10	E1:2	Control (Sym)	WE*	CK3
	MA9	E1:1		SDRAS*	C2:0
	MA8	E1:0		SDCAS*	C2:1
	MA7	E0:7		MIV*	Q3
	MA6	E0:6		MAA0	E3:6
	MA5	E0:5		MAA1	E3:5
	MA4	E0:4		MAA2	E3:4
	MA3	E0:3			
	MA2	E0:2			
	MA1	E0:1			
MA0	E0:0				

Table 2- MPC8240 Sandpoint TLA600/700 Wiring

Note: All signals in this table are required for disassembly

Group Name	Sandpoint Signal Name	TLA700 input	Group Name	Sandpoint Signal Name	TLA700 input	
DebugAdd (Hex)	DA0	E3:2	RAS_CS (Bin)	CS7*	C1:1	
	DA1	E3:1		CS6*	C1:0	
	DA2	E3:0		CS5*	C0:7	
	DA3	E2:7		CS4*	C0:6	
	DA4	E2:6		CS3*	C0:5	
	KPLL0	E2:5		CS2*	C0:4	
	KPLL1	E2:4		CS1*	C0:3	
	KPLL2	E2:3		CS0*	C0:2	
	KPLL3	E2:2		CAS_DQM (Bin)	DQM7* ¹	C2:4
	KPLL4	E2:1			DQM6* ¹	C2:3
	REQ_XGNT4*	E2:0			DQM5* ¹	C2:2
	GNT_XREQ4*	E1:7			DQM4* ¹	C0:1
	PCICLK4	E1:6			DQM3* ¹	C0:0
	DA13	E1:5	DQM2* ¹		C1:7	
	CKO	E1:4	DQM1* ¹		C1:6	
	QACK*	E1:3	DQM0* ¹	C1:5		
	MA8	E1:0	ROMFlash (Bin)	RCS1*	C1:3	
	MA7	E0:7		RCS0*	C1:2	
	MA6	E0:6	Ungrouped	TESTCLK ¹	CK1	
	MA5	E0:5				
	MA4	E0:4				
	MA3	E0:3				
	MA2	E0:2				
	MA1	E0:1				
	MA0	E0:0				
	DebugAddr2	C3:7				
	DebugAddr1	C3:6				
DebugAddr0	C3:5					

Table 2 (cont'd. – MPC8240 Sandpoint TLA600/700 Wiring)

Note: 1) Signal required for disassembly

Group Name	MPC8241/5 Signal Name	TLA700 input	Group Name	MPC8241/5 Signal Name	TLA700 input
HiData (Hex)	DH0	D3:7	LoData (Hex)	DL0	A3:7
	DH1	D3:6		DL1	A3:6
	DH2	D3:5		DL2	A3:5
	DH3	D3:4		DL3	A3:4
	DH4	D3:3		DL4	A3:3
	DH5	D3:2		DL5	A3:2
	DH6	D3:1		DL6	A3:1
	DH7	D3:0		DL7	A3:0
	DH8	D2:7		DL8	A2:7
	DH9	D2:6		DL9	A2:6
	DH10	D2:5		DL10	A2:5
	DH11	D2:4		DL11	A2:4
	DH12	D2:3		DL12	A2:3
	DH13	D2:2		DL13	A2:2
	DH14	D2:1		DL14	A2:1
	DH15	D2:0		DL15	A2:0
	DH16	D1:7		DL16	A1:7
	DH17	D1:6		DL17	A1:6
	DH18	D1:5		DL18	A1:5
	DH19	D1:4		DL19	A1:4
	DH20	D1:3		DL20	A1:3
	DH21	D1:2		DL21	A1:2
	DH22	D1:1		DL22	A1:1
	DH23	D1:0		DL23	A1:0
	DH24	D0:7		DL24	A0:7
	DH25	D0:6		DL25	A0:6
	DH26	D0:5		DL26	A0:5
	DH27	D0:4		DL27	A0:4
	DH28	D0:3		DL28	A0:3
	DH29	D0:2		DL29	A0:2
	DH30	D0:1		DL30	A0:1
	DH31	D0:0		DL31	A0:0
DRAMAddr (Hex)	SDBA1	E1:7	Control (Sym)	WE*	C2:1
	SDBA0	E1:6		SDRAS*	C2:3
	SDMA14	E3:6		SDCAS*	C2:2
	SDMA13	E3:5		MIV*	C2:0
	SDMA12	E3:4		MAA0	C2:4
	SDMA11	E3:3		MAA1	C2:5
	SDMA10	E3:2	MAA2	C2:6	
	SDMA9	E3:1	ROMFlash (Bin)	RCS3*	E1:3
	SDMA8	E3:0		RCS2*	E1:4
	SDMA7	E2:7		RCS1*	E1:5
	SDMA6	E2:6		RCS0*	E3:7
	SDMA5	E2:5			
	SDMA4	E2:4			
	SDMA3	E2:3			
	SDMA2	E2:2			
	SDMA1	E2:1			
	SDMA0	E2:0			

Table 3- MPC8241/5 TLA600/700Wiring

Note: All signals in this table are required for disassembly

DebugAdd (Hex)	QACK*/DA0	C0:0	RAS_CS (Bin)	RAS/CS7*	C2:7	
	CKO/DA1	C0:1		RAS/CS6*	CK2	
	DA2	C0:2		RAS/CS5*	CK0	
	PCI_CLK4/DA3	C0:3		RAS/CS4*	CK1	
	REQ4*/DA4	C0:4		RAS/CS3*	Q3	
	GNT4*/DA5	C0:5		RAS/CS2*	Q2	
	PLL_CFG4/DA6	C0:6		RAS/CS1*	Q1	
	PLL_CFG3/DA7	C0:7		RAS/CS0*	Q0	
	PLL_CFG2/DA8	C1:0		CAS_DQM (Bin)	CAS/DQM7* ¹	C3:7
	PLL_CFG1/DA9	C1:1			CAS/DQM6* ¹	C3:6
	PLL_CFG0/DA10	C1:2	CAS/DQM5* ¹		C3:5	
	DA11	C1:3	CAS/DQM4* ¹		C3:4	
	DA12	C1:4	CAS/DQM3* ¹		C3:3	
	DA13	C1:5	CAS/DQM2* ¹		C3:2	
	DA14	C1:6	CAS/DQM1* ¹		C3:1	
	DA15	C1:7	CAS/DQM0* ¹	C3:0		
		Ungrouped	SDRAM_CLK ¹	CK3		

Table 3 (cont'd.) – MPC8241/5 TLA600/700 Wiring

Note: 1) Signal required for disassembly

4.0 CLOCK SELECTION

4.1 General Information

There are two clocking selections available when using the NEX-824X support package. Each is explained in detail below.

The clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (the button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

4.2 Clocking Options - Explanation

Bus Cycles - This is the default clocking selection. In this mode the software monitors the CLK, SDRAS*, SDCAS*, and MIV* signals to permit the acquisition of MPC824X bus cycle activity. All Wait and Idle states will be ignored, offering the best use of acquisition memory. Refer to Appendix B for more information on how bus cycle data is acquired.

Rising Edge of CLK - In this mode, data will be acquired on every rising edge of the CLK signal. The disassembly software will try to filter and display these cycles accordingly, but incorrect decoding may

occur because of the numerous duplicated cycles. This clocking mode shows all bus cycles, including any Wait or Idle states. Since no clocking qualification is done only the CLK signal is needed.

5.0 VIEWING DATA

5.1 Viewing Timing Data on the TLA700

By default, the TLA700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: MPC824X and MPC824X-MagniVu. The first will show the same data (from the same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, MPC824X-MagniVu, will show all of the channels in 2GHz/8GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA700 System User's Manual for additional information on formatting the Waveform display.

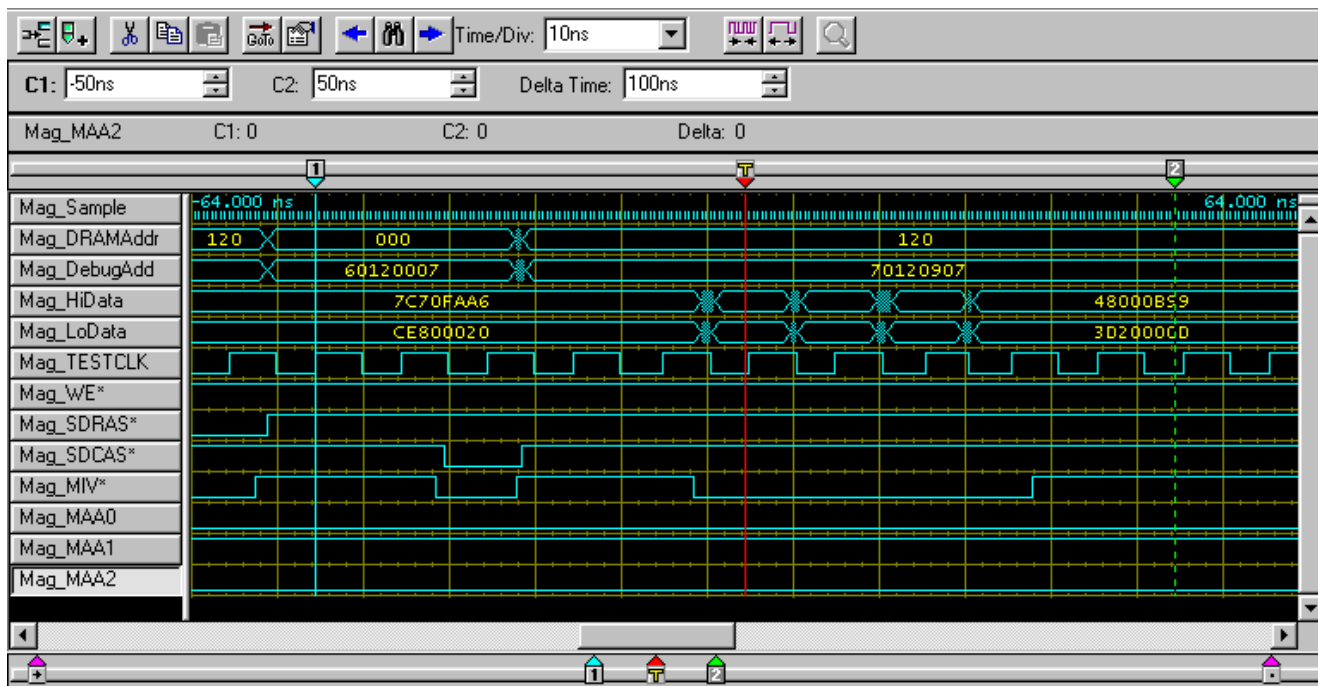


Figure 1- MPC824X MagniVu Display on TLA700

6.0 USING THE DISASSEMBLY SOFTWARE

6.1 General

The NEX-824X support software acquires and decodes Motorola MPC824X bus activity and displays the information as assembly language mnemonics (machine code) - see Figure 3. This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types of

interest to the software engineer (Figure 4). The user can choose to display the acquired data in Hardware, Software, Control Flow, or Subroutine modes.

A major feature of the NEX-824X software is its ability to intelligently acquire bus cycle information. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the support software is able to acquire only the valid MPC824X bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more microprocessor bus cycles. For debug purposes the user also has the ability to override this function and acquire data on every Rising CLK Edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 4.2 Clocking Options for further information.)

Every stored cycle (bus or clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps/125ps in the TLA600/700 series, permits precise measurements of microprocessor bus activity. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

6.2 Configuring the MPC-824X Disassembler

Because of the complexity and flexibility of the MPC824X micro it is necessary to properly configure the support so the disassembler can process the data and display it accurately. The configuration menu can be accessed by moving to an MPC824X List window, clicking on the display with the right mouse button, selecting **Properties** then left-clicking on the **Disassembly** tab. The menu shown in Figure 2 will then be displayed. Note the control box (named either "Sandpnt Controls" or "MPC824X Controls") that contains 5 select fields labeled Suppress SDRAM cycles, Instruction Order, Number of Row Bits, Number of Column Bits, and Mnemonics. Each select field is described in detail as follows:

Suppress SDRAM Cycles – This field permits Displaying (the default) or Suppressing the display of the Row and Column address cycles. If Suppress is selected then any Row or Column address cycle that does not have valid data associated with it will be hidden from view.

Instruction Order – By default the instructions will be processed with the HiData information disassembled first followed by the LoData. A select option is available to swap these resulting in LoData being disassembled first followed by the HiData.

Number of Row Bits – This field allows setting of the number of Row bits used by the memory interface. Default is 13, with selections for 12, 11, and 10 bits. This field must be properly set for the physical address reconstruction to be accurate.

Number of Column Bits – This field allows setting of the number of Column bits used by the memory interface. Default is 10, with selections for 9, 8, and 7 bits. This field must be properly set for the physical address reconstruction to be accurate.

Mnemonics – This field allows the user to choose to view the disassembled instructions as Book E mnemonics or Simplified mnemonics. See Appendix C for further information.

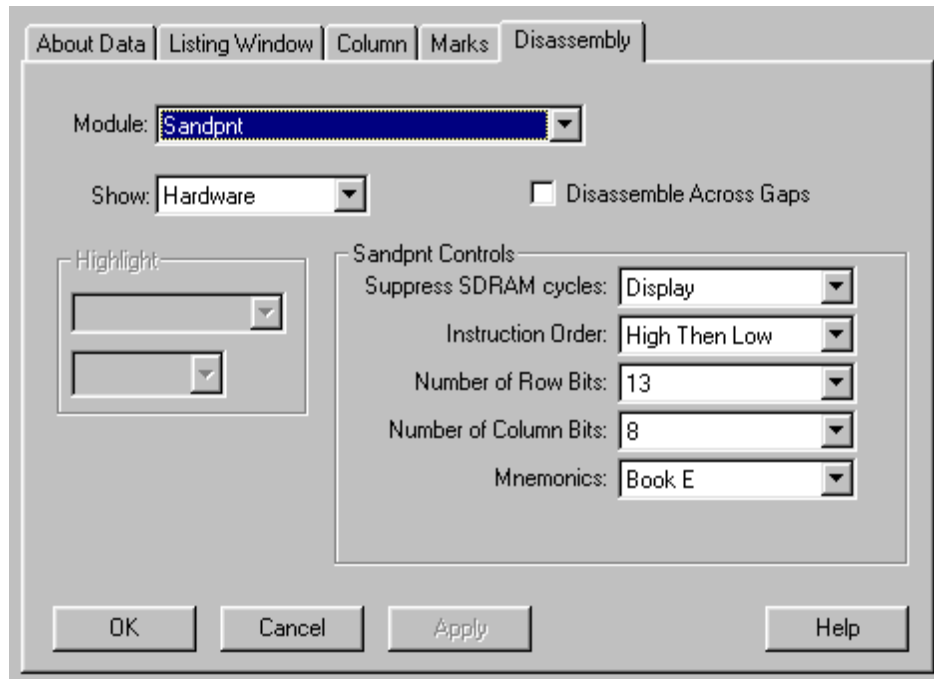


Figure 2- MPC824X Disassembly Controls

6.3 Disassembly Using the TLA700

The TLA700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified

can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the **From** window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

Sample	Sandpnt DebugAdd	Sandpnt DRAMAddr	Sandpnt HiData	Sandpnt LoData	Sandpnt Mnemonics	Timestamp
3924	-----	078	00031057	80000000	{ CAS INST }	30.000 ns
3925	00004BC0	009	7C5143A6	-----	mtspr 0x228,r2	30.500 ns
	00004BC4	009	-----	7C5242A6	mfspr r2,0x248	
3926	00004BC0	009	7C7342A6	-----	mfspr r3,0x268	10.000 ns
	00004BC4	009	-----	4C000064	rfi	
3927	00004BC0	009	7C6000A6	-----	mtmsr r3	10.000 ns
	00004BC4	009	-----	4E800020	b1r 20,0	
3928	00004BC0	009	7C70FAA6	-----	mfdbatl r3,3	10.500 ns
	00004BC4	009	-----	4E800020	b1r 20,0	
3929	-----	120	7C70FAA6	CE800020	{ RAS }	111.000 ns
3930	-----	000	7C70FAA6	CE800020	{ CAS INST }	30.000 ns
3931	00090000	120	9421FFE8	-----	stwu r1,0xFFE8(r1)	30.500 ns
	00090004	120	-----	7C0802A6	mrsprg0 r0	
3932	00090000	120	93E10014	-----	stwu r31,0x0014(r1)	10.000 ns
	00090004	120	-----	9001001C	stwu r0,0x001C(r1)	
3933	00090000	120	7C3F0B78	-----	mrr r31,r1	10.500 ns
	00090004	120	-----	48000EA1	b1 0x0003A8	
3934	00090000	120	48000B99	-----	b1 0x0002E6	10.000 ns
	00090004	120	-----	3D20000D	lis r9,0x000D	
3935	-----	11F	0008FFD8	0008FFD8	{ RAS }	90.500 ns
3936	0008FFC0	0F8	-----	0008FFD8	{ CAS/WRITE }	30.500 ns
3937	0008FFD0	0FA	0008FFD8	-----	{ CAS/WRITE }	70.500 ns
3938	0008FFD8	0FB	0009001C	-----	{ CAS/WRITE }	71.000 ns
3939	-----	121	0D030000	F6001C00	{ RAS }	91.000 ns
3940	-----	0D6	0D030000	F6001C00	{ CAS INST }	30.000 ns
3941	00090EB0	121	4E800020	-----	b1r 20,0	30.500 ns
	00090EB4	121	-----	3C808000	lis r4,0x8000	
3942	00090EB0	121	6084002A	-----	ori r4,r4,0x002A	10.000 ns
	00090EB4	121	-----	3C608000	lis r3,0x8000	
3943	00090EB0	121	800B0004	-----	lwz r0,0x0004(r11)	10.000 ns
	00090EB4	121	-----	7C0803A6	mtsprg0 r0	
3944	00090EB0	121	83EBFFFC	-----	lwz r31,0xFFFC(r11)	10.500 ns
	00090EB4	121	-----	7D615B78	mrr r1,r11	
3945	-----	0D8	83EBFFFC	FD615B78	{ CAS INST }	70.500 ns
3946	00090EC0	121	60631FFF	-----	ori r3,r3,0x1FFF	30.000 ns
	00090FC4	121	-----	4C00012C	lsync	

Figure 3- MPC824X Disassembly

The other column of interest is the Mnemonics column, where the MPC824X disassembly information is displayed. As mentioned previously, it is possible to filter the MPC824X instructions that are displayed. This is done via selections made in the Disassembly tab of the Properties window (see Figure 4). By default the display is in Hardware mode, where all bus cycles are displayed (Memory Reads, Memory Writes, Instructions, etc.). Other choices are: Software (only executed instructions are displayed), Control Flow (display of instructions affecting code flow such as Jumps, Branches, etc.), and Subroutine (only instructions such as Calls, Returns, etc. are displayed).

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

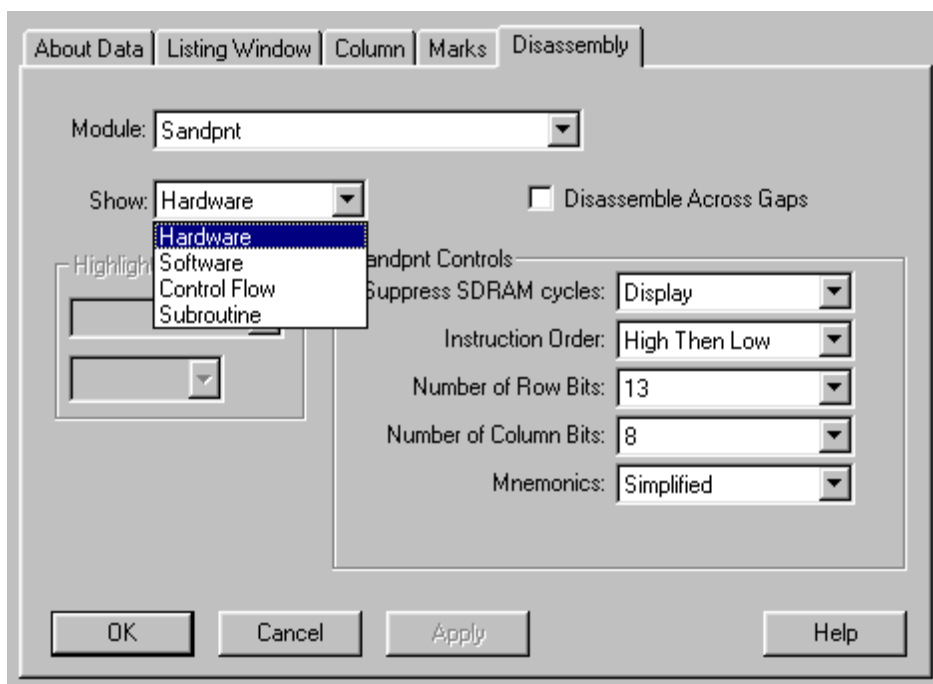


Figure 4- Disassembly Display Filter Window

7.0 THE MPC824X CONTROL GROUP SYMBOL TABLE

The use of Symbol Tables when displaying state data and defining a trigger enables the user to quickly determine the type of bus cycle that occurred or is desired. A symbol table for the Control group for both the NEX-824X (MPC824X_Ctrl) and NEX-SANDPNT (SANDPNT_Ctrl) is given in Table 3. The symbols quickly show the type of bus transaction acquired when viewing data in Listing display. This same symbol table can be used in the Trigger area of the TLA to easily define the sort of bus cycle that is to be triggered on.

Pattern	TLA700 Symbols	Meaning
x 01 0 xxx	RAS_CYCLE	Row Address cycle
1 10 0 000	CAS_CYCLE_FOR_PROC_DATA_READ	Column Address cycle for processor Data Read
1 11 0 000	PROC_DATA_READ	Processor Data Read
1 10 0 001	CAS_CYCLE_FOR_PROC_TOUCH_LOAD	Column Address cycle for Processor Touch Load
1 11 0 001	PROC_TOUCH_LOAD	Processor Touch Load
1 10 0 010	CAS_CYCLE_FOR_PROC_INST_FETCH	Column Address cycle for Processor Instruction Fetch
1 11 0 010	PROC_INST_FETCH	Processor Instruction Fetch
1 1x 0 011	RESERVED	Reserved
1 1x 0 100	PCI_MEM_READ	¹ PCI Memory Read
1 1x 0 101	DMA0_MEM_READ	DMA channel 0 Memory Read
1 1x 0 110	DMA1_MEM_READ	DMA channel 1 Memory Read
1 1x 0 111	I2O_MEM_READ	¹ I ² O Memory Read
0 10 0 000	CAS_CYCLE_&_PROC_DATA_WRITE	Column Address cycle and Processor Data Write
0 11 0 000	PROC_DATA_WRITE	Processor Data Write
0 1x 0 001	RESERVED	Reserved
0 1x 0 010	RESERVED	Reserved
0 1x 0 011	RESERVED	Reserved
0 1x 0 100	PCI_MEM_WRITE	¹ PCI Memory Write
0 1x 0 101	DMA0_MEM_WRITE	DMA channel 0 Memory Write
0 1x 0 110	DMA1_MEM_WRITE	DMA channel 1 Memory Write
0 1x 0 111	I2O_MEM_WRITE	¹ I ² O Memory Write

Table 4- NEX-824X Control Symbol Table

Signals, from left to right: WE* SDRAS* SDCAS* MIV* MAA0 MAA1 MAA2

Note: 1) Although triggering on these cycles is possible no valid data can be displayed because it is not present on pins monitored by the NEX-824X support

APPENDIX A - NEX-MPC8240 Mictor Pinout

NOTES: The pin numbers are given for the 352-pin Tape Ball Grid Array (TBGA) package. Blank entries in the MPC8240 Pin # and Signal columns denote unused TLA inputs that can be wired to any user signal.

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	CK0	RAS_CS5*	L2	36	6	CK1	RAS_CS4*	M2
4	7	A3:7	DL0 ¹	AD17	35	8	A1:7	DL16 ¹	B1
5	9	A3:6	DL1 ¹	AE17	34	10	A1:6	DL17 ¹	A1
6	11	A3:5	DL2 ¹	AE15	33	12	A1:5	DL18 ¹	A3
7	13	A3:4	DL3 ¹	AF15	32	14	A1:4	DL19 ¹	A4
8	15	A3:3	DL4 ¹	AC14	31	16	A1:3	DL20 ¹	A5
9	17	A3:2	DL5 ¹	AE13	30	18	A1:2	DL21 ¹	A6
10	19	A3:1	DL6 ¹	AF13	29	20	A1:1	DL22 ¹	A7
11	21	A3:0	DL7 ¹	AF12	28	22	A1:0	DL23 ¹	D7
12	23	A2:7	DL8 ¹	AF11	27	24	A0:7	DL24 ¹	A8
13	25	A2:6	DL9 ¹	AF10	26	26	A0:6	DL25 ¹	B8
14	27	A2:5	DL10 ¹	AF9	25	28	A0:5	DL26 ¹	A10
15	29	A2:4	DL11 ¹	AD8	24	30	A0:4	DL27 ¹	D10
16	31	A2:3	DL12 ¹	AF8	23	32	A0:3	DL28 ¹	A12
17	33	A2:2	DL13 ¹	AF7	22	34	A0:2	DL29 ¹	B11
18	35	A2:1	DL14 ¹	AF6	21	36	A0:1	DL30 ¹	B12
19	37	A2:0	DL15 ¹	AE5	20	38	A0:0	DL31 ¹	A14

A-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	Q0	RAS_CS0*	Y4	36	6	CK2	RAS_CS6*	M1
4	7	D3:7	DH0 ¹	AC17	35	8	D1:7	DH16 ¹	E4
5	9	D3:6	DH1 ¹	AF16	34	10	D1:6	DH17 ¹	A2
6	11	D3:5	DH2 ¹	AE16	33	12	D1:5	DH18 ¹	B3
7	13	D3:4	DH3 ¹	AE14	32	14	D1:4	DH19 ¹	D4
8	15	D3:3	DH4 ¹	AF14	31	16	D1:3	DH20 ¹	B4
9	17	D3:2	DH5 ¹	AC13	30	18	D1:2	DH21 ¹	B5
10	19	D3:1	DH6 ¹	AE12	29	20	D1:1	DH22 ¹	D6
11	21	D3:0	DH7 ¹	AE11	28	22	D1:0	DH23 ¹	C6
12	23	D2:7	DH8 ¹	AE10	27	24	D0:7	DH24 ¹	B7
13	25	D2:6	DH9 ¹	AE9	26	26	D0:6	DH25 ¹	C9
14	27	D2:5	DH10 ¹	AE8	25	28	D0:5	DH26 ¹	A9
15	29	D2:4	DH11 ¹	AC7	24	30	D0:4	DH27 ¹	B10
16	31	D2:3	DH12 ¹	AE7	23	32	D0:3	DH28 ¹	A11
17	33	D2:2	DH13 ¹	AE6	22	34	D0:2	DH29 ¹	A13
18	35	D2:1	DH14 ¹	AF5	21	36	D0:1	DH30 ¹	B13
19	37	D2:0	DH15 ¹	AC5	20	38	D0:0	DH31 ¹	A15

D-Group Mictor connector

Notes:

- 1) Signal required for disassembly

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	Q3	RAS_CS3*	AC4	36	6	Q2	RAS_CS2*	AA4
4	7	E3:7	RCS1*	N2	35	8	E1:7	unused	
5	9	E3:6	RCS0*	N4	34	10	E1:6	unused	
6	11	E3:5	SDBA0 ¹	P2	33	12	E1:5	do not use	-----
7	13	E3:4	SDMA12/SDBA1 ¹	P1	32	14	E1:4	do not use	-----
8	15	E3:3	SDMA11 ¹	N1	31	16	E1:3	do not use	-----
9	17	E3:2	SDMA10 ¹	R1	30	18	E1:2	do not use	-----
10	19	E3:1	SDMA9 ¹	R2	29	20	E1:1	do not use	-----
11	21	E3:0	SDMA8 ¹	T1	28	22	E1:0	do not use	-----
12	23	E2:7	SDMA7 ¹	T2	27	24	E0:7	do not use	-----
13	25	E2:6	SDMA6 ¹	U4	26	26	E0:6	do not use	-----
14	27	E2:5	SDMA5 ¹	U2	25	28	E0:5	do not use	-----
15	29	E2:4	SDMA4 ¹	U1	24	30	E0:4	do not use	-----
16	31	E2:3	SDMA3 ¹	V1	23	32	E0:3	do not use	-----
17	33	E2:2	SDMA2 ¹	V3	22	34	E0:2	do not use	-----
18	35	E2:1	SDMA1 ¹	W1	21	36	E0:1	do not use	-----
19	37	E2:0	SDMA0 ¹	W2	20	38	E0:0	do not use	-----

E-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 Channel	MPC8240 Signal Name	MPC8240 Pin #
3	5	CK3	SDRAM_CLK ²	see Note 1	36	6	Q1	RAS_CS1*	AA3
4	7	C3:7	CAS/DQM7 ¹	J1	35	8	C1:7	DA15 ³	J2
5	9	C3:6	CAS/DQM6 ¹	K1	34	10	C1:6	DA14 ³	F1
6	11	C3:5	CAS/DQM5 ¹	AC2	33	12	C1:5	DA13 ³	AF19
7	13	C3:4	CAS/DQM4 ¹	AC1	32	14	C1:4	DA12 ³	AF17
8	15	C3:3	CAS/DQM3 ¹	K2	31	16	C1:3	DA11 ³	AD26
9	17	C3:2	CAS/DQM2 ¹	K3	30	18	C1:2	PLL0/DA10 ³	A22
10	19	C3:1	CAS/DQM1 ¹	AB2	29	20	C1:1	PLL1/DA9 ³	B19
11	21	C3:0	CAS/DQM0 ¹	AB1	28	22	C1:0	PLL2/DA8 ³	A21
12	23	C2:7	RAS_CS7*	L1	27	24	C0:7	PLL3/DA7 ³	B18
13	25	C2:6	MAA2 ¹	AE1	26	26	C0:6	PLL4/DA6 ³	B17
14	27	C2:5	MAA1 ¹	AF1	25	28	C0:5	GNT4*/DA5 ³	W26
15	29	C2:4	MAA0 ¹	AF2	24	30	C0:4	REQ4*/DA4 ³	Y26
16	31	C2:3	SDRAS* ¹	AD1	23	32	C0:3	PCICLK4/DA3 ³	AF26
17	33	C2:2	SDCAS* ¹	AD2	22	34	C0:2	DA2 ³	C25
18	35	C2:1	WE* ¹	AA1	21	36	C0:1	CKO/DA1 ³	B15
19	37	C2:0	MIV* ¹	A16	20	38	C0:0	QACK*/D0 ³	F2

C-Group Mictor connector

Notes:

- 1) Signal required for disassembly
- 2) Any active SDRAM clock signal can be used.
- 3) These signals are used for Debug Address support.

APPENDIX B – NEX-MPC8240 P6860 Compression Pinouts

For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	CK2-	Gnd	Gnd
A13	CK2+	RAS_CS6*	M1
B12	D1:7	DH16 ¹	E4
B10	D1:6	DH17 ¹	A2
A12	D1:5	DH18 ¹	B3
A10	D1:4	DH19 ¹	D4
B9	D1:3	DH20 ¹	B4
B7	D1:2	DH21 ¹	B5
A9	D1:1	DH22 ¹	D6
A7	D1:0	DH23 ¹	C6
B6	D0:7	DH24 ¹	B7
B4	D0:6	DH25 ¹	C9
A6	D0:5	DH26 ¹	A9
A4	D0:4	DH27 ¹	B10
B3	D0:3	DH28 ¹	A11
B1	D0:2	DH29 ¹	A13
A3	D0:1	DH30 ¹	B13
A1	D0:0	DH31 ¹	A15

Probe Connection D0/D1

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	CK1-	Gnd	Gnd
A13	CK1+	RAS_CS4*	M2
B12	A1:7	DL16 ¹	B1
B10	A1:6	DL17 ¹	A1
A12	A1:5	DL18 ¹	A3
A10	A1:4	DL19 ¹	A4
B9	A1:3	DL20 ¹	A5
B7	A1:2	DL21 ¹	A6
A9	A1:1	DL22 ¹	A7
A7	A1:0	DL23 ¹	D7
B6	A0:7	DL24 ¹	A8
B4	A0:6	DL25 ¹	B8
A6	A0:5	DL26 ¹	A10
A4	A0:4	DL27 ¹	D10
B3	A0:3	DL28 ¹	A12
B1	A0:2	DL29 ¹	B11
A3	A0:1	DL30 ¹	B12
A1	A0:0	DL31 ¹	A14

Probe A0/A1

Notes:

- 1) Signal required for disassembly
- 2) Any active SDRAM clock signal can be used.
- 3) These signals are used for Debug Address support.

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	Q0-	Gnd	Gnd
A13	Q0+	RAS_CS0*	Y4
B12	D3:7	DH0 ¹	AC17
B10	D3:6	DH1 ¹	AF16
A12	D3:5	DH2 ¹	AE16
A10	D3:4	DH3 ¹	AE14
B9	D3:3	DH4 ¹	AF14
B7	D3:2	DH5 ¹	AC13
A9	D3:1	DH6 ¹	AE12
A7	D3:0	DH7 ¹	AE11
B6	D2:7	DH8 ¹	AE10
B4	D2:6	DH9 ¹	AE9
A6	D2:5	DH10 ¹	AE8
A4	D2:4	DH11 ¹	AC7
B3	D2:3	DH12 ¹	AE7
B1	D2:2	DH13 ¹	AE6
A3	D2:1	DH14 ¹	AF5
A1	D2:0	DH15 ¹	AC5

Probe Connection D2/D3

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	CK0-	Gnd	Gnd
A13	CK0+	RAS_CS5*	L2
B12	A3:7	DL0 ¹	AD17
B10	A3:6	DL1 ¹	AE17
A12	A3:5	DL2 ¹	AE15
A10	A3:4	DL3 ¹	AF15
B9	A3:3	DL4 ¹	AC14
B7	A3:2	DL5 ¹	AE13
A9	A3:1	DL6 ¹	AF13
A7	A3:0	DL7 ¹	AF12
B6	A2:7	DL8 ¹	AF11
B4	A2:6	DL9 ¹	AF10
A6	A2:5	DL10 ¹	AF9
A4	A2:4	DL11 ¹	AD8
B3	A2:3	DL12 ¹	AF8
B1	A2:2	DL13 ¹	AF7
A3	A2:1	DL14 ¹	AF6
A1	A2:0	DL15 ¹	AE5

Probe A2/A3

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	Q2-	Gnd	Gnd
A13	Q2+	RAS_CS2*	AA4
B12	E1:7	unused	
B10	E1:6	unused	
A12	E1:5	do not use	-----
A10	E1:4	do not use	-----
B9	E1:3	do not use	-----
B7	E1:2	do not use	-----
A9	E1:1	do not use	-----
A7	E1:0	do not use	-----
B6	E0:7	do not use	-----
B4	E0:6	do not use	-----
A6	E0:5	do not use	-----
A4	E0:4	do not use	-----
B3	E0:3	do not use	-----
B1	E0:2	do not use	-----
A3	E0:1	do not use	-----
A1	E0:0	do not use	-----

Probe Connection E0/E1

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	Q3-	Gnd	Gnd
A13	Q3+	RAS_CS3*	AC4
B12	E3:7	RCS1*	N2
B10	E3:6	RCS0*	N4
A12	E3:5	SDBA0 ¹	P2
A10	E3:4	SDMA12/SDBA1 ¹	P1
B9	E3:3	SDMA11 ¹	N1
B7	E3:2	SDMA10 ¹	R1
A9	E3:1	SDMA9 ¹	R2
A7	E3:0	SDMA8 ¹	T1
B6	E2:7	SDMA7 ¹	T2
B4	E2:6	SDMA6 ¹	U4
A6	E2:5	SDMA5 ¹	U2
A4	E2:4	SDMA4 ¹	U1
B3	E2:3	SDMA3 ¹	V1
B1	E2:2	SDMA2 ¹	V3
A3	E2:1	SDMA1 ¹	W1
A1	E2:0	SDMA0 ¹	W2

Probe E2/E3

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	Q1-	Gnd	Gnd
A13	Q1+	RAS_CS1*	AA3
B12	C1:7	DA15 ³	J2
B10	C1:6	DA14 ³	F1
A12	C1:5	DA13 ³	AF19
A10	C1:4	DA12 ³	AF17
B9	C1:3	DA11 ³	AD26
B7	C1:2	PLL0/DA10 ³	A22
A9	C1:1	PLL1/DA9 ³	B19
A7	C1:0	PLL2/DA8 ³	A21
B6	C0:7	PLL3/DA7 ³	B18
B4	C0:6	PLL4/DA6 ³	B17
A6	C0:5	GNT4*/DA5 ³	W26
A4	C0:4	REQ4*/DA4 ³	Y26
B3	C0:3	PCICLK4/DA3 ³	AF26
B1	C0:2	DA2 ³	C25
A3	C0:1	CKO/DA1 ³	B15
A1	C0:0	QACK*/D0 ³	F2

Probe Connection C0/C1

Pad #	TLA Channel	MPC8240 Signal Name	MPC8240 Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	SDRAM_CLK ²	see Note 1
B12	C3:7	CAS/DQM7 ¹	J1
B10	C3:6	CAS/DQM6 ¹	K1
A12	C3:5	CAS/DQM5 ¹	AC2
A10	C3:4	CAS/DQM4 ¹	AC1
B9	C3:3	CAS/DQM3 ¹	K2
B7	C3:2	CAS/DQM2 ¹	K3
A9	C3:1	CAS/DQM1 ¹	AB2
A7	C3:0	CAS/DQM0 ¹	AB1
B6	C2:7	RAS_CS7*	L1
B4	C2:6	MAA2 ¹	AE1
A6	C2:5	MAA1 ¹	AF1
A4	C2:4	MAA0 ¹	AF2
B3	C2:3	SDRAS* ¹	AD1
B1	C2:2	SDCAS* ¹	AD2
A3	C2:1	WE* ¹	AA1
A1	C2:0	MIV* ¹	A16

Probe C2/C3

Notes:

- 1) Signal required for disassembly
- 2) Any active SDRAM clock signal can be used.
- 3) These signals are used for Debug Address support.

APPENDIX C - NEX-MPC8241/5 Mictor Pinout

NOTES: The pin numbers given for the MPC8241 are for the 357-pin Plastic Ball Grid Array (PBGA) package, and for the MPC8245 are for the 352-pin Tape Ball Grid Array (TBGA) package. Blank entries in the Pin # and Signal columns denote unused TLA inputs that may be wired to any user signal.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	CK0	RAS_CS5*	C8	L2	36	6	CK1	RAS_CS4*	C9	M2
4	7	A3:7	DL0 ¹	M19	AD17	35	8	A1:7	DL16 ¹	B3	B1
5	9	A3:6	DL1 ¹	M17	AE17	34	10	A1:6	DL17 ¹	C4	A1
6	11	A3:5	DL2 ¹	L16	AE15	33	12	A1:5	DL18 ¹	C2	A3
7	13	A3:4	DL3 ¹	L17	AF15	32	14	A1:4	DL19 ¹	D3	A4
8	15	A3:3	DL4 ¹	K18	AC14	31	16	A1:3	DL20 ¹	G5	A5
9	17	A3:2	DL5 ¹	J18	AE13	30	18	A1:2	DL21 ¹	E1	A6
10	19	A3:1	DL6 ¹	K17	AF13	29	20	A1:1	DL22 ¹	H5	A7
11	21	A3:0	DL7 ¹	K16	AF12	28	22	A1:0	DL23 ¹	E2	D7
12	23	A2:7	DL8 ¹	J15	AF11	27	24	A0:7	DL24 ¹	F1	A8
13	25	A2:6	DL9 ¹	J17	AF10	26	26	A0:6	DL25 ¹	F2	B8
14	27	A2:5	DL10 ¹	H18	AF9	25	28	A0:5	DL26 ¹	G2	A10
15	29	A2:4	DL11 ¹	F16	AD8	24	30	A0:4	DL27 ¹	J5	D10
16	31	A2:3	DL12 ¹	H16	AF8	23	32	A0:3	DL28 ¹	H1	A12
17	33	A2:2	DL13 ¹	H15	AF7	22	34	A0:2	DL29 ¹	H4	B11
18	35	A2:1	DL14 ¹	G17	AF6	21	36	A0:1	DL30 ¹	J4	B12
19	37	A2:0	DL15 ¹	D19	AE5	20	38	A0:0	DL31 ¹	J1	A14

A-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	Q0	RAS_CS0*	A17	Y4	36	6	CK2	RAS_CS6*	A10	M1
4	7	D3:7	DH0 ¹	M18	AC17	35	8	D1:7	DH16 ¹	C3	E4
5	9	D3:6	DH1 ¹	L18	AF16	34	10	D1:6	DH17 ¹	D4	A2
6	11	D3:5	DH2 ¹	L15	AE16	33	12	D1:5	DH18 ¹	E5	B3
7	13	D3:4	DH3 ¹	K19	AE14	32	14	D1:4	DH19 ¹	F5	D4
8	15	D3:3	DH4 ¹	K15	AF14	31	16	D1:3	DH20 ¹	D1	B4
9	17	D3:2	DH5 ¹	J19	AC13	30	18	D1:2	DH21 ¹	E4	B5
10	19	D3:1	DH6 ¹	J16	AE12	29	20	D1:1	DH22 ¹	D2	D6
11	21	D3:0	DH7 ¹	H17	AE11	28	22	D1:0	DH23 ¹	E3	C6
12	23	D2:7	DH8 ¹	G19	AE10	27	24	D0:7	DH24 ¹	F4	B7
13	25	D2:6	DH9 ¹	G18	AE9	26	26	D0:6	DH25 ¹	G3	C9
14	27	D2:5	DH10 ¹	G16	AE8	25	28	D0:5	DH26 ¹	G4	A9
15	29	D2:4	DH11 ¹	D18	AC7	24	30	D0:4	DH27 ¹	G1	B10
16	31	D2:3	DH12 ¹	F18	AE7	23	32	D0:3	DH28 ¹	H2	A11
17	33	D2:2	DH13 ¹	E18	AE6	22	34	D0:2	DH29 ¹	J3	A13
18	35	D2:1	DH14 ¹	G15	AF5	21	36	D0:1	DH30 ¹	J2	B13
19	37	D2:0	DH15 ¹	E15	AC5	20	38	D0:0	DH31 ¹	K5	A15

D-Group Mictor connector

Notes:

- 1) Signal required for disassembly

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	Q3	RAS_CS3*	C17	AC4	36	6	Q2	RAS_CS2*	C16	AA4
4	7	E3:7	RCS0*	C10	N4	35	8	E1:7	SDBA1 ¹	C11	P1
5	9	E3:6	SDMA14/ CHKSTOP_IN* ¹	K2	D14	34	10	E1:6	SDBA0 ¹	B11	P2
6	11	E3:5	SDMA13/TBEN ¹	K3	B14	33	12	E1:5	RCS1*	B9	N2
7	13	E3:4	SDMA12/SRESET* ¹	L3	B16	32	14	E1:4	RCS2*/TRIG_IN	P18	AF20
8	15	E3:3	SDMA11 ¹	A11	N1	31	16	E1:3	RCS3*/TRIG_OUT	N18	AC18
9	17	E3:2	SDMA10 ¹	B12	R1	30	18	E1:2			
10	19	E3:1	SDMA9 ¹	A12	R2	29	20	E1:1			
11	21	E3:0	SDMA8 ¹	C12	T1	28	22	E1:0			
12	23	E2:7	SDMA7 ¹	B13	T2	27	24	E0:7			
13	25	E2:6	SDMA6 ¹	C13	U4	26	26	E0:6			
14	27	E2:5	SDMA5 ¹	D12	U2	25	28	E0:5			
15	29	E2:4	SDMA4 ¹	A14	U1	24	30	E0:4			
16	31	E2:3	SDMA3 ¹	C14	V1	23	32	E0:3			
17	33	E2:2	SDMA2 ¹	B14	V3	22	34	E0:2			
18	35	E2:1	SDMA1 ¹	A15	W1	21	36	E0:1			
19	37	E2:0	SDMA0 ¹	B15	W2	20	38	E0:0			

E-Group Mictor connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	MPC824X Signal Name	8241 Pin #	8245 Pin #
3	5	CK3	SDRAM_CLK ²	Note 1	Note 1	36	6	Q1	RAS_CS1*	B17	AA3
4	7	C3:7	CAS/DQM7 ¹	B8	J1	35	8	C1:7	DA15 ³	D8	J2
5	9	C3:6	CAS/DQM6 ¹	A9	K1	34	10	C1:6	DA14 ³	B6	F1
6	11	C3:5	CAS/DQM5 ¹	D14	AC2	33	12	C1:5	DA13 ³	N16	AF19
7	13	C3:4	CAS/DQM4 ¹	D15	AC1	32	14	C1:4	DA12 ³	M16	AF17
8	15	C3:3	CAS/DQM3 ¹	C7	K2	31	16	C1:3	DA11 ³	T13	AD26
9	17	C3:2	CAS/DQM2 ¹	A6	K3	30	18	C1:2	PLL0/DA10 ³	N3	A22
10	19	C3:1	CAS/DQM1 ¹	B18	AB2	29	20	C1:1	PLL1/DA9 ³	N2	B19
11	21	C3:0	CAS/DQM0 ¹	A18	AB1	28	22	C1:0	PLL2/DA8 ³	N1	A21
12	23	C2:7	RAS_CS7*	B10	L1	27	24	C0:7	PLL3/DA7 ³	M4	B18
13	25	C2:6	MAA2 ¹	C18	AE1	26	26	C0:6	PLL4/DA6 ³	M3	B17
14	27	C2:5	MAA1 ¹	D17	AF1	25	28	C0:5	GNT4*/DA5 ³	T11	W26
15	29	C2:4	MAA0 ¹	E17	AF2	24	30	C0:4	REQ4*/DA4 ³	W13	Y26
16	31	C2:3	SDRAS* ¹	B19	AD1	23	32	C0:3	PCICLK4/DA3 ³	V17	AF26
17	33	C2:2	SDCAS* ¹	D16	AD2	22	34	C0:2	DA2 ³	R5	C25
18	35	C2:1	WE* ¹	B16	AA1	21	36	C0:1	CKO/DA1 ³	L1	B15
19	37	C2:0	MIV* ¹	K1	A16	20	38	C0:0	QACK*/DA0 ³	A3	F2

C-Group Mictor connector

Notes:

- 1) Signal required for disassembly
- 2) Any active SDRAM clock signal can be used.
- 3) These signals are used for Debug Address support.

APPENDIX D – NEX-MPC8241/5 P6860 Compression Pinouts

NOTES: The pin numbers given for the MPC8241 are for the 357-pin Plastic Ball Grid Array (PBGA) package, and for the MPC8245 are for the 352-pin Tape Ball Grid Array (TBGA) package. Blank entries in the Pin # and Signal columns denote unused TLA inputs that may be wired to any user signal.

For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	CK2-	Gnd	Gnd	Gnd
A13	CK2+	RAS_CS6*	A10	M1
B12	D1:7	DH16 ¹	C3	E4
B10	D1:6	DH17 ¹	D4	A2
A12	D1:5	DH18 ¹	E5	B3
A10	D1:4	DH19 ¹	F5	D4
B9	D1:3	DH20 ¹	D1	B4
B7	D1:2	DH21 ¹	E4	B5
A9	D1:1	DH22 ¹	D2	D6
A7	D1:0	DH23 ¹	E3	C6
B6	D0:7	DH24 ¹	F4	B7
B4	D0:6	DH25 ¹	G3	C9
A6	D0:5	DH26 ¹	G4	A9
A4	D0:4	DH27 ¹	G1	B10
B3	D0:3	DH28 ¹	H2	A11
B1	D0:2	DH29 ¹	J3	A13
A3	D0:1	DH30 ¹	J2	B13
A1	D0:0	DH31 ¹	K5	A15

Probe Connection D0/D1

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	CK1-	Gnd	Gnd	Gnd
A13	CK1+	RAS_CS4*	C9	M2
B12	A1:7	DL16 ¹	B3	B1
B10	A1:6	DL17 ¹	C4	A1
A12	A1:5	DL18 ¹	C2	A3
A10	A1:4	DL19 ¹	D3	A4
B9	A1:3	DL20 ¹	G5	A5
B7	A1:2	DL21 ¹	E1	A6
A9	A1:1	DL22 ¹	H5	A7
A7	A1:0	DL23 ¹	E2	D7
B6	A0:7	DL24 ¹	F1	A8
B4	A0:6	DL25 ¹	F2	B8
A6	A0:5	DL26 ¹	G2	A10
A4	A0:4	DL27 ¹	J5	D10
B3	A0:3	DL28 ¹	H1	A12
B1	A0:2	DL29 ¹	H4	B11
A3	A0:1	DL30 ¹	J4	B12
A1	A0:0	DL31 ¹	J1	A14

Probe A0/A1

Notes:

- 1) Signal required for disassembly
- 2) Any active SDRAM clock signal can be used.
- 3) These signals are used for Debug Address support.

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	Q0-	Gnd	Gnd	Gnd
A13	Q0+	RAS_CS0*	A17	Y4
B12	D3:7	DH0 ¹	M18	AC17
B10	D3:6	DH1 ¹	L18	AF16
A12	D3:5	DH2 ¹	L15	AE16
A10	D3:4	DH3 ¹	K19	AE14
B9	D3:3	DH4 ¹	K15	AF14
B7	D3:2	DH5 ¹	J19	AC13
A9	D3:1	DH6 ¹	J16	AE12
A7	D3:0	DH7 ¹	H17	AE11
B6	D2:7	DH8 ¹	G19	AE10
B4	D2:6	DH9 ¹	G18	AE9
A6	D2:5	DH10 ¹	G16	AE8
A4	D2:4	DH11 ¹	D18	AC7
B3	D2:3	DH12 ¹	F18	AE7
B1	D2:2	DH13 ¹	E18	AE6
A3	D2:1	DH14 ¹	G15	AF5
A1	D2:0	DH15 ¹	E15	AC5

Probe Connection D2/D3

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	CK0-	Gnd	Gnd	Gnd
A13	CK0+	RAS_CS5*	C8	L2
B12	A3:7	DL0 ¹	M19	AD17
B10	A3:6	DL1 ¹	M17	AE17
A12	A3:5	DL2 ¹	L16	AE15
A10	A3:4	DL3 ¹	L17	AF15
B9	A3:3	DL4 ¹	K18	AC14
B7	A3:2	DL5 ¹	J18	AE13
A9	A3:1	DL6 ¹	K17	AF13
A7	A3:0	DL7 ¹	K16	AF12
B6	A2:7	DL8 ¹	J15	AF11
B4	A2:6	DL9 ¹	J17	AF10
A6	A2:5	DL10 ¹	H18	AF9
A4	A2:4	DL11 ¹	F16	AD8
B3	A2:3	DL12 ¹	H16	AF8
B1	A2:2	DL13 ¹	H15	AF7
A3	A2:1	DL14 ¹	G17	AF6
A1	A2:0	DL15 ¹	D19	AE5

Probe A2/A3

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	Q2-	Gnd	Gnd	Gnd
A13	Q2+	RAS_CS2*	C16	AA4
B12	E1:7	SDBA1 ¹	C11	P1
B10	E1:6	SDBA0 ¹	B11	P2
A12	E1:5	RCS1*	B9	N2
A10	E1:4	RCS2*/TRIG_IN	P18	AF20
B9	E1:3	RCS3*/TRIG_OUT	N18	AC18
B7	E1:2			
A9	E1:1			
A7	E1:0			
B6	E0:7			
B4	E0:6			
A6	E0:5			
A4	E0:4			
B3	E0:3			
B1	E0:2			
A3	E0:1			
A1	E0:0			

Probe Connection E0/E1

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	Q3-	Gnd	Gnd	Gnd
A13	Q3+	RAS_CS3*	C17	AC4
B12	E3:7	RCS0*	C10	N4
B10	E3:6	SDMA14/ CHKSTOP_IN* ¹	K2	D14
A12	E3:5	SDMA13/TBEN ¹	K3	B14
A10	E3:4	SDMA12/SRESET* ¹	L3	B16
B9	E3:3	SDMA11 ¹	A11	N1
B7	E3:2	SDMA10 ¹	B12	R1
A9	E3:1	SDMA9 ¹	A12	R2
A7	E3:0	SDMA8 ¹	C12	T1
B6	E2:7	SDMA7 ¹	B13	T2
B4	E2:6	SDMA6 ¹	C13	U4
A6	E2:5	SDMA5 ¹	D12	U2
A4	E2:4	SDMA4 ¹	A14	U1
B3	E2:3	SDMA3 ¹	C14	V1
B1	E2:2	SDMA2 ¹	B14	V3
A3	E2:1	SDMA1 ¹	A15	W1
A1	E2:0	SDMA0 ¹	B15	W2

Probe E2/E3

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	Q1-	Gnd	Gnd	Gnd
A13	Q1+	RAS_CS1*	B17	AA3
B12	C1:7	DA15 ³	D8	J2
B10	C1:6	DA14 ³	B6	F1
A12	C1:5	DA13 ³	N16	AF19
A10	C1:4	DA12 ³	M16	AF17
B9	C1:3	DA11 ³	T13	AD26
B7	C1:2	PLL0/DA10 ³	N3	A22
A9	C1:1	PLL1/DA9 ³	N2	B19
A7	C1:0	PLL2/DA8 ³	N1	A21
B6	C0:7	PLL3/DA7 ³	M4	B18
B4	C0:6	PLL4/DA6 ³	M3	B17
A6	C0:5	GNT4*/DA5 ³	T11	W26
A4	C0:4	REQ4*/DA4 ³	W13	Y26
B3	C0:3	PCICLK4/DA3 ³	V17	AF26
B1	C0:2	DA2 ³	R5	C25
A3	C0:1	CKO/DA1 ³	L1	B15
A1	C0:0	QACK*/DA0 ³	A3	F2

Probe Connection C0/C1

Pad #	TLA Channel	MPC824X Signal Name	MPC8241 Pin #	MPC8245 Pin #
A15	CK3-	Gnd	Gnd	Gnd
A13	CK3+	SDRAM_CLK ²	Note 1	Note 1
B12	C3:7	CAS/DQM7 ¹	B8	J1
B10	C3:6	CAS/DQM6 ¹	A9	K1
A12	C3:5	CAS/DQM5 ¹	D14	AC2
A10	C3:4	CAS/DQM4 ¹	D15	AC1
B9	C3:3	CAS/DQM3 ¹	C7	K2
B7	C3:2	CAS/DQM2 ¹	A6	K3
A9	C3:1	CAS/DQM1 ¹	B18	AB2
A7	C3:0	CAS/DQM0 ¹	A18	AB1
B6	C2:7	RAS_CS7*	B10	L1
B4	C2:6	MAA2 ¹	C18	AE1
A6	C2:5	MAA1 ¹	D17	AF1
A4	C2:4	MAA0 ¹	E17	AF2
B3	C2:3	SDRAS* ¹	B19	AD1
B1	C2:2	SDCAS* ¹	D16	AD2
A3	C2:1	WE* ¹	B16	AA1
A1	C2:0	MIV* ¹	K1	A16

Probe C2/C3

Notes:

- 1) Signal required for disassembly
- 2) Any active SDRAM clock signal can be used.
- 3) These signals are used for Debug Address support.

APPENDIX E - Necessary Signals for Clocking

To properly acquire MPC824X bus activity in Bus Cycle Clocking mode (see Section 5.0 for further information on this mode), the following signals must be provided: CLK, SDRAS*, SDCAS*, and MIV*. If Bus Cycle Clocking does not work, move to the Activity Indicator window of the TLA and observe that these signals are toggling.

When using the NEX-824X support in Every Rising Edge of CLK mode, the only signal that is required is CLK, and this signal must show activity in the Activity Indicator window of the TLA.

APPENDIX F – Support for Simplified Mnemonics

The MPC8240 has a set of instruction codes defined in Appendix A of the MPC8240 Integrated Processor User's Manual, and these opcodes are the ones that are displayed by default in the disassembly listing. The MPC-8240 disassembler also supports the Simplified Mnemonics for the PowerPC family based on the following document:

"PowerPC Microprocessor Family: The Programming Environments"
Document G522-0290-00
Copyright Motorola, Inc. 1997.

The actual opcode binary between the two mnemonics is unchanged, simply the opcode text that is used to represent the opcode. Because there is no way for the MPC-8240 software to know which opcodes the user prefers to view a select field has been added to allow switching from one to the other. Refer to Section 6.1 for information on how this switching is done.

The following Simplified Mnemonics documented in Appendix F are supported:

F.3.1 Double-Word Comparisons

When a compare value involves a 64-bit value (L = 1), a 'd' is inserted into the mnemonic before the immediate indicator; an 'i' indicates a double-word compare.

F.3.2 Word Comparisons

When a compare value involves a 32-bit value (L = 0), a 'w' is inserted into the mnemonic before the immediate indicator; an 'i' indicates a word compare.

F.5.3 Branch Mnemonics Incorporating Conditions

For the 'bc' instruction variations, the BO and BI field values are used to produce appropriately modified mnemonics.

NOTES: so(un) and ns(u) are used where summary overflow and unordered overlap.

'Not less than' (nl) is shown as 'greater than or equal to' (ge).

'Not greater than' (ng) is shown as 'less than or equal to' (le).

F.6 Simplified Mnemonics for Condition Register Logical Instructions

The mnemonics are translated into set, clear, move and invert mnemonics.

F.7 Simplified Mnemonics for Trap Instructions

The TO values are used to produce a modified mnemonic.

NOTES: Support provided for:

lt, le, eq, ge, gt, ne, llt, lle, lge, lgt, Unconditional.

Remaining Mnemonics are represented as follows:

nl -> ge

ng -> le

lnl -> lge

lng -> lle

F.8 Simplified Mnemonics for Special-Purpose Registers

The SPR numeric value is used to produce a modified mnemonic containing the SPR identifier.

NOTES: There is an error in the table for Simplified Mnemonic for Move to SPRG0-SPRG3. The form shown under Simplified Mnemonic for Move from SPRG0-SPRG3 was followed. There is also an error for Simplified Mnemonic for Move from Time base lower. The form shown under Simplified Mnemonic for Move to Time base lower was followed.

F.9.1 No-Op

The 'nop' mnemonic replaces the 'ori 0,0,0' instruction.

F.9.2 Load Immediate

As appropriate, the 'addi' and 'addis' are replaced by 'li' and 'lis', respectively, when no addition is being performed.

F.9.4 Move Register

When no additional computation is being performed, the 'or' mnemonic is replaced by 'mr'.

F.9.5 Complement Register

When no additional computation is being performed, the 'nor' mnemonic is replaced by 'not'.

F.9.6 Move To Condition Register

When the low-order 32 bits of a General Purpose Register is moved to the Condition Register, the 'mtrf' mnemonic is translated to the 'mtr' form.

APPENDIX G - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX H - References

Tektronix TLA700 System User's Manual

Tektronix TLA700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

Tektronix P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual

Motorola MPC8240 Integrated Processor Hardware Specification
Document #MPC8240EC/D; 07/2000; Rev 0.5

Motorola MPC8240 Integrated Processor User's Manual
Document #MPC8240UM/D; 07/1999; Rev. 0

Motorola - PowerPC™ Microprocessor Family: The Programming Environments
Document #MPCFPE/AD; 1/97; REV. 1