NEX-NEXVuDDR667x8SR/DRxU

DDRII Unbuffered Synchronous
DRAM MTS-DIMM Support NEXVuDDR533 thru 667

Including these Software Support packages:

DDR2M-3A DDR2M-2A
DDR2M-2B DDRSPA

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1.0 OVERVIEW

1.1 General Information

The NEXVu families of Logic Analyzer DIMMs (NEX-NEXVUDDR667XU-x) Logic Analyzer DIMMs has been designed to provide a quick and easy connection to interface a Tektronix TLA700 Logic Analyzer to a 240-pin DDRII (Double Data Rate II) Synchronous DRAM Dual In-Line Memory Module (SDRAM DIMM) DIMM. **Contact Nexus Technology for other available DDRII NEXVu-DIMM supports, and current DIMMs and software this manual covers**.

This manual covers all Unbuffered NEXVu DDR products from NEXUS. While it refers to the latest version, the information is directly applicable to the lower speed 533 versions.

Note: The NEX-NEXVuDDR667xU DIMMs will operate as specified by Micron at 667MT/s. If your top rate is 400MT/s consider the DDR2M-2A support package. This software package gives full support but only requires two Logic Analyzer modules. The DDR2M-2A software support package is a standard support included in this package.
At printing this manual covered the following Nexus products: All Unbuffered NEXVu DDR products and options. Call for a full list of available products.

Logic Analyzer connections are made using P6860 or P6864 High-Density Connectorless probes to help minimize the size of the Logic Analyzer DIMM board, thus reducing trace length and keeping signal loading to a minimum.

The NEX-NEXVuDDR667xU support includes three software packages that can be used with different TLA configurations to acquire DDR2 data at up to 667MT/s speeds:

DDR2M-3A allows the user to acquire DDRII 667 Read **AND** Write data from a target. This support requires 4-P6860 and 4-P6864 High-Density Compression probes, and three merged TLA7AA4 or TLA7AB4 136-channel 450MHz state speed acquisition cards.

DDR2M-2A allows the user to acquire DDRII up to 400MT/s Read **AND** Write data from a target. This support requires 8-P6860 High-Density Compression probes, and two merged TLA7AA4 or TLA7AB4 136-channel 450MHz state speed acquisition cards.

DDR2M-2B allows the user to acquire DDRII 667 Read **OR** Write data from a target. This support requires 8-P6860 High-Density Compression probes, and two merged TLA7AA4 or TLA7AB4 136-channel 450MHz state speed acquisition cards.

The NEX-NEXVuDDR667xU supports are usable with a TLA7XX-series Logic Analyzer only, and the TLA must be running V4.2 or later of the TLA Application Software. The NEX-NEXVuDDR667xU software also post-processes the acquisition to display valid cycle information to the user.

Note that this manual uses some terms generically. For instance, references to the TLA700 apply to all suitable TLA700 Logic Analyzers. NEX-NEXVuDDR667xU refers to both the DDR2M-3A, DDR2M-2A and DDR2M-2B software support packages.

Appendix E has a silk-screened print of the NEX-NEXVUDDR667XU-A Logic Analyzer DIMM board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the DDR-II SDRAM Specification and the Tektronix TLA700 Logic Analyzers. It is also expected that the user is familiar with the Windows environment used on the TLA.

2.0 SOFTWARE INSTALLATION

The NEX-NEXVuDDR667xU software is installed using the same method as other Windows programs. Place the DDR2M-3A, DDR2M-2A or DDR2M-2B Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer module in the Setup window, select Load Support Package from the File pull-down, then choose either DDR2M-3A, DDR2M-2A, or DDR2M-2B and click on **Okay**. Note that the selected support may require two or three merged modules and that the TLA acquisition cards must be configured properly for the software to load.

3.0 CONNECTING to the NEX-NEXVuDDR667xU DIMM

3.1 General

Care should be taken to support the weight of the acquisition probes so that the Logic Analyzer DIMM board and/or target socket are not damaged

The NEX-NEXVuDDR667xU support TLA requirements vary depending upon the data rate of the DDRII interface and the desire to acquire both Read **and** Write data or Read **or** Write data.

To acquire DDRII Read **and** Write data at speeds up to 667MT/s will require three merged TLA7Ax4 136-channel 450MHz state speed acquisition cards and the use of the **DDR2M-3A** support software. The Master card will be in the center of the three cards; Slave card #1 is in the adjacent high-numbered slots and Slave card #2 will be in the adjacent lower-numbered slots. The logic analyzer modules should be connected to the NEX-NEXVUDDR667XU-A DIMM as follows using four (4) P6860 probes and four (4) P6864 probes:

TLA Master P6860 **A3/A2** probe head to DDRII DIMM **M_A3/A2** position
TLA Master P6860 **A1/A0** probe head to DDRII DIMM **M_A1/A0** position
TLA Master P6860 **D3/D2** probe head to DDRII DIMM **M_D3/D2** position
TLA Master P6860 **D1/D0** probe head to DDRII DIMM **M_D1/D0** position
TLA Master P6860 **C3/C2** probe head to DDRII DIMM **M_C3/C2** position
TLA Master P6860 **C1/C0** probe head to DDRII DIMM **M_C1/C0** position
TLA Master P6860 **E3/E2** probe head to DDRII DIMM **M_E3/E2** position
TLA Slave #1 P6864 **C3/E3** probe head to DDRII DIMM **S_C3/E3** position
TLA Slave #1 P6864 **A1/A3** probe head to DDRII DIMM **S_A1/A3** position
TLA Slave #2 P6864 **C3/E3** probe head to DDRII DIMM **S2_C3/E3** position
TLA Slave #2 P6864 **A1/A3** probe head to DDRII DIMM **S2_A1/A3** position

Above shows the Channel Grouping / Wiring for use with the **DDR2M-3A** support.
Note that Logic Analyzer connections can be made on either the from or back of the NEXVu DIMM.

A TLA configuration with two merged TLA7Ax4 136-channel 450MHz state speed acquisition cards can be used to acquire Read **and** Write data at up to 400MT/s speeds (**DDR2M-2A**) or Read **or** Write data at up to 667MT/s rates (**DDR2M-2B**). In either case the Master acquisition card will be in the lower-numbered mainframe slots while the Slave card will be in the adjacent higher-numbered slots. With either support package the acquisition cards should be connected to the NEX-NEXVuDDR667xU Logic Analyzer DIMM as follows using eight (8) P6860 probes:

TLA Master P6860 **A3/A2** probe head to DDRII DIMM **M_A3/A2** position
TLA Master P6860 **A1/A0** probe head to DDRII DIMM **M_A1/A0** position
TLA Master P6860 **D3/D2** probe head to DDRII DIMM **M_D3/D2** position
TLA Master P6860 **D1/D0** probe head to DDRII DIMM **M_D1/D0** position
TLA Master P6860 **C3/C2** probe head to DDRII DIMM **M_C3/C2** position
TLA Master P6860 **C1/C0** probe head to DDRII DIMM **M_C1/C0** position
TLA Master P6860 **E3/E2** probe head to DDRII DIMM **M_E3/E2** position
TLA Slave P6860 **C3/C2** probe head to DDRII DIMM **S_C3/E3** position
TLA Slave P6860 **A3/A2** probe head to DDRII DIMM **S_A1/A3** position
TLA Slave P6860 **E3/E2** probe head to DDRII DIMM **S2_C3/E3** position
TLA Slave P6860 **A1/A0** probe head to DDRII DIMM **S2_A1/A3** position

Above shows the Channel Grouping / Wiring for use with the **DDR2M-2A** support, and Table 3 shows the Channel Grouping / Wiring for the **DDR2M-2B** support.
Note that Logic Analyzer connections can be made on either the from or back of the NEXVu DIMM.

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RdA_DatHi (Hex)	RD_A_DQ63	236	S2_C3:0	RdA_DatLo (Hex)	RD_A_DQ31	159	S2_A1:5
	RD_A_DQ62	235	S2_C3:1		RD_A_DQ30	158	S2_A1:4
	RD_A_DQ61	230	S2_E3:7		RD_A_DQ29	153	S2_A3:1
	RD_A_DQ60	229	S2_E3:6		RD_A_DQ28	152	S2_A3:0
	RD_A_DQ59	117	S2_C3:2		RD_A_DQ27	40	S2_A1:3
	RD_A_DQ58	116	S2_C3:3		RD_A_DQ26	39	S2_A1:2
	RD_A_DQ57	111	S2_C3:4		RD_A_DQ25	34	S2_A1:1
	RD_A_DQ56	110	S2_C3:5		RD_A_DQ24	33	S2_A1:0
	RD_A_DQ55	227	S2_E3:5		RD_A_DQ23	150	S_C3:0
	RD_A_DQ54	226	S2_E3:4		RD_A_DQ22	149	S_C3:1
	RD_A_DQ53	218	S2_C3:6		RD_A_DQ21	144	S_E3:7
	RD_A_DQ52	217	S2_C3:7		RD_A_DQ20	143	S_E3:6
	RD_A_DQ51	108	S2_E3:3		RD_A_DQ19	31	S_C3:2
	RD_A_DQ50	107	S2_E3:2		RD_A_DQ18	30	S_C3:3
	RD_A_DQ49	99	S_A3:7		RD_A_DQ17	25	S_C3:4
	RD_A_DQ48	98	S_A3:6		RD_A_DQ16	24	S_C3:5
	RD_A_DQ47	215	S2_E3:1		RD_A_DQ15	141	S_E3:5
	RD_A_DQ46	214	S2_E3:0		RD_A_DQ14	140	S_E3:4
	RD_A_DQ45	209	S_A3:5		RD_A_DQ13	132	S_E3:3
	RD_A_DQ44	208	S_A3:4		RD_A_DQ12	131	S_E3:2
	RD_A_DQ43	96	S_A1:0		RD_A_DQ11	22	S_C3:6
	RD_A_DQ42	95	S_A1:1		RD_A_DQ10	21	S_C3:7
	RD_A_DQ41	90	S_ A1:2		RD_A_DQ9	13	M_E3:0
	RD_A_DQ40	89	S_ A1:3		RD_A_DQ8	12	M_E3:1
	RD_A_DQ39	206	S_ A3:3		RD_A_DQ7	129	S_E3:1
	RD_A_DQ38	205	S_ A3:2		RD_A_DQ6	128	S_E3:0
	RD_A_DQ37	200	S_ A3:1		RD_A_DQ5	123	M_E3:2
	RD_A_DQ36	199	S_ A3:0		RD_A_DQ4	122	M_E3:3
	RD_A_DQ35	87	S_ A1:4		RD_A_DQ3	10	M_E3:4
	RD_A_DQ34	86	S_ A1:5		RD_A_DQ2	9	M_E3:5
	RD_A_DQ33	81	S_ A1:6		RD_A_DQ1	4	M_E3:6
	RD_A_DQ32	80	S_ A1:7		RD_A_DQ0	3	M_E3:7

Table 1- DDR2M-3A (667 Read & Write) TLA Channel Grouping

Notes:

All signals on this page are required for accurate post-processing of acquired data
The ‘S’ in front of a TLA channel denotes Slave card #1 of the merged set
The ‘S2’ in front of a TLA channel denotes Slave card #2 of the merged set
The ‘M’ in front of a TLA channel denotes the Master card of the merged set

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RdB_DatHi	RD_B_DQ63	236	S2_C2:0	RdB_DatLo	RD_B_DQ31	159	S2_A0:5
(Hex)	RD_B_DQ62	235	S2_C2:1	(Hex)	RD_B_DQ30	158	S2_A0:4
	RD_B_DQ61	230	S2_E2:7		RD_B_DQ29	153	S2_A2:1
	RD_B_DQ60	229	S2_E2:6		RD_B_DQ28	152	S2_A2:0
	RD_B_DQ59	117	S2_C2:2		RD_B_DQ27	40	S2_A0:3
	RD_B_DQ58	116	S2_C2:3		RD_B_DQ26	39	S2_A0:2
	RD_B_DQ57	111	S2_C2:4		RD_B_DQ25	34	S2_A0:1
	RD_B_DQ56	110	S2_C2:5		RD_B_DQ24	33	S2_A0:0
	RD_B_DQ55	227	S2_E2:5		RD_B_DQ23	150	S_C2:0
	RD_B_DQ54	226	S2_E2:4		RD_B_DQ22	149	S_C2:1
	RD_B_DQ53	218	S2_C2:6		RD_B_DQ21	144	S_E2:7
	RD_B_DQ52	217	S2_C2:7		RD_B_DQ20	143	S_E2:6
	RD_B_DQ51	108	S2_E2:3		RD_B_DQ19	31	S_C2:2
	RD_B_DQ50	107	S2_E2:2		RD_B_DQ18	30	S_C2:3
	RD_B_DQ49	99	S_A2:7		RD_B_DQ17	25	S_C2:4
	RD_B_DQ48	98	S_A2:6		RD_B_DQ16	24	S_C2:5
	RD_B_DQ47	215	S2_E2:1		RD_B_DQ15	141	S_E2:5
	RD_B_DQ46	214	S2_E2:0		RD_B_DQ14	140	S_E2:4
	RD_B_DQ45	209	S_A2:5		RD_B_DQ13	132	S_E2:3
	RD_B_DQ44	208	S_A2:4		RD_B_DQ12	131	S_E2:2
	RD_B_DQ43	96	S_A0:0		RD_B_DQ11	22	S_C2:6
	RD_B_DQ42	95	S_A0:1		RD_B_DQ10	21	S_C2:7
	RD_B_DQ41	90	S_ A0:2		RD_B_DQ9	13	M_E2:0
	RD_B_DQ40	89	S_ A0:3		RD_B_DQ8	12	M_E2:1
	RD_B_DQ39	206	S_ A2:3		RD_B_DQ7	129	S_E2:1
	RD_B_DQ38	205	S_ A2:2		RD_B_DQ6	128	S_E2:0
	RD_B_DQ37	200	S_ A2:1		RD_B_DQ5	123	M_E2:2
	RD_B_DQ36	199	S_ A2:0		RD_B_DQ4	122	M_E2:3
	RD_B_DQ35	87	S_ A0:4		RD_B_DQ3	10	M_E2:4
	RD_B_DQ34	86	S_ A0:5		RD_B_DQ2	9	M_E2:5
	RD_B_DQ33	81	S_ A0:6		RD_B_DQ1	4	M_E2:6
	RD_B_DQ32	80	S_ A0:7		RD_B_DQ0	3	M_E2:7

Table 1 – DDR2M-3A (667 Read and Write) TLA Channel Grouping (cont’d.)

Notes:

All signals on this page are required for accurate post-processing of acquired data
The ‘S’ in front of a TLA channel denotes the Slave card of the merged set
The ‘S2’ in front of a TLA channel denotes the Slave 2 card of the merged set
The ‘M’ in front of a TLA channel denotes the Master card of the merged set
All signals on this page are acquired using the TLA’s demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
WrA_DatHi (Hex)	WR_A_DQ63	236	S2_C1:0	WrA_DatLo (Hex)	WR_A_DQ31	159	S2_D1:5
	WR_A_DQ62	235	S2_C1:1		WR_A_DQ30	158	S2_D1:4
	WR_A_DQ61	230	S2_E1:7		WR_A_DQ29	153	S2_D3:1
	WR_A_DQ60	229	S2_E1:6		WR_A_DQ28	152	S2_D3:0
	WR_A_DQ59	117	S2_C1:2		WR_A_DQ27	40	S2_D1:3
	WR_A_DQ58	116	S2_C1:3		WR_A_DQ26	39	S2_D1:2
	WR_A_DQ57	111	S2_C1:4		WR_A_DQ25	34	S2_D1:1
	WR_A_DQ56	110	S2_C1:5		WR_A_DQ24	33	S2_D1:0
	WR_A_DQ55	227	S2_E1:5		WR_A_DQ23	150	S_C1:0
	WR_A_DQ54	226	S2_E1:4		WR_A_DQ22	149	S_C1:1
	WR_A_DQ53	218	S2_C1:6		WR_A_DQ21	144	S_E1:7
	WR_A_DQ52	217	S2_C1:7		WR_A_DQ20	143	S_E1:6
	WR_A_DQ51	108	S2_E1:3		WR_A_DQ19	31	S_C1:2
	WR_A_DQ50	107	S2_E1:2		WR_A_DQ18	30	S_C1:3
	WR_A_DQ49	99	S_D3:7		WR_A_DQ17	25	S_C1:4
	WR_A_DQ48	98	S_D3:6		WR_A_DQ16	24	S_C1:5
	WR_A_DQ47	215	S2_E1:1		WR_A_DQ15	141	S_E1:5
	WR_A_DQ46	214	S2_E1:0		WR_A_DQ14	140	S_E1:4
	WR_A_DQ45	209	S_D3:5		WR_A_DQ13	132	S_E1:3
	WR_A_DQ44	208	S_D3:4		WR_A_DQ12	131	S_E1:2
	WR_A_DQ43	96	S_D1:0		WR_A_DQ11	22	S_C1:6
	WR_A_DQ42	95	S_D1:1		WR_A_DQ10	21	S_C1:7
	WR_A_DQ41	90	S_ D1:2		WR_A_DQ9	13	M_E1:0
	WR_A_DQ40	89	S_ D1:3		WR_A_DQ8	12	M_E1:1
	WR_A_DQ39	206	S_ D3:3		WR_A_DQ7	129	S_E1:1
	WR_A_DQ38	205	S_ D3:2		WR_A_DQ6	128	S_E1:0
	WR_A_DQ37	200	S_ D3:1		WR_A_DQ5	123	M_E1:2
	WR_A_DQ36	199	S_ D3:0		WR_A_DQ4	122	M_E1:3
	WR_A_DQ35	87	S_ D1:4		WR_A_DQ3	10	M_E1:4
	WR_A_DQ34	86	S_ D1:5		WR_A_DQ2	9	M_E1:5
	WR_A_DQ33	81	S_ D1:6		WR_A_DQ1	4	M_E1:6
	WR_A_DQ32	80	S_ D1:7		WR_A_DQ0	3	M_E1:7

Table 1 – DDR2M-3A (667 Read and Write) TLA Channel Grouping (cont'd.)

Notes:

All signals on this page are required for accurate post-processing of acquired data
The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
The 'M' in front of a TLA channel denotes the Master card of the merged set
All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
WrB_DatHi	WR_B_DQ63	236	S2_C0:0	WrB_DatLo	WR_B_DQ31	159	S2_D0:5
(Hex)	WR_B_DQ62	235	S2_C0:1	(Hex)	WR_B_DQ30	158	S2_D0:4
	WR_B_DQ61	230	S2_E0:7		WR_B_DQ29	153	S2_D2:1
	WR_B_DQ60	229	S2_E0:6		WR_B_DQ28	152	S2_D2:0
	WR_B_DQ59	117	S2_C0:2		WR_B_DQ27	40	S2_D0:3
	WR_B_DQ58	116	S2_C0:3		WR_B_DQ26	39	S2_D0:2
	WR_B_DQ57	111	S2_C0:4		WR_B_DQ25	34	S2_D0:1
	WR_B_DQ56	110	S2_C0:5		WR_B_DQ24	33	S2_D0:0
	WR_B_DQ55	227	S2_E0:5		WR_B_DQ23	150	S_C0:0
	WR_B_DQ54	226	S2_E0:4		WR_B_DQ22	149	S_C0:1
	WR_B_DQ53	218	S2_C0:6		WR_B_DQ21	144	S_E0:7
	WR_B_DQ52	217	S2_C0:7		WR_B_DQ20	143	S_E0:6
	WR_B_DQ51	108	S2_E0:3		WR_B_DQ19	31	S_C0:2
	WR_B_DQ50	107	S2_E0:2		WR_B_DQ18	30	S_C0:3
	WR_B_DQ49	99	S_D2:7		WR_B_DQ17	25	S_C0:4
	WR_B_DQ48	98	S_D2:6		WR_B_DQ16	24	S_C0:5
	WR_B_DQ47	215	S2_E0:1		WR_B_DQ15	141	S_E0:5
	WR_B_DQ46	214	S2_E0:0		WR_B_DQ14	140	S_E0:4
	WR_B_DQ45	209	S_D2:5		WR_B_DQ13	132	S_E0:3
	WR_B_DQ44	208	S_D2:4		WR_B_DQ12	131	S_E0:2
	WR_B_DQ43	96	S_D0:0		WR_B_DQ11	22	S_C0:6
	WR_B_DQ42	95	S_D0:1		WR_B_DQ10	21	S_C0:7
	WR_B_DQ41	90	S_ D0:2		WR_B_DQ9	13	M_E0:0
	WR_B_DQ40	89	S_ D0:3		WR_B_DQ8	12	M_E0:1
	WR_B_DQ39	206	S_ D2:3		WR_B_DQ7	129	S_E0:1
	WR_B_DQ38	205	S_ D2:2		WR_B_DQ6	128	S_E0:0
	WR_B_DQ37	200	S_ D2:1		WR_B_DQ5	123	M_E0:2
	WR_B_DQ36	199	S_ D2:0		WR_B_DQ4	122	M_E0:3
	WR_B_DQ35	87	S_ D0:4		WR_B_DQ3	10	M_E0:4
	WR_B_DQ34	86	S_ D0:5		WR_B_DQ2	9	M_E0:5
	WR_B_DQ33	81	S_ D0:6		WR_B_DQ1	4	M_E0:6
	WR_B_DQ32	80	S_ D0:7		WR_B_DQ0	3	M_E0:7

Table 1 – DDR2M-3A (667 Read and Write) TLA Channel Grouping (cont'd.)

Notes:

All signals on this page are required for accurate post-processing of acquired data
The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
The 'M' in front of a TLA channel denotes the Master card of the merged set
All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RdAChkBits	RD_A_CB7	168	S2_A3:7	WrAChkBits [5]	WR_A_CB7	168	S2_D3:7
(OFF)	RD_A_CB6	167	S2_A3:6	(OFF)	WR_A_CB6	167	S2_D3:6
	RD_A_CB5	162	S2_A1:7		WR_A_CB5	162	S2_ D1:7
	RD_A_CB4	161	S2_A1:6		WR_A_CB4	161	S2_ D1:6
	RD_A_CB3	49	S2_A3:5		WR_A_CB3	49	S2_ D3:5
	RD_A_CB2	48	S2_A3:4		WR_A_CB2	48	S2_ D3:4
	RD_A_CB1	43	S2_A3:3		WR_A_CB1	43	S2_ D3:3
	RD_A_CB0	42	S2_A3:2		WR_A_CB0	42	S2_ D3:2
RdBChkBits [5]	RD_B_CB7	168	S2_A2:7	WrBChkBits [5]	WR_B_CB7	168	S2_D2:7
(OFF)	RD_B_CB6	167	S2_A2:6	(OFF)	WR_B_CB6	167	S2_D2:6
	RD_B_CB5	162	S2_A0:7		WR_B_CB5	162	S2_D0:7
	RD_B_CB4	161	S2_A0:6		WR_B_CB4	161	S2_D0:6
	RD_B_CB3	49	S2_A2:5		WR_B_CB3	49	S2_D2:5
	RD_B_CB2	48	S2_A2:4		WR_B_CB2	48	S2_D2:4
	RD_B_CB1	43	S2_A2:3		WR_B_CB1	43	S2_D2:3
	RD_B_CB0	42	S2_A2:2		WR_B_CB0	42	S2_D2:2
ADatMsks	A_DM7	232	M_A2:7	BDatMsks [5]	B_DM7	232	M_D2:7
(BIN)	A_DM6	223	M_A3:3	(BIN)	B_DM6	223	M_D3:3
	A_DM5	211	M_A3:7		B_DM5	211	M_D3:7
	A_DM4	202	M_C2:5		B_DM4	202	M_C0:5
	A_DM3	155	M_C1:4		B_DM3	155	M_C3:4
	A_DM2	146	M_D1:6		B_DM2	146	M_A1:6
	A_DM1	134	M_D1:0		B_DM1	134	M_A1:0
	A_DM0	125	M_D0:0		B_DM0	125	M_A0:0
Strobes	DQS7	114	M_A2:4	Address	BA2	54	M_A1:4
(HEX)	DQS6	105	M_A3:0	(Hex)	BA1	190	M_E3:4
	DQS5	93	M_D2:4		BA0	71	M_D3:2
	DQS4	84	M_D3:0		A13	196	M_D2:2
	DQS3	37	M_C0:3		A12	176	M_C1:6
	DQS2	28	M_D1:5		A11	57	M_A1:2
	DQS1	16	M_D0:7		A10/AP	70	M_C3:2
	DQS0	7	M_D0:3		A9	177	M_C1:7
Command	S1#/GND	76	M_Q0		A8	179	M_A0:7
(Sym)	S0#	193	M_C2:2		A7	58	M_A1:1
	RAS#	192	M_C2:3		A6	180	M_A0:6
	CAS#	74	M_C2:0		A5	60	M_A0:5
	WE#	73	M_C2:1		A4	61	M_ A0:4
Misc	DDRCK2+/-	220/221	M_CK0		A3	182	M_ A0:3
(OFF)	DDRCK1+/-	137/138	M_CK2		A2	63	M_ A0:1
	DDRCK0+/-	185/186	M_CK3		A1	183	M_ A0:2
					A0	188	M_ D3:6

Table 1 – DDR2M-3A (667 Read and Write) TLA Channel Grouping (cont'd.)

Notes:

' # ' denotes a low-true signal
All signals on this page are required for accurate post-processing of acquired data
The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
The 'M' in front of a TLA channel denotes the Master card of the merged set
Signals in these groups are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
Ungrouped	ODT1/GND	77	M_D3:5	Ungrouped	CKE1	171	M_Q1
	ODT0	195	M_D2:3		CKE0	52	M_CK1
	RC0	55	M_A1:3		A15	173	M_C1:2
	SCL	120	M_A2:0		A14	174	M_C1:3
	SDA	119	M_ A2:1		A13	196	M_D2:2
	SA2	101	M_ A3:5		GND	18	M_D1:2
	SA1	240	M_ A2:2		A_DM8	164	M_C1:2
	SA0	239	M_ A2:3		B_DM8	164	M_C3:0
	NC_TEST	102	M_A3:4		DQS8	46	M_C0:7
	GND	19	M_D1:3		DQS8#	45	M_C0:6
	GND	68	M_C3:3		DQS7#	113	M_A2:5
	GND	112	M_A3:6		DQS6#	104	M_A3:1
	GND	135	M_D1:1		DQS5#	92	M_D2:5
	GND	147	M_D1:7		DQS4#	83	M_D3:1
	GND	165	M_C1:1		DQS3#	36	M_C0:2
	GND	203	M_C2:4		DQS2#	27	M_D1:4
	GND	224	M_A3:2		DQS1#	15	M_D0:6
	GND	233	M_A2:6		DQS0#	6	M_D0:2

Table 1 – DDR2M-3A (667 Read and Write) TLA Channel Grouping (cont'd.)

Notes:

' # ' denotes a low-true signal
The 'M' in front of a TLA channel denotes the Master card of the merged set

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RDDatHi	RD_DQ63	236	S_ E2:0	RDDatLo	RD_DQ31	159	S_A1:1
(Hex)	RD_DQ62	235	S_ E2:1	(Hex)	RD_DQ30	158	S_A1:0
	RD_DQ61	230	S_ E2:2		RD_DQ29	153	S_A0:3
	RD_DQ60	229	S_ E2:3		RD_DQ28	152	S_A0:2
	RD_DQ59	117	S_ E2:4		RD_DQ27	40	S_A0:5
	RD_DQ58	116	S_ E2:5		RD_DQ26	39	S_A0:4
	RD_DQ57	111	S_ E3:0		RD_DQ25	34	S_A0:1
	RD_DQ56	110	S_ E3:1		RD_DQ24	33	S_A0:0
	RD_DQ55	227	S_E2:6		RD_DQ23	150	S_C2:0
	RD_DQ54	226	S_E2:7		RD_DQ22	149	S_C2:1
	RD_DQ53	218	S_ E3:4		RD_DQ21	144	S_C2:2
	RD_DQ52	217	S_E3:5		RD_DQ20	143	S_C2:3
	RD_DQ51	108	S_E3:2		RD_DQ19	31	S_C2:4
	RD_DQ50	107	S_E3:3		RD_DQ18	30	S_C2:5
	RD_DQ49	99	S_A2:2		RD_DQ17	25	S_C3:0
	RD_DQ48	98	S_A2:3		RD_DQ16	24	S_C3:1
	RD_DQ47	215	S_E3:6		RD_DQ15	141	S_C2:6
	RD_DQ46	214	S_E3:7		RD_DQ14	140	S_C2:7
	RD_DQ45	209	S_A2:6		RD_DQ13	132	S_C3:2
	RD_DQ44	208	S_A2:7		RD_DQ12	131	S_C3:3
	RD_DQ43	96	S_A2:0		RD_DQ11	22	S_C3:4
	RD_DQ42	95	S_A2:1		RD_DQ10	21	S_C3:5
	RD_DQ41	90	S_ A2:4		RD_DQ9	13	M_E3:0
	RD_DQ40	89	S_ A2:5		RD_DQ8	12	M_E3:1
	RD_DQ39	206	S_ A3:2		RD_DQ7	129	S_C3:6
	RD_DQ38	205	S_ A3:3		RD_DQ6	128	S_C3:7
	RD_DQ37	200	S_ A3:6		RD_DQ5	123	M_E3:2
	RD_DQ36	199	S_ A3:7		RD_DQ4	122	M_E3:3
	RD_DQ35	87	S_ A3:0		RD_DQ3	10	M_E3:4
	RD_DQ34	86	S_ A3:1		RD_DQ2	9	M_E3:5
	RD_DQ33	81	S_ A3:4		RD_DQ1	4	M_E3:6
	RD_DQ32	80	S_ A3:5		RD_DQ0	3	M_E3:7

Table 2- DDR2M-2A (400 Read & Write) TLA Channel Grouping

Notes:

All signals are required for accurate post-processing of acquired data
The 'S' in front of a TLA channel denotes the Slave card of the merged pair
The 'M' in front of a TLA channel denotes the Master card of the merged pair

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
WRDatHi (Hex)	WR_DQ63	236	S_ E0:0	WRDatLo (Hex)	WR_DQ31	236	S_D1:1
	WR_DQ62	235	S_ E0:1		WR_DQ30	235	S_D1:0
	WR_DQ61	230	S_ E0:2		WR_DQ29	230	S_D0:3
	WR_DQ60	229	S_ E0:3		WR_DQ28	229	S_D0:2
	WR_DQ59	117	S_ E0:4		WR_DQ27	117	S_D0:5
	WR_DQ58	116	S_ E0:5		WR_DQ26	116	S_D0:4
	WR_DQ57	111	S_ E1:0		WR_DQ25	111	S_D0:1
	WR_DQ56	110	S_ E1:1		WR_DQ24	110	S_D0:0
	WR_DQ55	227	S_E0:6		WR_DQ23	227	S_C0:0
	WR_DQ54	226	S_E0:7		WR_DQ22	226	S_C0:1
	WR_DQ53	218	S_ E1:4		WR_DQ21	218	S_C0:2
	WR_DQ52	217	S_E1:5		WR_DQ20	217	S_C0:3
	WR_DQ51	108	S_E1:2		WR_DQ19	108	S_C0:4
	WR_DQ50	107	S_E1:3		WR_DQ18	107	S_C0:5
	WR_DQ49	99	S_D2:2		WR_DQ17	99	S_C1:0
	WR_DQ48	98	S_D2:3		WR_DQ16	98	S_C1:1
	WR_DQ47	215	S_E1:6		WR_DQ15	215	S_C0:6
	WR_DQ46	214	S_E1:7		WR_DQ14	214	S_C0:7
	WR_DQ45	209	S_D2:6		WR_DQ13	209	S_C1:2
	WR_DQ44	208	S_D2:7		WR_DQ12	208	S_C1:3
	WR_DQ43	96	S_D2:0		WR_DQ11	96	S_C1:4
	WR_DQ42	95	S_D2:1		WR_DQ10	95	S_C1:5
	WR_DQ41	90	S_ D2:4		WR_DQ9	90	M_E1:0
	WR_DQ40	89	S_ D2:5		WR_DQ8	89	M_E1:1
	WR_DQ39	206	S_ D3:2		WR_DQ7	206	S_C1:6
	WR_DQ38	205	S_ D3:3		WR_DQ6	205	S_C1:7
	WR_DQ37	200	S_ D3:6		WR_DQ5	200	M_E1:2
	WR_DQ36	199	S_ D3:7		WR_DQ4	199	M_E1:3
	WR_DQ35	87	S_ D3:0		WR_DQ3	87	M_E1:4
	WR_DQ34	86	S_ D3:1		WR_DQ2	86	M_E1:5
	WR_DQ33	81	S_ D3:4		WR_DQ1	81	M_E1:6
	WR_DQ32	80	S_ D3:5		WR_DQ0	80	M_E1:7

Table 2 – DDR2M-2A (400 Read and Write) TLA Channel Grouping (cont'd)

Notes:

All signals on this page are required for accurate post-processing of acquired data
The 'S' in front of a TLA channel denotes the Slave card of the merged pair
The 'M' in front of a TLA channel denotes the Master card of the merged pair
All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RdChkBits (OFF)	RD_CB7	168	S_A1:7	WrChkBits[4] (OFF)	WR_CB7	168	S_D1:7
	RD_CB6	167	S_A1:6		WR_CB6	167	S_D1:6
	RD_CB5	162	S_A1:5		WR_CB5	162	S_D1:5
	RD_CB4	161	S_A1:4		WR_CB4	161	S_D1:4
	RD_CB3	49	S_A1:3		WR_CB3	49	S_D1:3
	RD_CB2	48	S_A1:2		WR_CB2	48	S_D1:2
	RD_CB1	43	S_A0:7		WR_CB1	43	S_D0:7
	RD_CB0	42	S_A0:6		WR_CB0	42	S_D0:6
DataMsks (BIN)	DM7	232	M_A2:7	Strobes (HEX)	DQS7	114	M_A2:4
	DM6	223	M_A3:3		DQS6	105	M_A3:0
	DM5	211	M_A3:7		DQS5	93	M_D2:4
	DM4	202	M_C2:5		DQS4	84	M_D3:0
	DM3	155	M_C1:4		DQS3	37	M_C0:3
	DM2	146	M_D1:6		DQS2	28	M_D1:5
	DM1	134	M_D1:0		DQS1	16	M_D0:7
	DM0	125	M_D0:0		DQS0	7	M_D0:3
Address (Hex)	BA2	54	M_A1:4	Misc (OFF)	DDRCK2+/-	220/221	M_CK0
	BA1	190	M_E3:4		DDRCK1+/-	137/138	M_CK2
	BA0	71	M_D3:2		DDRCK0+/-	185/186	M_CK3
	A13	196	M_D2:2	Command (Sym)	S1#/GND	76	M_Q0
	A12	176	M_C1:6		S0#	193	M_C2:2
	A11	57	M_A1:2		RAS#	192	M_C2:3
	A10/AP	70	M_C3:2		CAS#	74	M_C2:0
	A9	177	M_C1:7		WE#	73	M_C2:1
	A8	179	M_A0:7				
	A7	58	M_A1:1				
	A6	180	M_A0:6				
	A5	60	M_A0:5				
	A4	61	M_ A0:4				
	A3	182	M_ A0:3				
	A2	63	M_ A0:1				
	A1	183	M_ A0:2				
	A0	188	M_ D3:6				

Table 2 – DDR2M-2A (400 Read and Write) TLA Channel Grouping (cont'd)

Notes:

All signals on this page are required for accurate post-processing of acquired data
The 'S' in front of a TLA channel denotes the Slave card of the merged pair
The 'M' in front of a TLA channel denotes the Master card of the merged pair
Signals in these groups are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
Ungrouped	ODT1/GND	77	M_D3:5	Ungrouped	CKE1	171	M_Q1
	ODT0	195	M_D2:3		CKE0	52	M_CK1
	RC0	55	M_A1:3		A15	173	M_C1:2
	SCL	120	M_A2:0		A14	174	M_C1:3
	SDA	119	M_ A2:1		A13	196	M_D2:2
	SA2	101	M_ A3:5		GND	18	M_D1:2
	SA1	240	M_ A2:2		A_DM8	164	M_C1:2
	SA0	239	M_ A2:3		B_DM8	164	M_C3:0
	NC_TEST	102	M_A3:4		DQS8	46	M_C0:7
	GND	19	M_D1:3		DQS8#	45	M_C0:6
	GND	68	M_C3:3		DQS7#	113	M_A2:5
	GND	112	M_A3:6		DQS6#	104	M_A3:1
	GND	135	M_D1:1		DQS5#	92	M_D2:5
	GND	147	M_D1:7		DQS4#	83	M_D3:1
	GND	165	M_C1:1		DQS3#	36	M_C0:2
	GND	203	M_C2:4		DQS2#	27	M_D1:4
	GND	224	M_A3:2		DQS1#	15	M_D0:6
	GND	233	M_A2:6		DQS0#	6	M_D0:2

Table 2 – DDR2M-2A (400 Read and Write) TLA Channel Grouping (cont'd)

Notes:

' # ' denotes a low-true signal
Signal names preceded by an asterisk (*) are required for accurate acquisition and post-processing of acquired data

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
A_DatHi	A_DQ63	236	S_ E2:0	A_DatLo	A_DQ31	159	S_A1:1
(Hex)	A_DQ62	235	S_ E2:1	(Hex)	A_DQ30	158	S_A1:0
	A_DQ61	230	S_ E2:2		A_DQ29	153	S_A0:3
	A_DQ60	229	S_ E2:3		A_DQ28	152	S_A0:2
	A_DQ59	117	S_ E2:4		A_DQ27	40	S_A0:5
	A_DQ58	116	S_ E2:5		A_DQ26	39	S_A0:4
	A_DQ57	111	S_ E3:0		A_DQ25	34	S_A0:1
	A_DQ56	110	S_ E3:1		A_DQ24	33	S_A0:0
	A_DQ55	227	S_E2:6		A_DQ23	150	S_C2:0
	A_DQ54	226	S_E2:7		A_DQ22	149	S_C2:1
	A_DQ53	218	S_ E3:4		A_DQ21	144	S_C2:2
	A_DQ52	217	S_E3:5		A_DQ20	143	S_C2:3
	A_DQ51	108	S_E3:2		A_DQ19	31	S_C2:4
	A_DQ50	107	S_E3:3		A_DQ18	30	S_C2:5
	A_DQ49	99	S_A2:2		A_DQ17	25	S_C3:0
	A_DQ48	98	S_A2:3		A_DQ16	24	S_C3:1
	A_DQ47	215	S_E3:6		A_DQ15	141	S_C2:6
	A_DQ46	214	S_E3:7		A_DQ14	140	S_C2:7
	A_DQ45	209	S_A2:6		A_DQ13	132	S_C3:2
	A_DQ44	208	S_A2:7		A_DQ12	131	S_C3:3
	A_DQ43	96	S_A2:0		A_DQ11	22	S_C3:4
	A_DQ42	95	S_A2:1		A_DQ10	21	S_C3:5
	A_DQ41	90	S_ A2:4		A_DQ9	13	M_E3:0
	A_DQ40	89	S_ A2:5		A_DQ8	12	M_E3:1
	A_DQ39	206	S_ A3:2		A_DQ7	129	S_C3:6
	A_DQ38	205	S_ A3:3		A_DQ6	128	S_C3:7
	A_DQ37	200	S_ A3:6		A_DQ5	123	M_E3:2
	A_DQ36	199	S_ A3:7		A_DQ4	122	M_E3:3
	A_DQ35	87	S_ A3:0		A_DQ3	10	M_E3:4
	A_DQ34	86	S_ A3:1		A_DQ2	9	M_E3:5
	A_DQ33	81	S_ A3:4		A_DQ1	4	M_E3:6
	A_DQ32	80	S_ A3:5		A_DQ0	3	M_E3:7

Table 3- DDR2M-2B (667 Read or Write) TLA Channel Grouping

Notes:

All signals on this page are required for accurate post-processing of acquired data
The ‘S’ in front of a TLA channel denotes the Slave card of the merged pair
The ‘M’ in front of a TLA channel denotes the Master card of the merged pair

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
B_DatHi	B_DQ63	236	S_ E0:0	B_DatLo	B_DQ31	159	S_D1:1
(Hex)	B_DQ62	235	S_ E0:1	(Hex)	B_DQ30	158	S_D1:0
	B_DQ61	230	S_ E0:2		B_DQ29	153	S_D0:3
	B_DQ60	229	S_ E0:3		B_DQ28	152	S_D0:2
	B_DQ59	117	S_ E0:4		B_DQ27	40	S_D0:5
	B_DQ58	116	S_ E0:5		B_DQ26	39	S_D0:4
	B_DQ57	111	S_ E1:0		B_DQ25	34	S_D0:1
	B_DQ56	110	S_ E1:1		B_DQ24	33	S_D0:0
	B_DQ55	227	S_E0:6		B_DQ23	150	S_C0:0
	B_DQ54	226	S_E0:7		B_DQ22	149	S_C0:1
	B_DQ53	218	S_ E1:4		B_DQ21	144	S_C0:2
	B_DQ52	217	S_E1:5		B_DQ20	143	S_C0:3
	B_DQ51	108	S_E1:2		B_DQ19	31	S_C0:4
	B_DQ50	107	S_E1:3		B_DQ18	30	S_C0:5
	B_DQ49	99	S_D2:2		B_DQ17	25	S_C1:0
	B_DQ48	98	S_D2:3		B_DQ16	24	S_C1:1
	B_DQ47	215	S_E1:6		B_DQ15	141	S_C0:6
	B_DQ46	214	S_E1:7		B_DQ14	140	S_C0:7
	B_DQ45	209	S_D2:6		B_DQ13	132	S_C1:2
	B_DQ44	208	S_D2:7		B_DQ12	131	S_C1:3
	B_DQ43	96	S_D2:0		B_DQ11	22	S_C1:4
	B_DQ42	95	S_D2:1		B_DQ10	21	S_C1:5
	B_DQ41	90	S_ D2:4		B_DQ9	13	M_E1:0
	B_DQ40	89	S_ D2:5		B_DQ8	12	M_E1:1
	B_DQ39	206	S_ D3:2		B_DQ7	129	S_C1:6
	B_DQ38	205	S_ D3:3		B_DQ6	128	S_C1:7
	B_DQ37	200	S_ D3:6		B_DQ5	123	M_E1:2
	B_DQ36	199	S_ D3:7		B_DQ4	122	M_E1:3
	B_DQ35	87	S_ D3:0		B_DQ3	10	M_E1:4
	B_DQ34	86	S_ D3:1		B_DQ2	9	M_E1:5
	B_DQ33	81	S_ D3:4		B_DQ1	4	M_E1:6
	B_DQ32	80	S_ D3:5		B_DQ0	3	M_E1:7

Table 3 – DDR2M-2B (667 Read or Write) TLA Channel Grouping (cont'd)

Notes:

All signals are required for accurate post-processing of acquired data
The 'S' in front of a TLA channel denotes the Slave card of the merged pair
The 'M' in front of a TLA channel denotes the Master card of the merged pair
All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
AChekBits (OFF)	A_CB7	168	S_A1:7	BchekBits [4] (OFF)	B_CB7	168	S_D1:7
	A_CB6	167	S_A1:6		B_CB6	167	S_D1:6
	A_CB5	162	S_A1:5		B_CB5	162	S_D1:5
	A_CB4	161	S_A1:4		B_CB4	161	S_D1:4
	A_CB3	49	S_A1:3		B_CB3	49	S_D1:3
	A_CB2	48	S_A1:2		B_CB2	48	S_D1:2
	A_CB1	43	S_A0:7		B_CB1	43	S_D0:7
	A_CB0	42	S_A0:6		B_CB0	42	S_D0:6
ADatMsks (BIN)	A_DM7	232	M_A2:7	BDatMsks [4] (BIN)	B_DM7	232	M_D2:7
	A_DM6	223	M_A3:3		B_DM6	223	M_D3:3
	A_DM5	211	M_A3:7		B_DM5	211	M_D3:7
	A_DM4	202	M_C2:5		B_DM4	202	M_C0:5
	A_DM3	155	M_C1:4		B_DM3	155	M_C2:4
	A_DM2	146	M_D1:6		B_DM2	146	M_A1:6
	A_DM1	134	M_D1:0		B_DM1	134	M_A1:0
	A_DM0	125	M_D0:0		B_DM0	125	M_D0:0
Address (Hex)	BA2	54	M_A1:4	Misc (OFF)	DDRCK2+/-	220/221	M_CK0
	BA1	190	M_E3:4		DDRCK1+/-	137/138	M_CK2
	BA0	71	M_D3:2		DDRCK0+/-	185/186	M_CK3
	A13	196	M_D2:2	Strobes (HEX)	DQS7	114	M_A2:4
	A12	176	M_C1:6		DQS6	105	M_A3:0
	A11	57	M_A1:2		DQS5	93	M_D2:4
	A10/AP	70	M_C3:2		DQS4	84	M_D3:0
	A9	177	M_C1:7		DQS3	37	M_C0:3
	A8	179	M_A0:7		DQS2	28	M_D1:5
	A7	58	M_A1:1		DQS1	16	M_D0:7
	A6	180	M_A0:6		DQS0	7	M_D0:3
	A5	60	M_A0:5	Command (Sym)	S1#/GND	76	M_Q0
	A4	61	M_ A0:4		S0#	193	M_C2:2
	A3	182	M_ A0:3		RAS#	192	M_C2:3
	A2	63	M_ A0:1		CAS#	74	M_C2:0
	A1	183	M_ A0:2		WE#	73	M_C2:1
	A0	188	M_ D3:6				

Table 3 – DDR2M-2B (667 Read or Write) TLA Channel Grouping (cont'd)

Notes:

All signals on this page are required for accurate post-processing of acquired data
The 'S' in front of a TLA channel denotes the Slave card of the merged pair
The 'M' in front of a TLA channel denotes the Master card of the merged pair
Signals in these groups are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
Ungrouped	ODT1/GND	77	M_D3:5	Ungrouped	CKE1	171	M_Q1
	ODT0	195	M_D2:3		CKE0	52	M_CK1
	RC0	55	M_A1:3		A15	173	M_C1:2
	SCL	120	M_A2:0		A14	174	M_C1:3
	SDA	119	M_ A2:1		A13	196	M_D2:2
	SA2	101	M_ A3:5		GND	18	M_D1:2
	SA1	240	M_ A2:2		A_DM8	164	M_C1:2
	SA0	239	M_ A2:3		B_DM8	164	M_C3:0
	NC_TEST	102	M_A3:4		DQS8	46	M_C0:7
	GND	19	M_D1:3		DQS8#	45	M_C0:6
	GND	68	M_C3:3		DQS7#	113	M_A2:5
	NC112	112	M_A3:6		DQS6#	104	M_A3:1
	NC126	126	M_D0:0		DQS5#	92	M_D2:5
	GND	135	M_D1:1		DQS4#	83	M_D3:1
	NC147	147	M_D1:7		DQS3#	36	M_C0:2
	GND	165	M_C1:1		DQS2#	27	M_D1:4
	GND	203	M_C2:4		DQS1#	15	M_D0:6
	GND	224	M_A3:2		DQS0#	6	M_D0:2
	GND	233	M_A2:6				

Table 3 – DDR2M-2B (667 Read or Write) TLA Channel Grouping (cont'd)

Notes:

' # ' denotes a low-true signal
Signal names preceded by an asterisk (*) are required for accurate acquisition and post-processing of acquired data

3.2 Display Groups not in Tables 1, 2 or 3

There are several groups in the List window that are not documented in the tables as these groups are used only by the post-processing display software. To ensure correct data display these groups must not be modified. These groups are:

DataHi
DataLo
ChekBits
DataMasks
MRSAddr

4.0 CLOCK SELECTION

There are three clocking option fields available when using the support packages. These select fields permit the user to setup the TLA acquisition as follows:

SDRAM Clocking: – Permits selecting the DDR Clock to be used to acquire data. Also allows user to use only Chip Select S0# or Chip Selects S0# and S1# for acquisition. The field choices are:

DDR CK0; S0~ only active (default)
DDR CK0; S0~ & S1~ active
DDR CK1; S0~ only active
DDR CK1; S0~ & S1~ active
DDR CK2; S0~ only active
DDR CK2; S0~ & S1~ active

Clock Mode – Allows the user to choose the kind of data acquisition that will be made:

Selective Clocking (default) - This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS# or CAS# is asserted low along with S0# or S1#. After every assertion of CAS# (with either S0# or S1#) a samples are taken during the next 17 DDR Clock cycles to ensure that all valid memory cycles have been acquired, then acquisition pauses and waits for the next Command. If CAS# and a Chip Select are asserted during these 17 clock cycles the count is reset. The 17-clock cycle value was determined by adding the maximum Burst Length, CAS Latency, Additive Latency and Registered Delay values together to determine worst case delay from Command to the last cycle containing valid data.

Every SDRAM Clock Edge – As the name implies this will cause the acquisition card to store data on every Rising and Falling edge of the selected SDRAM clock.

Refresh Cycles: – Permits choosing whether Refresh Cycles will be stored or not. The field choices are:

Do Not Acquire (default) **–** This mode will reduce the number of Refresh cycles stored by the acquisition card to provide optimum use of the acquisition memory.

Acquire – Refresh Cycles will be stored.

5.0 CONFIGURING FOR READ / WRITE DATA ACQUISITION

IMPORTANT !

Prior to configuring your NEX-NEXVUDDR667XU support package it is ***strongly*** recommended that Appendix A (“How DDR Data is Clocked”), section 5.2 (“Selecting DDR Read Sample Points”) and section 5.3 (“Selecting DDR Write Sample Points”) be read. This background information is very helpful in properly configuring the support.

5.1 Adjusting Input Thresholds for Proper Data Acquisition

The voltage threshold must be properly set on the TLA for proper acquisition of the DDR bus. We recommend that you verify the center point of the SDRAM Clock, any DDR strobe, and any DDR data bit. The CLK threshold should be set close to 0v because the clock is a differential signal. The threshold setting can be verified as correct by taking a TLA acquisition and verifying a 50% duty cycle on the clock by looking at the DDRCK2, DDRCK1 or DDRCK0 MagniVu trace. All other signals should be set close to the center of the voltage swing. Please note that synchronous acquisition using a TLA7AAx or TLA7ABx card requires a valid data window of approximately 625ps.

Although you should measure and set the thresholds as described, you can start with a 0.9V threshold value for all signals except for TLA CLK3, CLK1 and CLK0 which should be set to 0.07V because they are differential signals. These values can be used as a starting point.

5.2 Selecting DDRII Read Sample Points

For the NEX-NEXVUDDR667XU post-processing software packages to accurately show valid data it is necessary to choose the proper sample point to ensure that valid data is acquired when the software expects it. Since valid DDR2 Read data is straddled by the Strobes (see Figure 1) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Reads is determined by adding the Additive Latency value to the CAS Latency value, resulting in the total number of clock cycles from the Read Command to the first valid Read Data. (If these values are not known the technique described in Section 7.3 can be used to determine them.) In Figure 1 the total Read latency is 5 cycles.

The DDR2M-3A support acquires two samples of valid Read data on each rising edge of the DDR2 clock. So to acquire both pieces of data the RdA_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #1 in the Figure, and the RdB_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #2.

DDR2M-2A support clocks data from both the rising and falling edge of the DDR2 clock, so only Sample Pt. #1 needs to be used to set the sample point for the RDDatHi/Lo groups.

DDR2M-2B support clocks data in a similar fashion to the DDR2M-3A support in that only the DDR2 clock rising edge is used and two sample points are defined relative to that edge. However, the DDR2M-2B support differs in that only Read **or** Write data can be acquired – not both, so the user must decide in advance which data is of interest and set the A_DatHi/Lo and B_DatHi/Lo sample points appropriately.

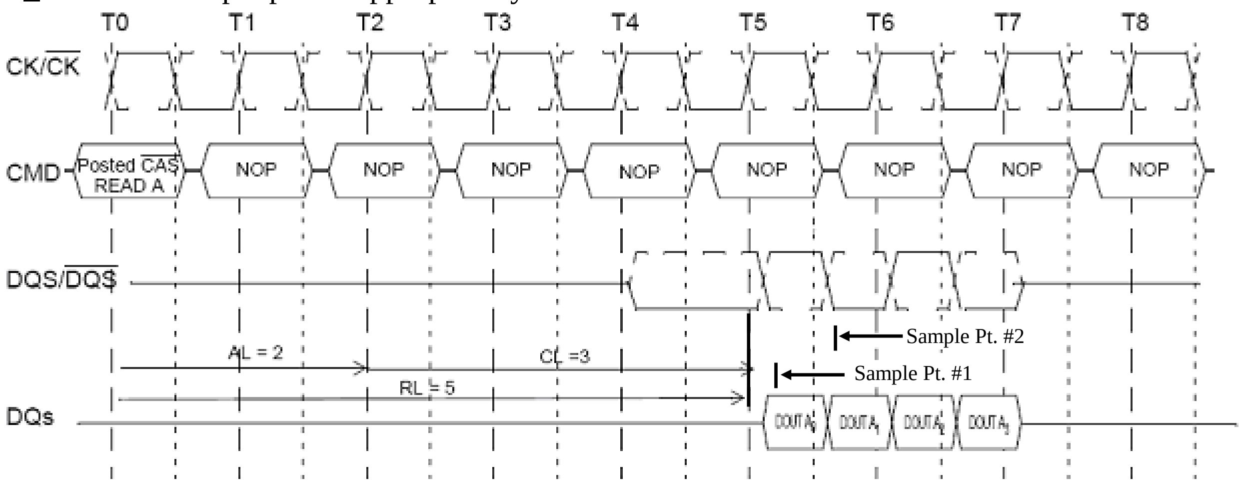


Figure 1- Read Cycle Latency = CAS Latency + Additive Latency (3+2=5 cycles)

5.3 Selecting DDRII Write Sample Points

Unlike valid DDR Read data, valid Write data is bisected by the Strobes. Since valid DDR2 Write data is bisected by the Strobes (see Figure 2) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Writes is determined by adding the Additive Latency value to the CAS Latency value and then subtracting one, resulting in the total number of clock cycles from the Write Command to the first valid Write Data. (If these values are not known the technique described in Section 7.3 can be used to determine them.) In Figure 2 the total Write latency is 4 cycles.

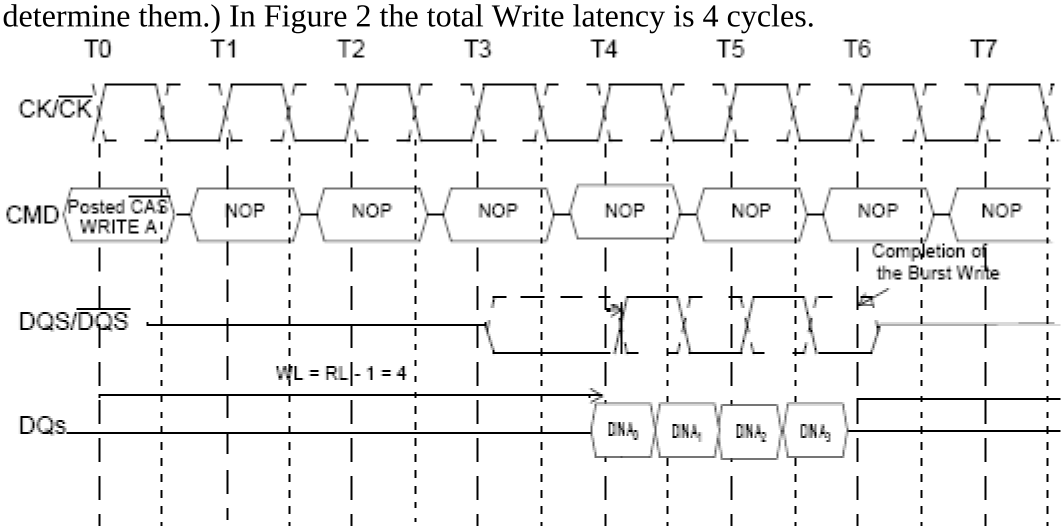


Figure 2- Write Cycle Latency = CAS Latency + Additive Latency -1 (3+2-1=4 cycles)

The DDR2M-3A support acquires two samples of valid Write data on each rising edge of the DDR2 clock. So to acquire both pieces of data the WrA_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #1 in the Figure, and the WrB_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #2.

DDR2M-2A support clocks data from both the rising and falling edge of the DDR2 clock, so only Sample Pt. #1 needs to be used to set the sample point for the WRDatHi/Lo groups.

DDR2M-2B support clocks data in a similar fashion to the DDR2M-3A support in that only the DDR2 clock rising edge is used and two sample points are defined relative to that edge. However, the DDR2M-2B support differs in that only Read **or** Write data can be acquired – not both, so the user must decide in advance which data is of interest and set the A_DatHi/Lo and B_DatHi/Lo sample points appropriately.

5.4 DDR2M-3A Support Setup

Using the DDR2M-3A support it is possible to acquire both Read and Write data by setting the sample point of the data groups appropriately. To adjust the Read Data group sample points first make an appropriate acquisition of either Read data by triggering on the cycle of interest. Then create a timing window display of MagniVu data and display the RdA_DatHi and RdA_DatLo 32-bit data groups, the individual Command group signals and the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2). A sample waveform display of MagniVu Read data is shown in Figure 3. To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (see Figure 3).

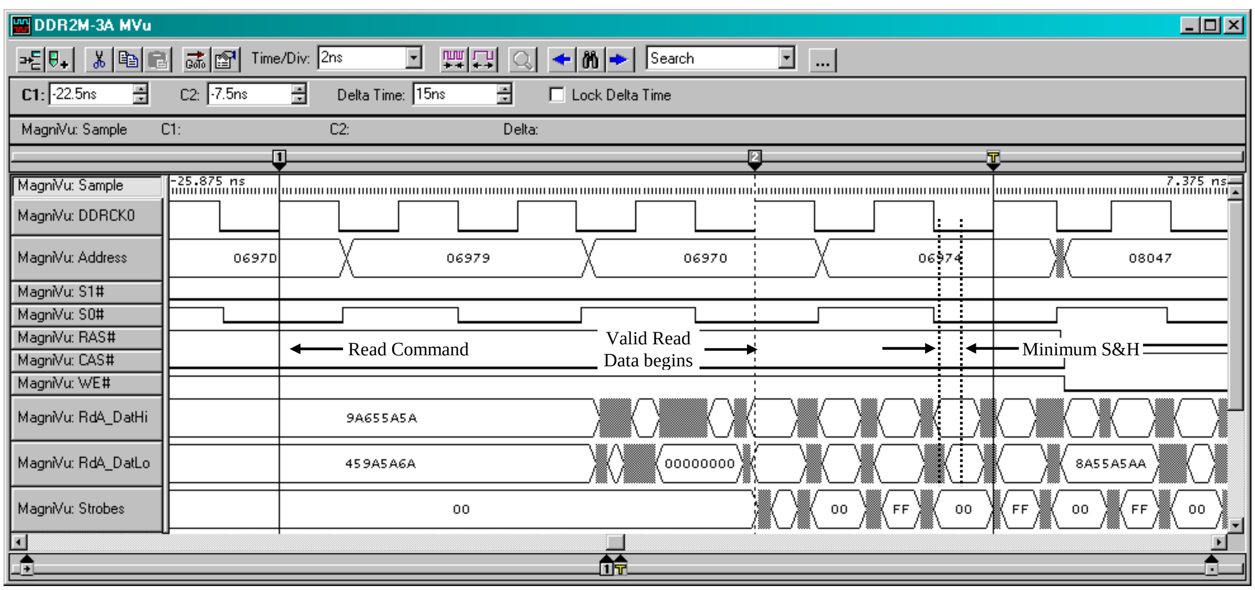


Figure 3- Locating Minimum Valid DDR2M-3A Read Data Window

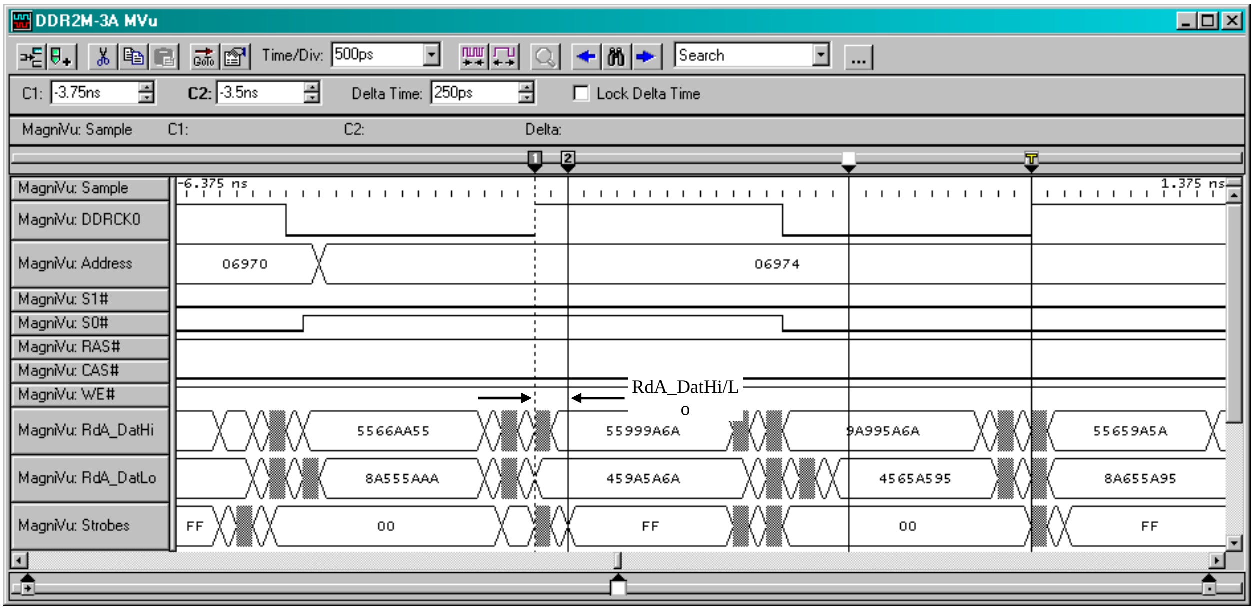


Figure 4- Measuring DDR2M-3A RdA_Dat/Hi/Lo Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 4) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is ~500ps, meaning that a suitable Setup & Hold value would be –500ps/1.125ns. Now the sample point for the RdB_DatHi and RdB_DatLo groups must be determined (see Figure 5). The next valid Read data (after the cycle measured above) occurs approximately 2.37ns after the rising edge of DDRCK0, so a suitable Setup & Hold value would be –2.375ns/3ns.

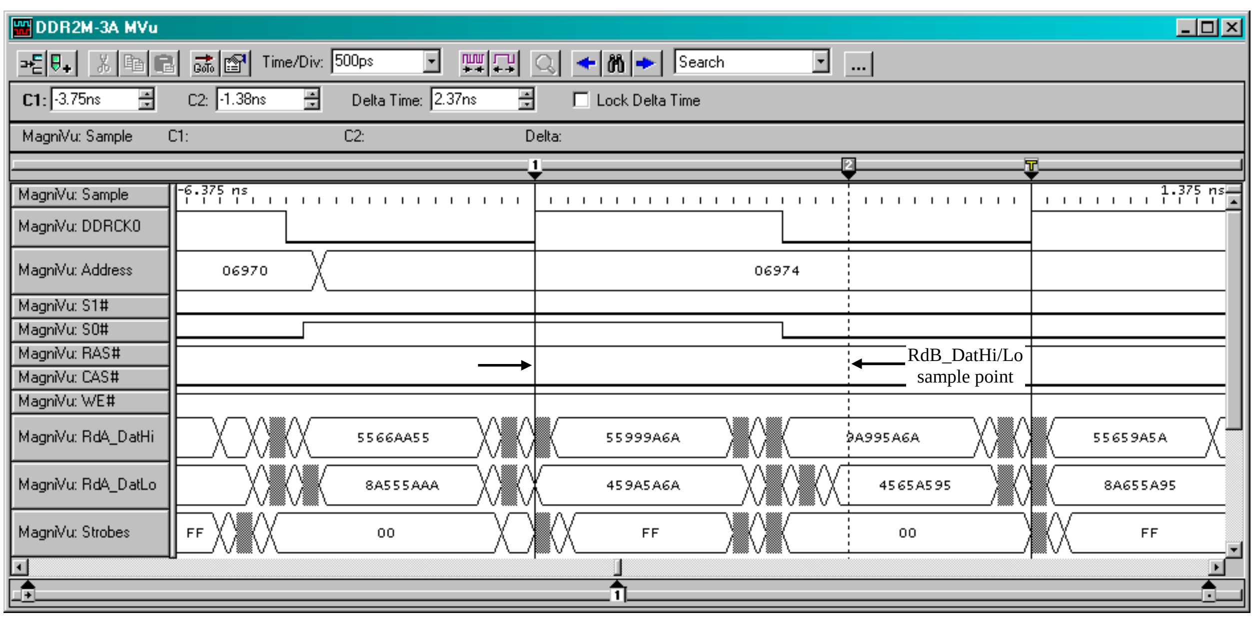


Figure 5- Measuring DDR2M-3A RdB_Dat/Hi/Lo Read Data Setup & Hold

Now the sample point positions must be set for the RdA_DatHi, RdA_DatLo, RdB_DatHi and RdB_DatLo groups in the Setup window. This window is found by going to the LA Card's Setup window, then clicking on the More button to the right of the clock select field. The TLA acquisition cards require a valid data window of 625ps, and this window can be placed to begin from 16.25ns prior to the clock edge to 7.625ns after the edge in 125ps increments. Each 32-bit data group (RdA_DatHi, RdA_DatLo, RdB_DatHi, RdB_DatLo) will require its own value programmed from the measurements noted in the MagniVu window (Figure 6).

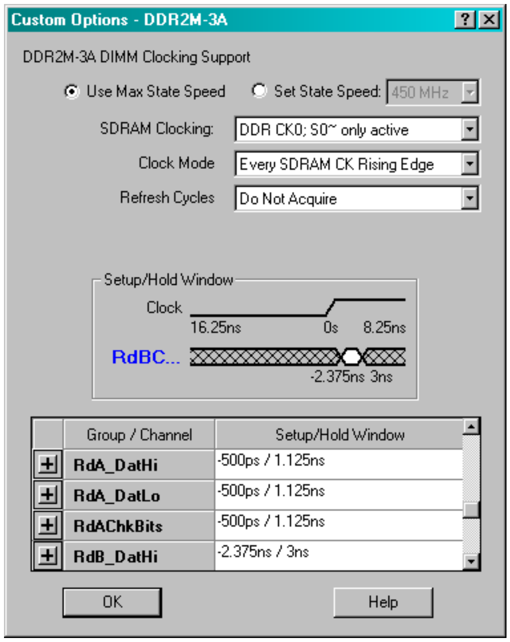


Figure 6- Setting DDR2M-3A RdA_DatHi/Lo and RdB_DatHi/Lo Sample Points

Setting the Setup & Hold values for acquiring Write data is a similar process. To determine the Write Data group sample points first make an appropriate acquisition of Write data by triggering on a Write Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups RdA_DatHi, and RdA_DatLo along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2).

Note: Because of the method used to acquire Write Data using the DDR2M-3A support, the MagniVu data from the RdA_DatHi/Lo data groups must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A "How DDR Data is Clocked".

A sample waveform display of MagniVu Write data is shown in Figure 7. To determine the sample point, locate the worst-case Setup & Hold timing of valid Write data during the acquired burst (note arrows in Figure 7). Refer to section 5.3 for important information on properly determining the Write data sample points.

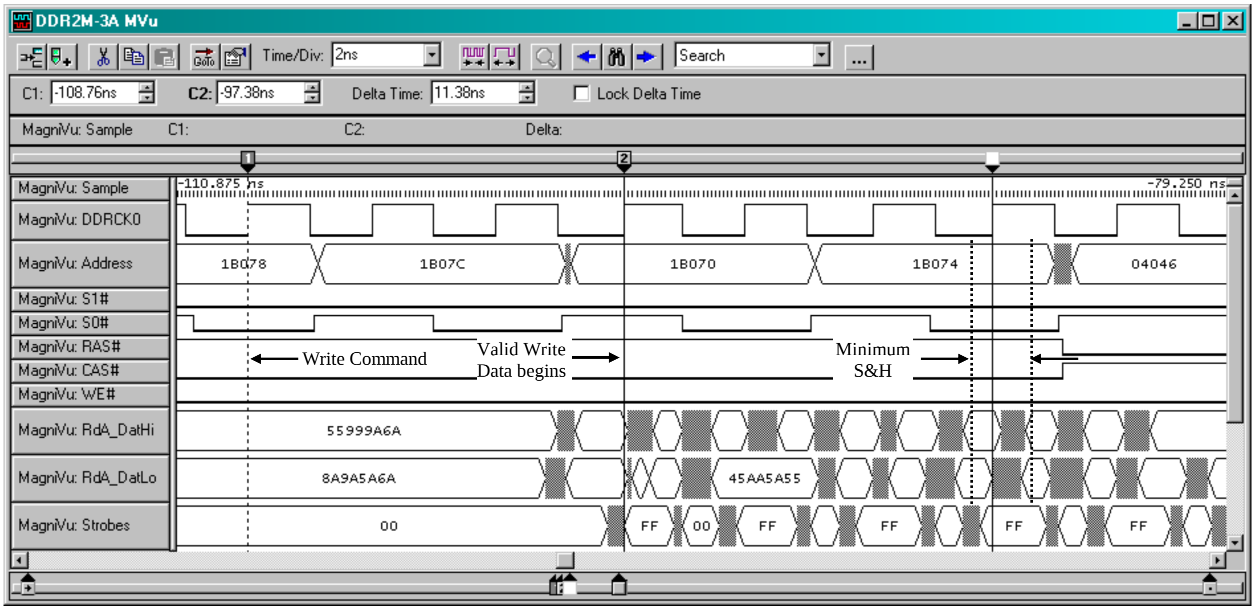


Figure 7- Locating Minimum Valid DDR2M-3A Write Data Window

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 8) and use the cursors to measure the time from the clock edge to the start of valid Write data. In this example the delay from edge to stable data transition is ~750ps, meaning that a suitable Setup & Hold value would be 750ps/-125ps.

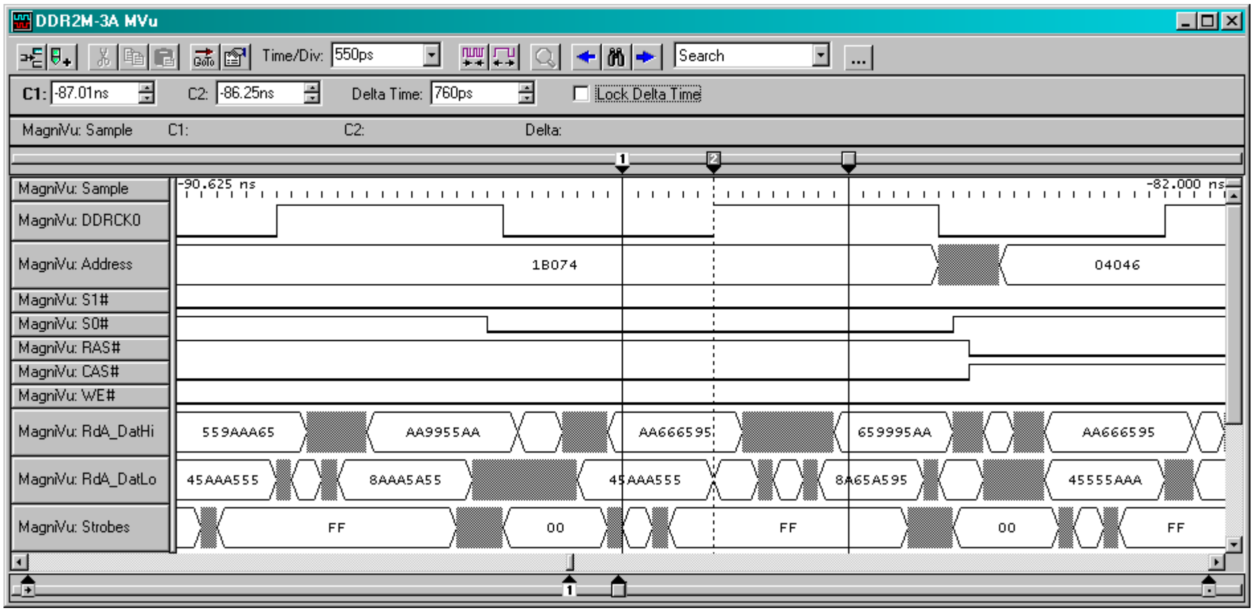


Figure 8- Measuring DDR2M-3A WrA_Dat/Hi/Lo Write Data Setup & Hold

Now the sample point for the WrB_DatHi and WrB_DatLo groups must be determined (see Figure 9). The next valid Write data (after the cycle measured above) occurs approximately 1.12ns after the rising edge of DDRCK0, so a suitable Setup & Hold value would be -1.125ns/1.750ns.

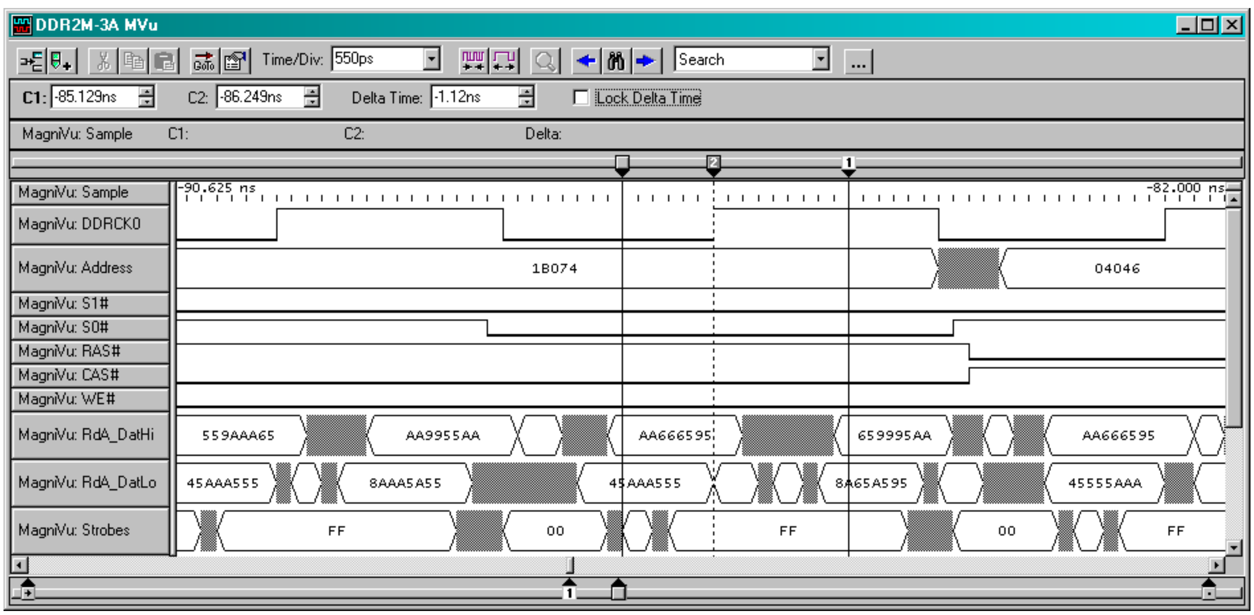


Figure 9- Measuring DDR2M-3A WrB_Dat/Hi/Lo Write Data Setup & Hold

The sample point positions must now be set for the WrA_DatHi, WrA_DatLo, WrB_DatHi, WrB_DatLo groups in the Setup window (Figure 10). Note that the WrtMasks group should have a Setup & Hold value that matches that of the Write Data groups.

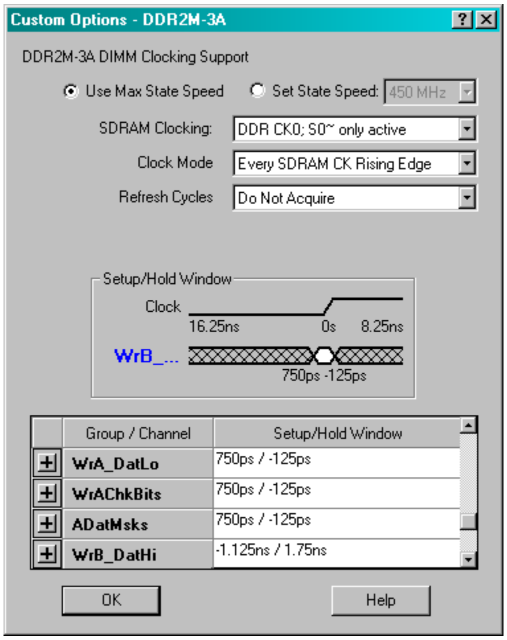


Figure 10- Setting DDR2M-3A WrA_DatHi/Lo and WrB_DatHi/Lo Sample Points

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 11 shows some of these additional data groups (RdADatB7-0) added to the same Waveform display shown in Figure 9. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see Figure 12). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit groups make up a 32-bit group.

Note: Again, it is very important to remember that, because of the method used to acquire Write Data using the DDR2M-3A support, the MagniVu data from the RdA_DatHi/Lo data groups must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A "How DDR Data is Clocked".

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (RdADatHi, RdADatLo, RdBDatHi, RdBDatLo, WrADatHi, WrADatLo, WrBDatHi, WrBDatLo) be reset to "Support Package Default". This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values – 625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

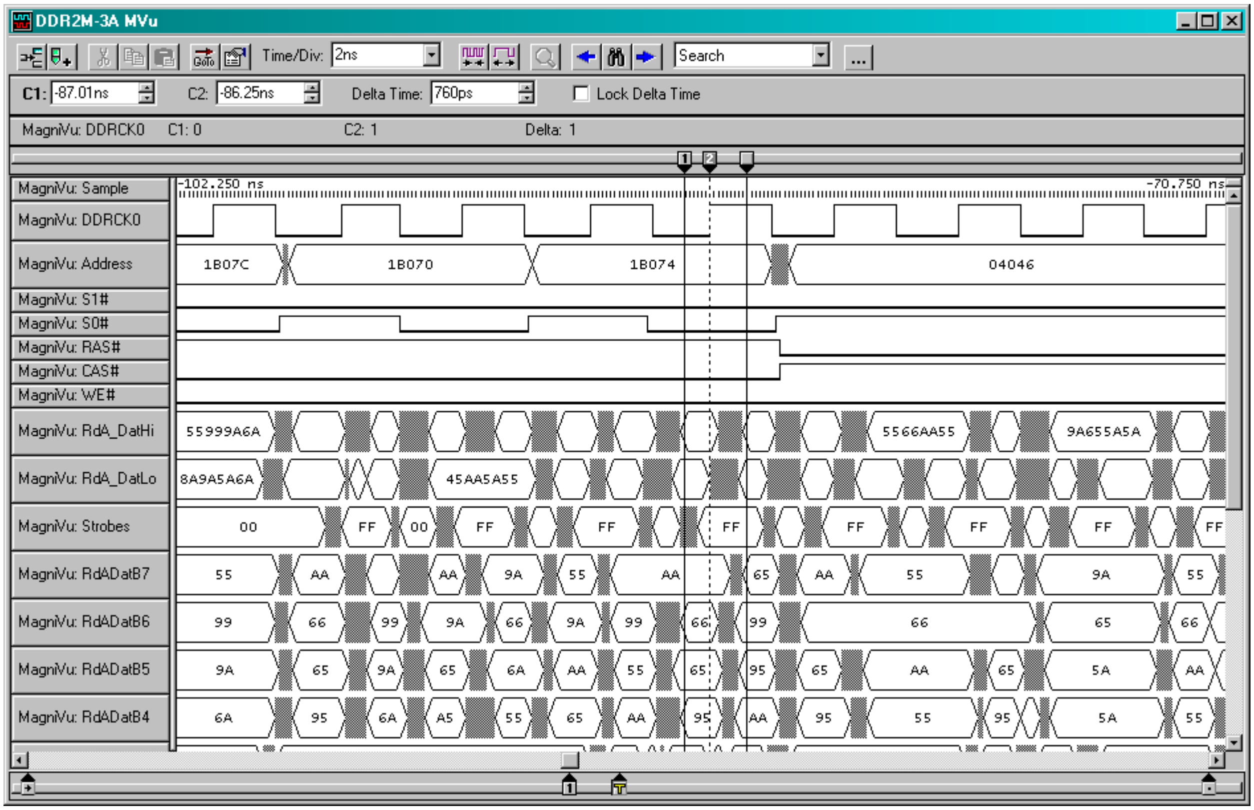


Figure 11- Viewing Individual 8-bit Read Data Groups

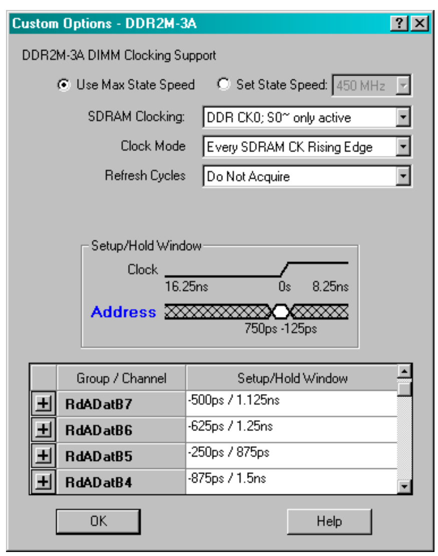


Figure 12- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

Note: Values shown are for illustration purposes only

5.5 DDR2M-2A Support

The DDR2M-2A support will acquire both Read and Write data on DDR2 targets running at up to 400MT/s. This support requires the same setup steps as those outlined in the DDR2M-3A setup (see section 5.4). However, instead of programming 8 data groups it is now necessary to program the sample windows for only four 32-bit data groups because Read and Write data are acquired on both the rising and falling edges of the DDR Clock rather than just the clock's rising edge as in the DDR2M-3A support.

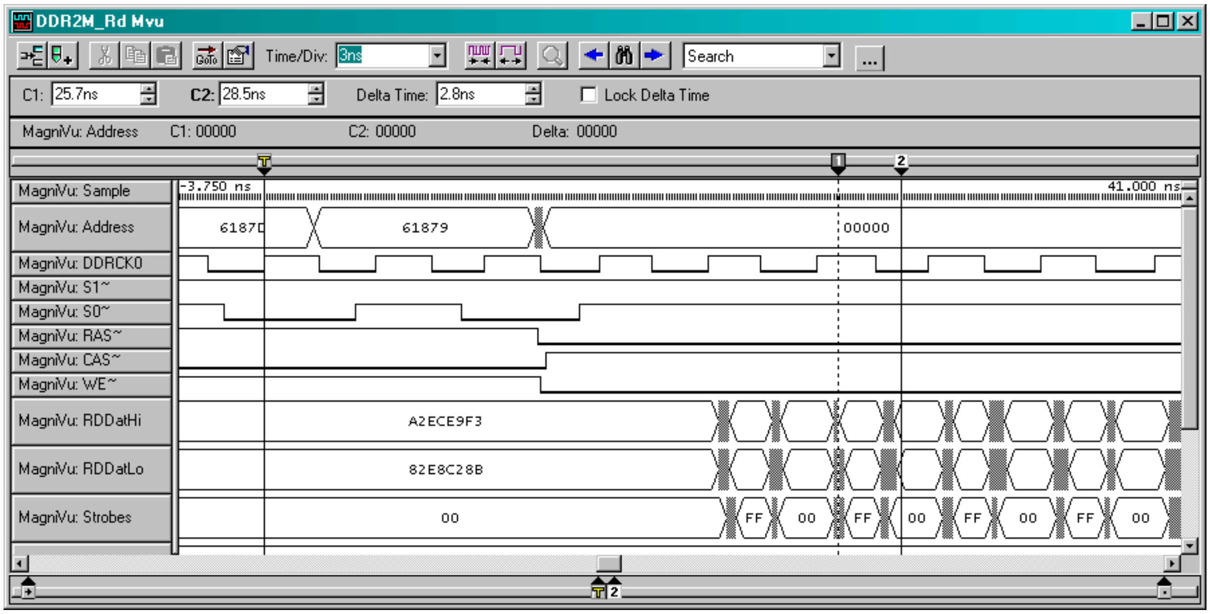


Figure 13- Locating Minimum Valid DDR2M-2A Read Data Window

To adjust the Read Data group sample points first make an appropriate acquisition of Read data by triggering on a Read Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2). A sample waveform display of MagniVu Read data is shown in Figure 13. To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (note arrows in Figure 13).

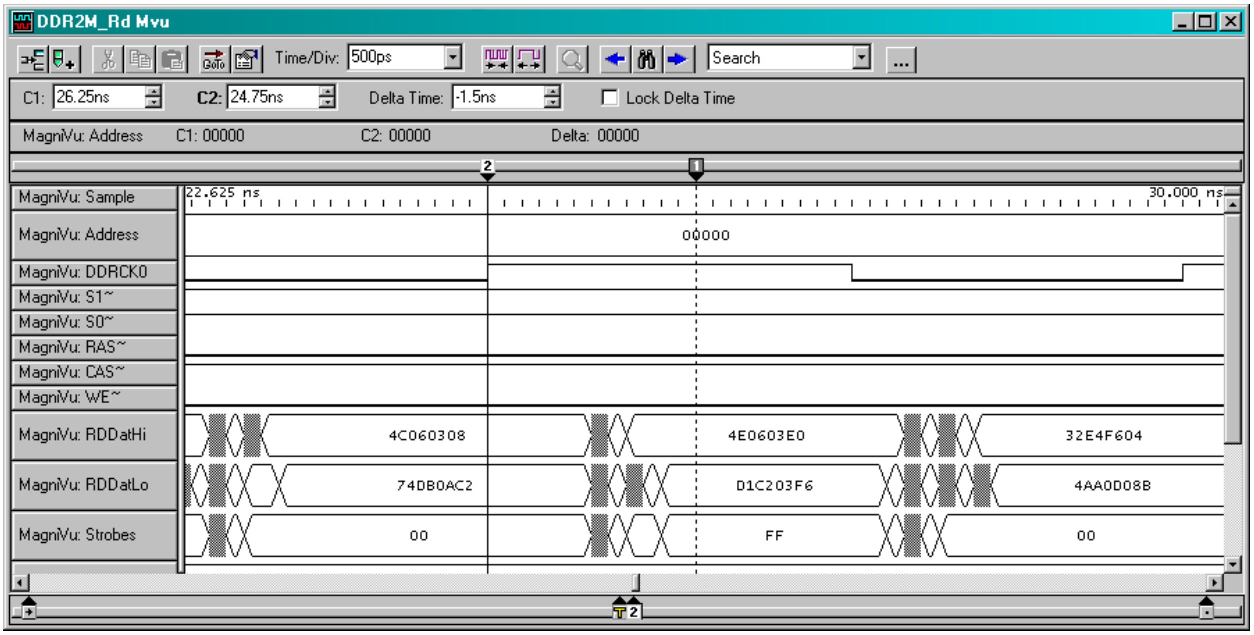


Figure 14- Measuring DDR2M-2A Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 14) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is ~1.5ns, meaning that a suitable Setup & Hold value would be –1.5ns/2.125ns. This sample point position must now be set for the RDDatHi and RDDatLo groups in the Setup window. This window is found by going to the LA Card's Setup window, then clicking on the **More** button to the right of the clock select field. The TLA acquisition cards require a valid data window of 625ps, and this window can be placed to begin from 16.25ns prior to the clock edge to 7.625ns after the edge in 125ps increments. Each 32-bit data group (RDDatHi and RDDataLo) will require its own value programmed from the measurements noted in the MagniVu window (Figure 15).

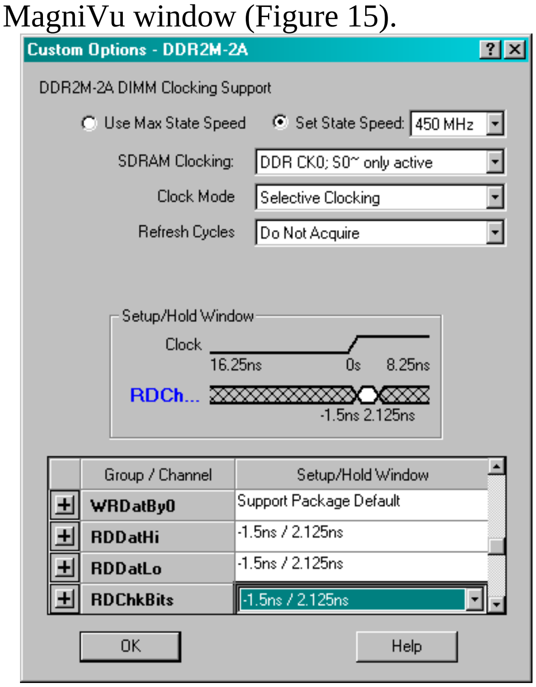


Figure 15- Setting DDR2M-2A Read Data Setup & Hold Sample Points

Setting the Setup & Hold values for acquiring Write data is similar, but the valid sample point now more closely aligns with the Strobe edges. To adjust the Write Data group sample points first make an appropriate acquisition of Write data by triggering on a Write Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups (RDDatHi and RDDatLo) along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2).

Note: Because of the method used to acquire Write Data using the DDR2M-2A support the MagniVu data from the RDDatHi/Lo data groups must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A "How DDR Data is Clocked".

A sample waveform display of MagniVu Write data is shown in Figure 16. To determine the sample point, locate the worst-case Setup & Hold timing of valid Write data during the acquired burst (note arrows in Figure 16). Refer to section 5.3 for important information on properly determining the Write data sample points.

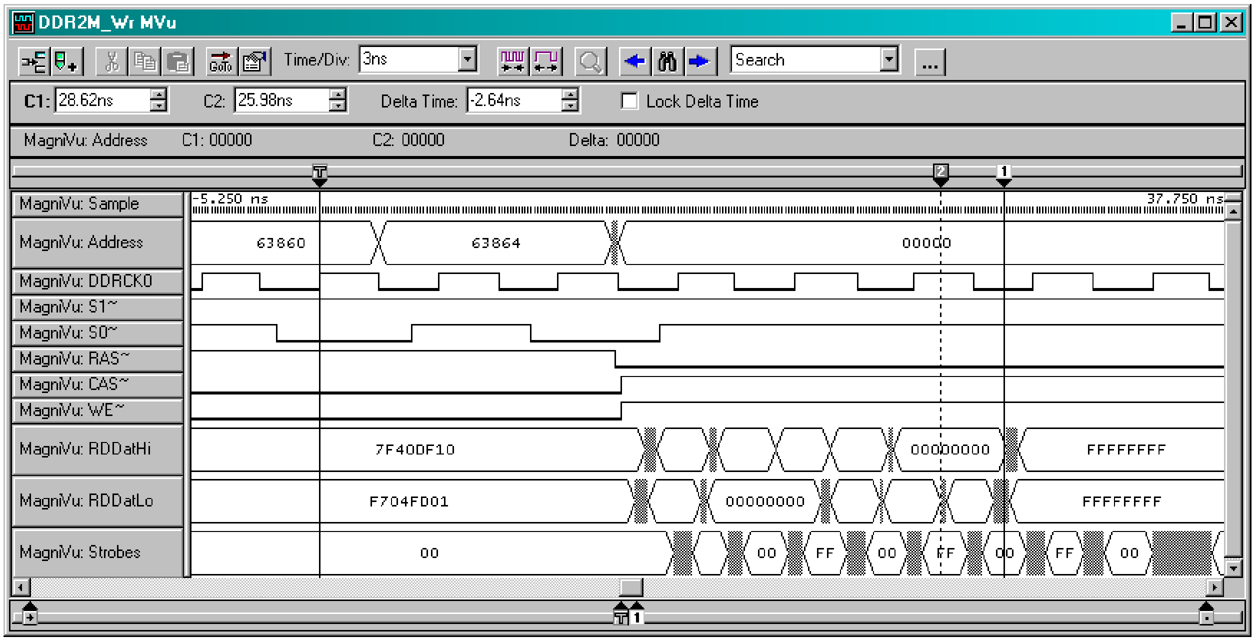


Figure 16- Locating Minimum Valid DDR2M-2A Write Data Window

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 17) and use the cursors to measure the time from the clock edge to the start of valid Write data. In this example the delay from edge to Strobe transition is ~1ns, meaning that a suitable Setup & Hold value would be 1ns/-375ps. This sample point position must now be set for the WRDatHi and WRDatLo groups in the Setup window (Figure 18). Note that the WrtMasks group should have a Setup & Hold value that aligns with the transition of the Strobes.

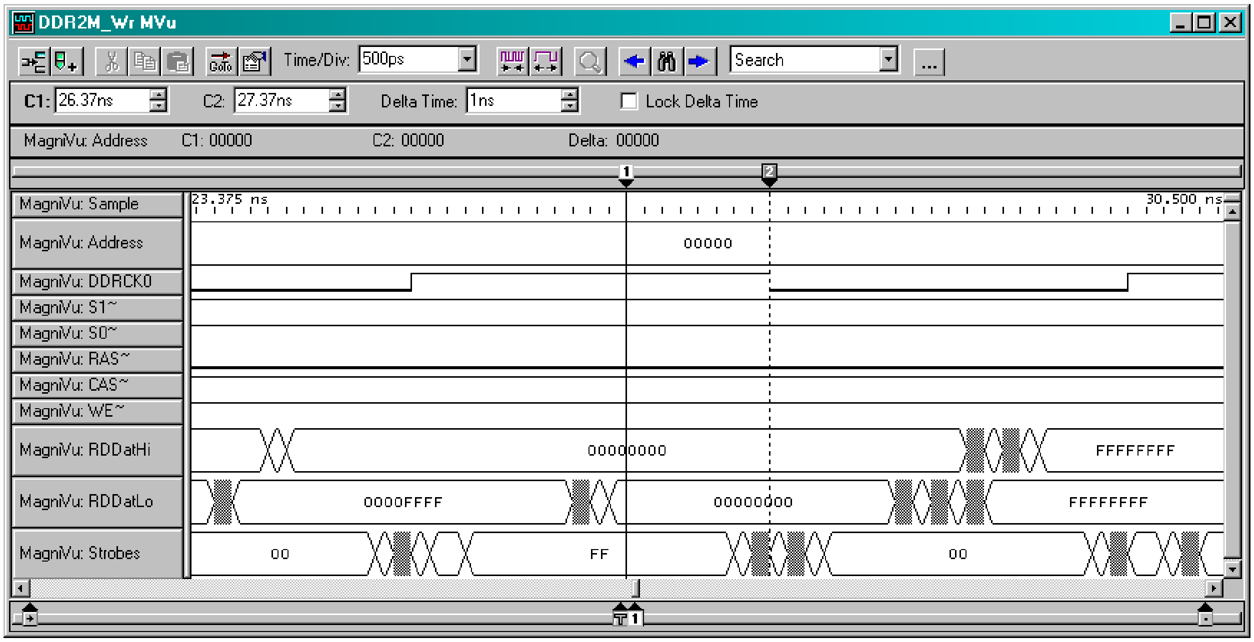


Figure 17- Measuring DDR2M-2A Write Data Setup & Hold

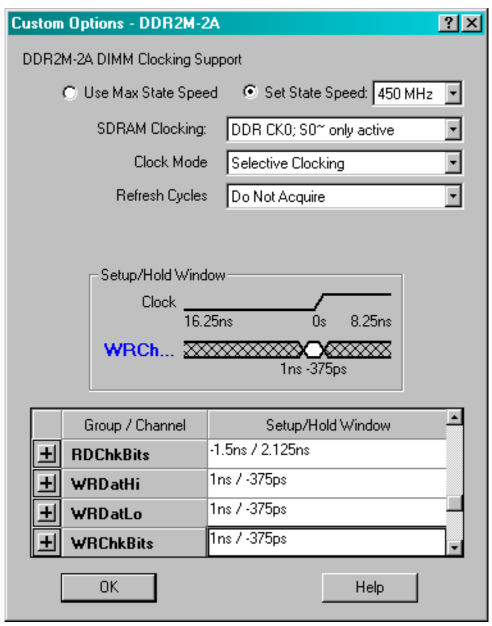


Figure 18- Setting DDR2M-2A Write Data Setup & Hold Sample Points

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 19 shows these added data groups (DatByte7-0) added to the same Waveform display shown in Figure 16. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see Figure 20). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit groups make up a 32-bit group.

Note: Again, it is very important to remember that, because of the method used to acquire Write Data using the DDR2M-2A support, the Read Data group information must be used to determine the Write Data sample points. For further explanation of this process refer to Appendix A "How DDR Data is Clocked".

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (RDDatHi, RDDatLo, WRDatHi or WRDatLo) be reset to "Support Package Default". This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values: 625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

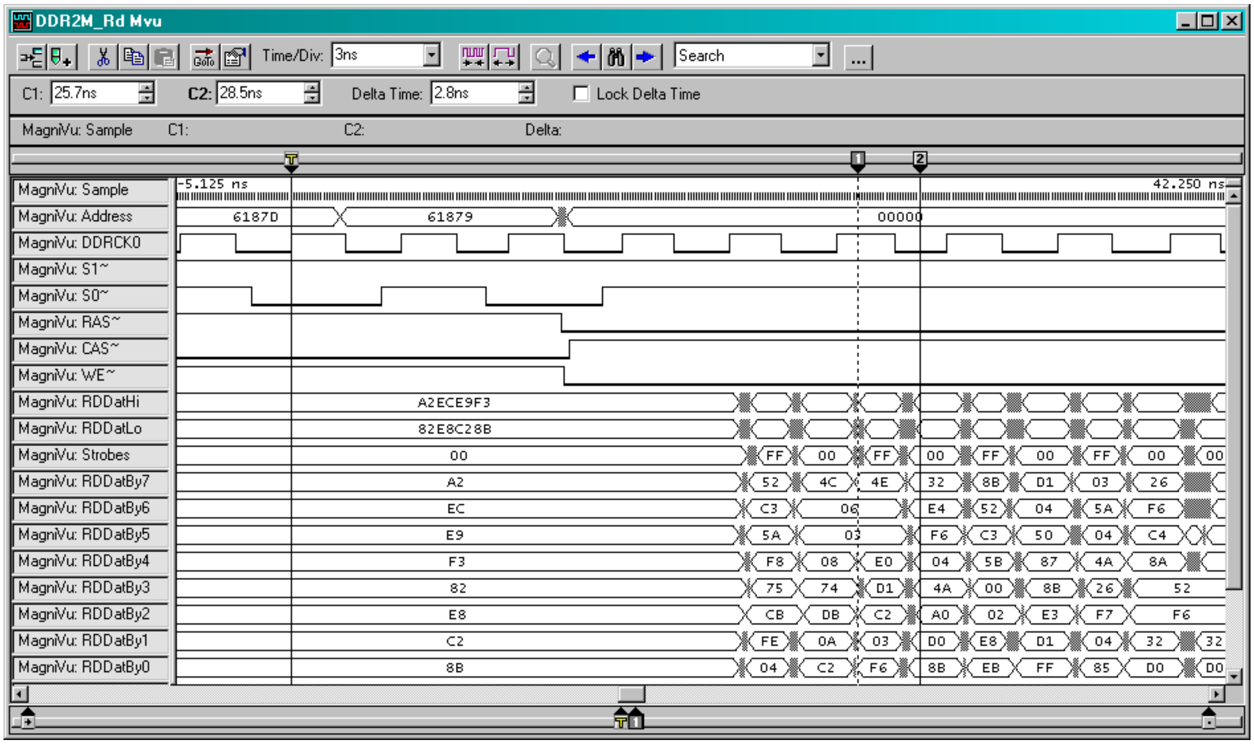


Figure 19- Viewing Individual 8-bit Read Data Groups

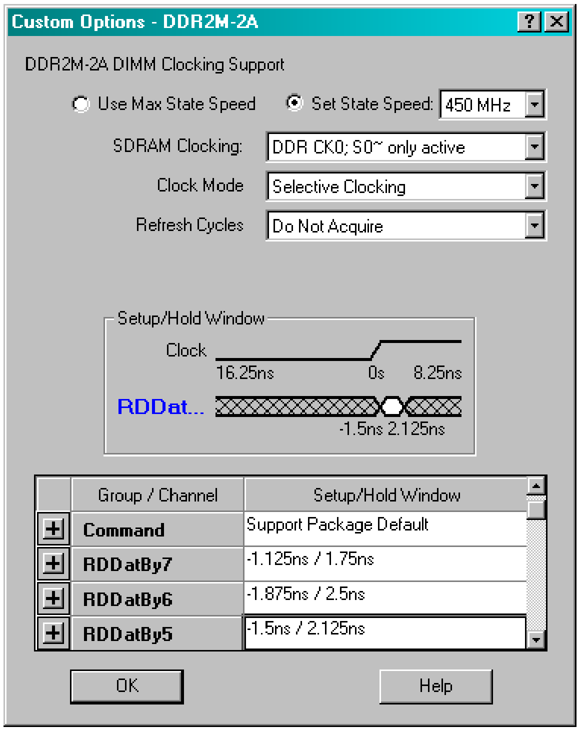


Figure 20- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

Note: Values shown are for illustration purposes only

5.6 DDR2M-2B Support

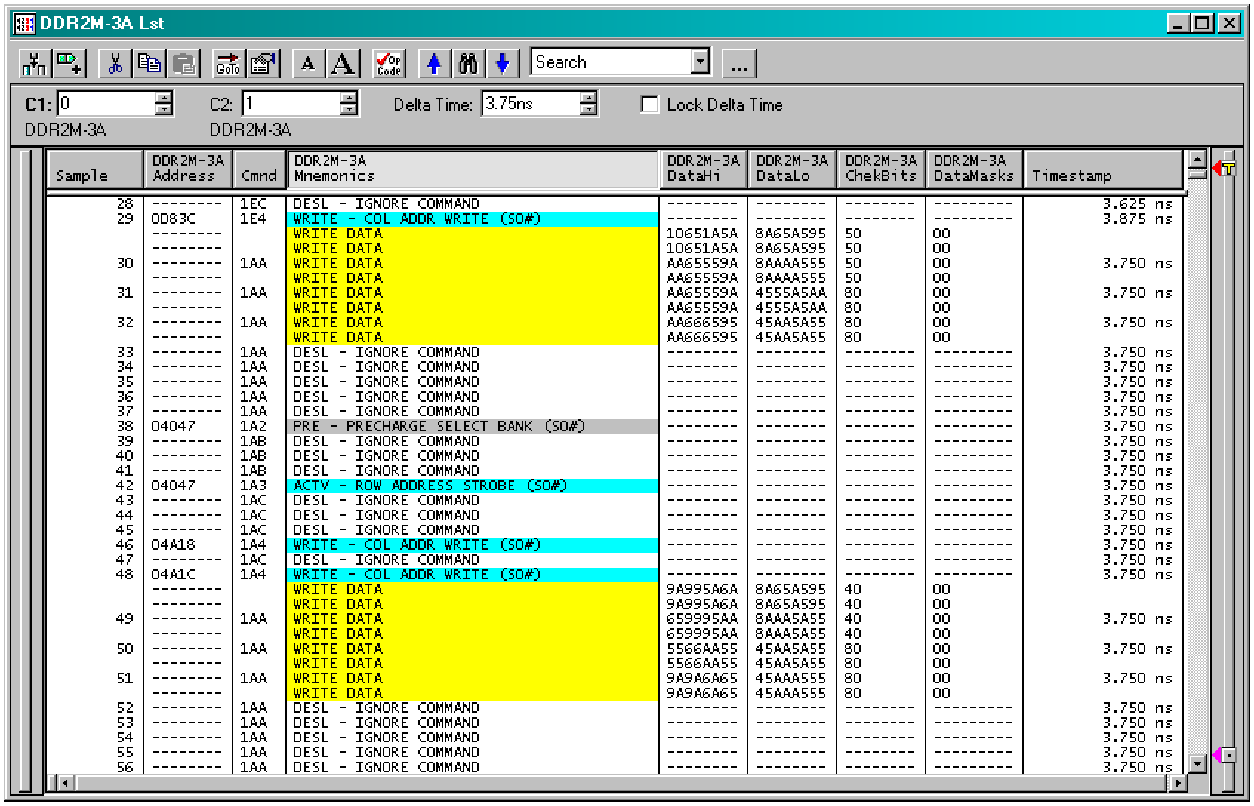
Using the DDR2M-2B support it is possible to acquire either Read or Write data from a 667MT/s target by moving the sample point of the data groups appropriately. Follow the instructions given for setting up DDR2M-3A support but choose whether to acquire Read or Write data by setting the data group sample points appropriately. Sample points will need to be set for the A_DatHi, A_DatLo, B_DatHi and B_DatLo data groups. Note that MagniVu data will only be valid on the A_DatHi/Lo data groups.

6.0 VIEWING DATA

6.1 Viewing NEX-NEXVuDDR667xU Data

When using the NEX-NEXVuDDR667xU support packages the raw Address and Data groups are suppressed and are replaced with post-processed data in new groups. This data is displayed in new groups that have the support package name preceding it (i.e., DDR2M-3A Address, DDR2M-3A DataHi, etc.). The raw data groups are suppressed so that the display of data can be done in a more user-friendly fashion.

The Command group is suppressed because its function is replaced with a column labeled "DDR2M-3A Mnemonics", "DDR2M-2A Mnemonics" or "DDR2M-2B Mnemonics". The NEX-NEXVuDDR667xU support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 21 shows the default DDR2M-3A display where all DDR data is displayed.



Sample	DDR2M-3A Address	Cmnd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChekBits	DDR2M-3A DataMasks	Timestamp
28	--------	1EC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.625 ns
29	0D83C	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	3.875 ns
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
30	--------	1AA	WRITE DATA	AA65559A	8AAAA555	50	00	3.750 ns
	--------		WRITE DATA	AA65559A	8AAAA555	50	00	
31	--------	1AA	WRITE DATA	AA65559A	4555A5AA	80	00	3.750 ns
	--------		WRITE DATA	AA65559A	4555A5AA	80	00	
32	--------	1AA	WRITE DATA	AA666595	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	AA666595	45AA5A55	80	00	
33	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
34	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
35	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
36	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
37	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
38	04047	1A2	PRE - PRECHARGE SELECT BANK (S0#)	--------	--------	--------	---------	3.750 ns
39	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
40	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
41	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
42	04047	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	3.750 ns
43	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
44	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
45	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	3.750 ns
47	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	3.750 ns
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
49	--------	1AA	WRITE DATA	659995AA	8AAA5A55	40	00	3.750 ns
	--------		WRITE DATA	659995AA	8AAA5A55	40	00	
50	--------	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	5566AA55	45AA5A55	80	00	
51	--------	1AA	WRITE DATA	9A9A6A65	45AAA555	80	00	3.750 ns
	--------		WRITE DATA	9A9A6A65	45AAA555	80	00	
52	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
53	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
54	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
55	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
56	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns

Figure 21- DDR2M-3A State Display

To change the display it is necessary to bring up the window's Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in Figure 22.

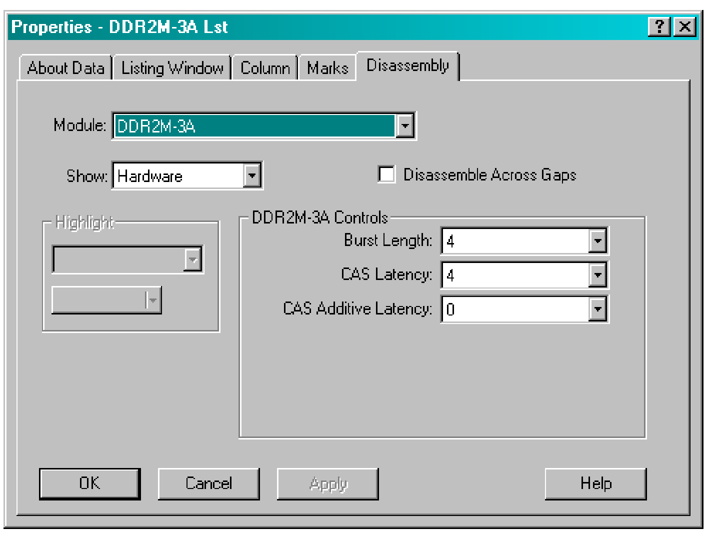


Figure 22- Disassembly Properties

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

Valid Cycles - (DDR2M-2B only) - tells the post-processing software whether the DDR2M-2B support was configured to acquire valid Read or Write data.

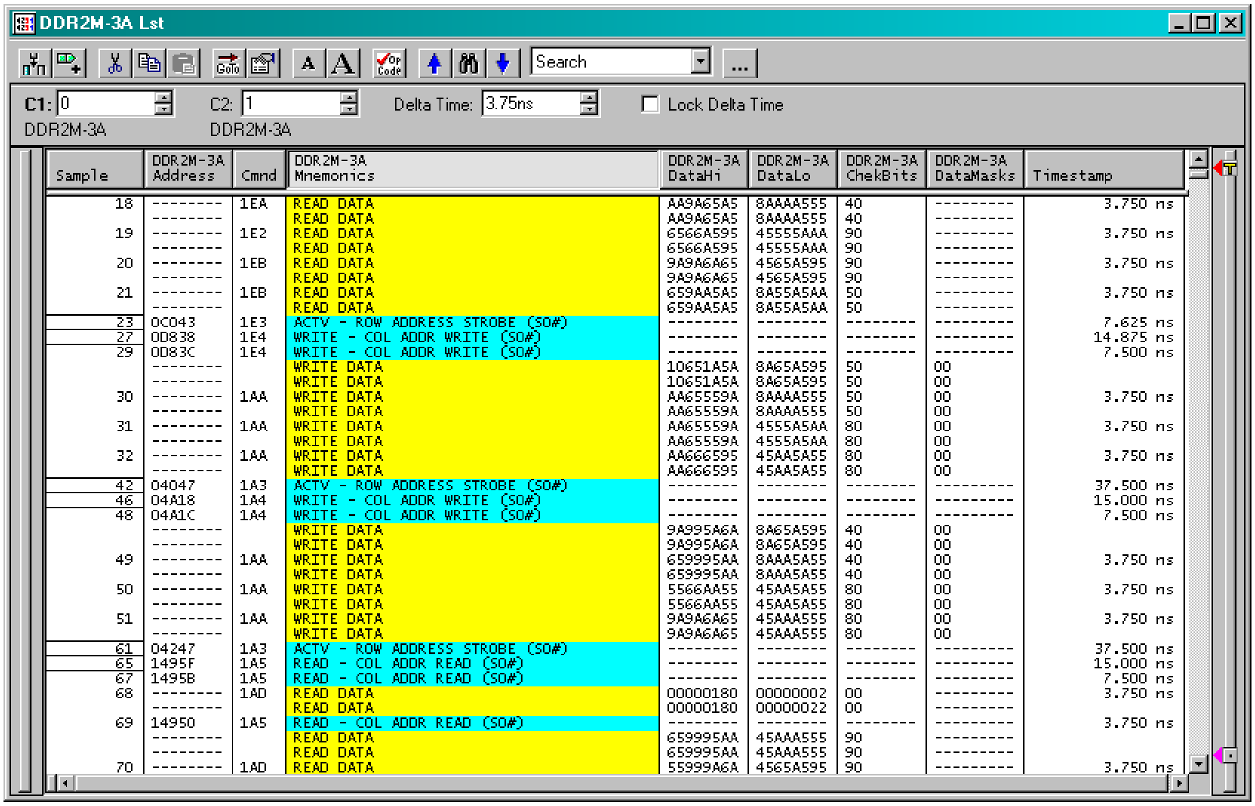
Burst Length – permits setting the burst length for Read and Write data. Valid choices are 4 (the default) and 8. This value must be set properly for all valid Read and Write data to be displayed.

CAS Latency – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 2 (default), 3, 4, or 5 cycles.

CAS Additive Latency – additional latency for data cycles. This value must also be set properly for valid Read and Write Data to be displayed. Valid choices are 0 (default), 1, 2, 3, or 4 cycles.

In addition to these Disassembly Properties selections, changing the settings in the **Show** field results in display changes as well:

> **Hardware –** (default) displays all acquired cycles
>
> **Software –** suppresses all idle or wait cycles
>
> **Control Flow –** shows Address Command and valid Read / Write data cycles
>
> **Subroutine –** shows valid Read / Write data cycles only



Sample	DDR2M-3A Address	Cmnd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChekBits	DDR2M-3A DataMasks	Timestamp
18	--------	1EA	READ DATA	AA9A65A5	8AAAA555	40	---------	3.750 ns
	--------		READ DATA	AA9A65A5	8AAAA555	40	---------	
19	--------	1E2	READ DATA	6566A595	45555AAA	90	---------	3.750 ns
	--------		READ DATA	6566A595	45555AAA	90	---------	
20	--------	1EB	READ DATA	9A9A6A65	4565A595	90	---------	3.750 ns
	--------		READ DATA	9A9A6A65	4565A595	90	---------	
21	--------	1EB	READ DATA	659AA5A5	8A55A5AA	50	---------	3.750 ns
	--------		READ DATA	659AA5A5	8A55A5AA	50	---------	
23	0C043	1E3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	7.625 ns
27	0D838	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	14.875 ns
29	0D83C	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	7.500 ns
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
30	--------	1AA	WRITE DATA	AA65559A	8AAAA555	50	00	3.750 ns
	--------		WRITE DATA	AA65559A	8AAAA555	50	00	
31	--------	1AA	WRITE DATA	AA65559A	4555A5AA	80	00	3.750 ns
	--------		WRITE DATA	AA65559A	4555A5AA	80	00	
32	--------	1AA	WRITE DATA	AA666595	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	AA666595	45AA5A55	80	00	
42	04047	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	37.500 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	15.000 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	7.500 ns
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
49	--------	1AA	WRITE DATA	659995AA	8AAA5A55	40	00	3.750 ns
	--------		WRITE DATA	659995AA	8AAA5A55	40	00	
50	--------	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	5566AA55	45AA5A55	80	00	
51	--------	1AA	WRITE DATA	9A9A6A65	45AAA555	80	00	3.750 ns
	--------		WRITE DATA	9A9A6A65	45AAA555	80	00	
61	04247	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	37.500 ns
65	1495F	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	15.000 ns
67	1495B	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	7.500 ns
68	--------	1AD	READ DATA	00000180	00000002	00	---------	3.750 ns
	--------		READ DATA	00000180	00000022	00	---------	
69	14950	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	3.750 ns
	--------		READ DATA	659995AA	45AAA555	90	---------	
	--------		READ DATA	659995AA	45AAA555	90	---------	
70	--------	1AD	READ DATA	55999A6A	4565A595	90	---------	3.750 ns

Figure 23- DDR2M-3A State Display- Control Flow

Changing the Show field setting in the display of Figure 21 from Hardware to Control Flow results in the display of Figure 23 where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

6.2 Viewing Raw DDR2 Data

In order to make the display of DDR2 data more user-friendly the raw data from the Address, all Data and other groups is suppressed in the Listing display. Instead the post-processing display software formats and reorders the data to tag and display valid DDR2 Address, Commands and Data. In the case of the DDR2M-3A support, which stores two Read and two Write data cycles in each TLA Sample location, the data is reordered chronologically in the display with the oldest data being shown on the line above the newer data.

To see the raw data using any of the NEX-NEXVuDDR667xU support packages perform a right mouse click in the Listing window, select **Add Column…** then click on the group to be added. Refer to the TLA User's Manual or online help for further information on added or deleting data groups.

6.3 DDR2M-3A / -2A / -2B Mnemonics Description

Table 4 gives a brief description of each of the text lines displayed in the post-processing software display.

Mnemonic	Description
ACTV - ROW ADDRESS STROBE (S0~)	Active command – activate a row in a bank for subsequent access (chip select 0)
ACTV - ROW ADDRESS STROBE (S1~)	Active command – activate a row in a bank for subsequent access (chip select 1)
BST - BURST STOP (S0~)	Burst Terminate command – truncate current Read burst (chip select 0)
BST - BURST STOP (S1~)	Burst Terminate command – truncate current Read burst (chip select 1)
DESL - IGNORE COMMAND	Deselect function – no new command
MRS - MODE REGISTER SET (S0~)	Mode Register Set command – mode register load (chip select 0)
MRS - MODE REGISTER SET (S1~)	Mode Register Set command – mode register load (chip select 1)
NOP - NO OPERATION (S0~)	No Operation command (chip select 0)
NOP - NO OPERATION (S1~)	No Operation command (chip select 1)
PRE - PRECHARGE SELECT BANK (S0~)	Precharge command (chip select 0)
PRE - PRECHARGE SELECT BANK (S1~)	Precharge command (chip select 1)
READ - COL ADDR READ (S0~)	Read command – initiates a burst read access to active row (chip select 0)
READ - COL ADDR READ (S1~)	Read command – initiates a burst read access to active row (chip select 1)
READ DATA	Valid Read data on the bus
REF - REFRESH (S0~)	Self Refresh command (chip select 0)
REF - REFRESH (S1~)	Self Refresh command (chip select 1)
WRITE - COL ADDR WRITE (S0~)	Write command – initiates a burst write access to active row (chip select 0)
WRITE - COL ADDR WRITE (S1~)	Write command – initiates a burst write access to active row (chip select 1)
WRITE DATA	Valid Write data on the bus
(UNKNOWN)	Command Cycle on falling edge of clock

Table 4- DDR2M-3A / -2A / -2B Mnemonics Definition

6.4 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: DDR2M-3A (or DDR2M-2A / DDR2M-2B) and DDRM-3A: MagniVu (or DDR2M-2A:MagniVu / DDR2M-2B: MagniVu). The first (DDR2M-3A/DDR2M-2A or DDR2M-2B) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, DDR-MagniVu (or DDR2M-2B-MagniVu), will show all of the channels in 8GHz MagniVu mode, so that edge relationships can be examined around the MagniVu trigger point. MagniVu is very useful and in some cases necessary to see/resolve DDR data. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

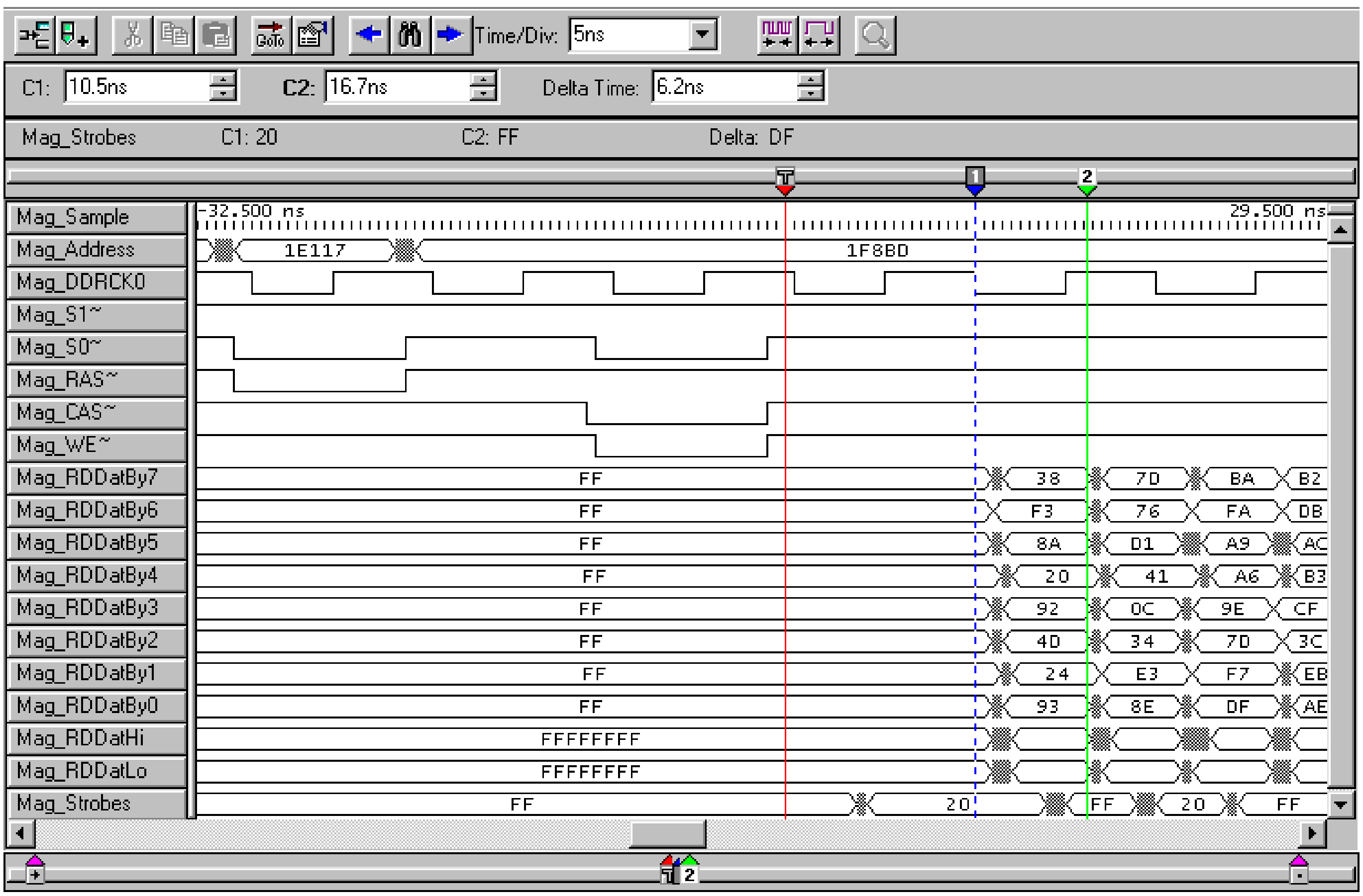


Figure 24- DDR2M-3A / -2A MagniVu Display on TLA

7.0 HINTS & TIPS

7.1 Symbolic Triggering on a Command using the NEX-NEXVuDDR667xU Supports

A Symbol Table has been included in the support packages for the Command data group (see Table 5). The use of Symbol Tables when triggering makes it easier for the user to define a given cycle to be triggered on. Rather than trying to remember what signals make up the Command group, the Symbol Table has the appropriate bits already set for the given cycle.

It is important to note that changing the group, channel, or wiring of the Command group can result in incorrect symbol information being displayed.

Symbol	Definition
DESL--IGNORE_COMMAND--DATA?	11 xxx
NOP--NO_OPERATION_(S0~)	x0 111
NOP--NO_OPERATION_(S1~)	0x 111
BST--BURST_STOP_(S0~)	x0 110
BST--BURST_STOP_(S1~)	0x 110
READ--COL_ADDR_READ_(S0~)	x0 101
READ--COL_ADDR_READ_(S1~)	0x 101
WRITE--COL_ADDR_WRITE_(S0~)	x0 100
WRITE--COL_ADDR_WRITE_(S1~)	0x 100
ACTV--ROW_ADDRESS_STROBE_(S0~)	x0 011
ACTV--ROW_ADDRESS_STROBE_(S1~)	0x 011
PRE--PRECHARGE_SELECT_BANK_(S0~)	x0 010
PRE--PRECHARGE_SELECT_BANK_(S1~)	0x 010
PALL--PRECHARGE_ALL_BANK_(S0~)	x0 010
PALL--PRECHARGE_ALL_BANK_(S1~)	0x 010
REF--REFRESH_(S0~)	x0 001
REF--REFRESH_(S1~)	0x 001
MRS--MODE_REGISTER_SET_(S0~)	x0 000
MRS--MODE_REGISTER_SET_(S1~)	0x 000

Table 5- DDR2M-3A / DDR2M-2A / DDR2M-3B Command Symbol Table

Signals, left-to-right: S1#, S0#, RAS#, CAS#, WE#

7.2 Triggering on a Command using the NEX-NEXVuDDR667xU Supports

The DDR2M-2A support package clocks data into the logic analyzer on both the rising and falling edges of the selected DDR Clock. Command information is only valid on the rising edge of the clock, but it is very possible (even likely) that valid information is also available on the falling edge of the clock preceding the Command's valid rising edge. This can result in a false trigger of the TLA. With the DDR2M-2A post-processing software such a cycle (falling edge of DDR Clock with valid Command data) is labeled as an Unknown cycle. These cycles would be filtered out (suppressed) when changing the Disassembly Properties display mode to something other than Hardware, resulting in a Trigger position that is hidden from the user.

To eliminate this problem it is suggested that a trigger condition be defined that ANDs the desired Command with the DDR Clock channel being used for acquisition in a LOW state (see Figure 25). (Since the data stored by the TLA reflects its state before the acquisition clock occurs the DDR Clock is stored as a LOW for a rising clock edge and as a HIGH for a falling clock edge.) Figure 26 shows the actual Trigger Clause definition used in the trigger program shown in Figure 25.

Note that this situation does not occur with the DDR2M-3A or DDR2M-2B supports since these supports only clock data using the rising edge of the DDR Clock. Thus adding the check for DDRCK0 is redundant.

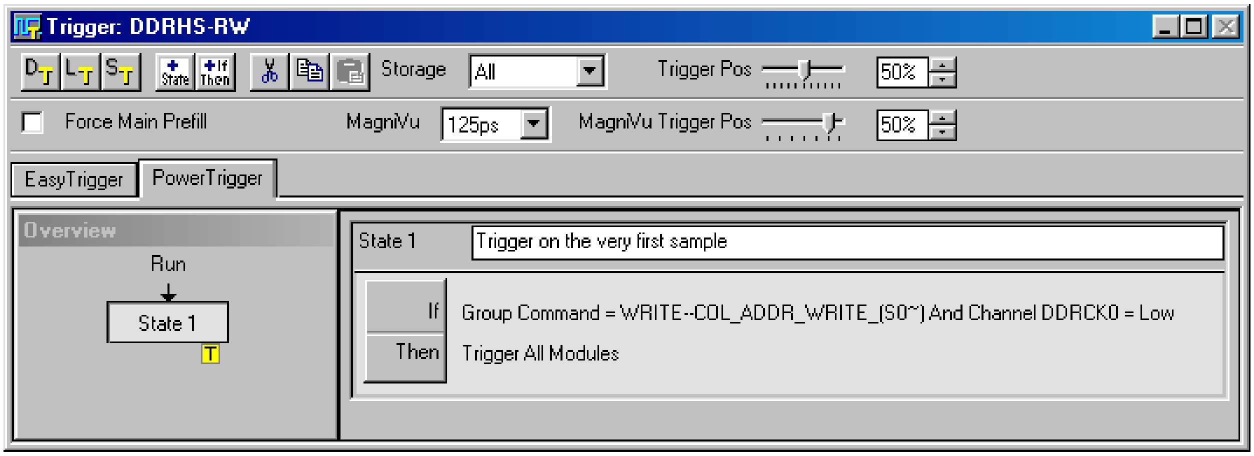


Figure 25- Recommended DDR2M-2A Command Trigger

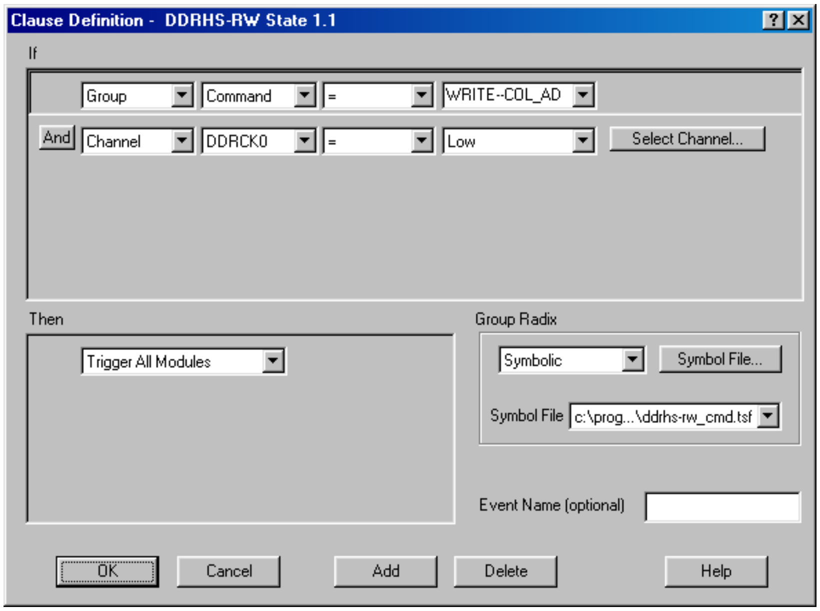


Figure 26- Recommended DDR2M-2A Command Trigger Detail

7.3 Installing Memories in a blank DIMM

If the user purchases a DIMM that will be configurable with alternate memory Vendor parts, or if the user wished to change memories on a purchased DIMM they should consider the flowing:
The memory must be of the same configuration as the DIMM was designed for. Said another way, make sure that the memory that you are going to mount has the same data width configuration as the Module was designed for.
Use BGA rework station that has the ability to see the board and the replacement chip at the same time. This normally includes a prism / light alignment system.
Nexus Technology can recommend a vendor for BGA rework is you do not have the facilities. Please contact us at Nexus Technology.

7.4 Capturing MRS (Mode Register Set) Data

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the NEX-NEXVuDDR667xU supports for the post-processing software to properly decode the acquisitions. The TLA trigger shown in Figure 27 can be used to acquire the MRS cycles when using either of these supports.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

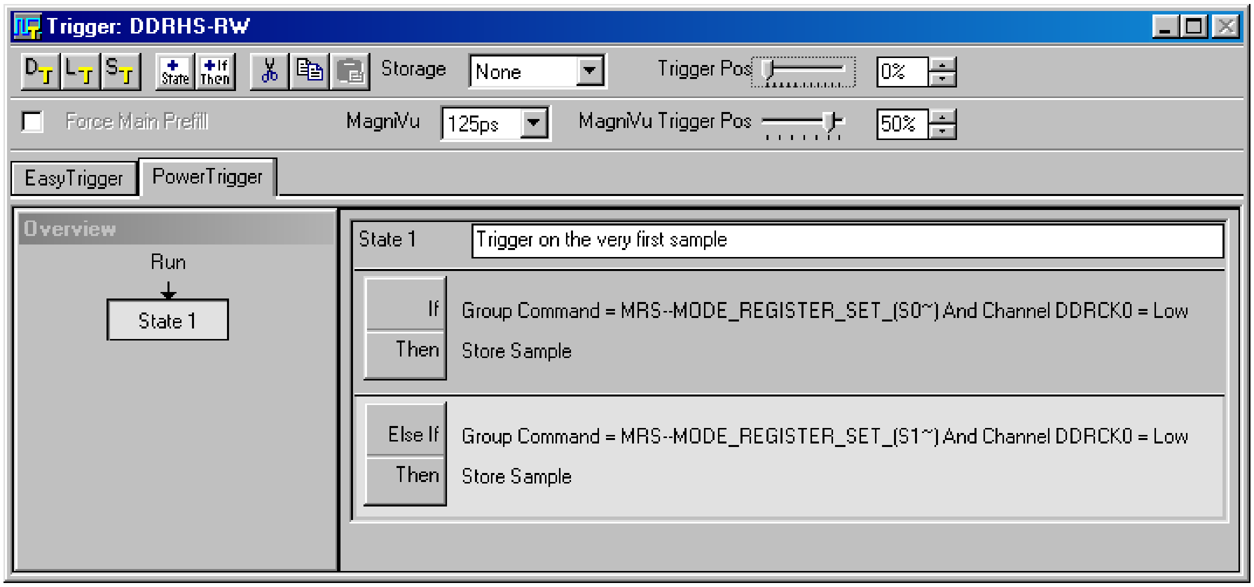


Figure 27- DDR2M-2A MRS Trigger

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in Figure 28. The last acquired MRS cycle will reflect the settings used in the DDR target – in this case, a CAS latency of 2 cycles with a Burst length of 8.

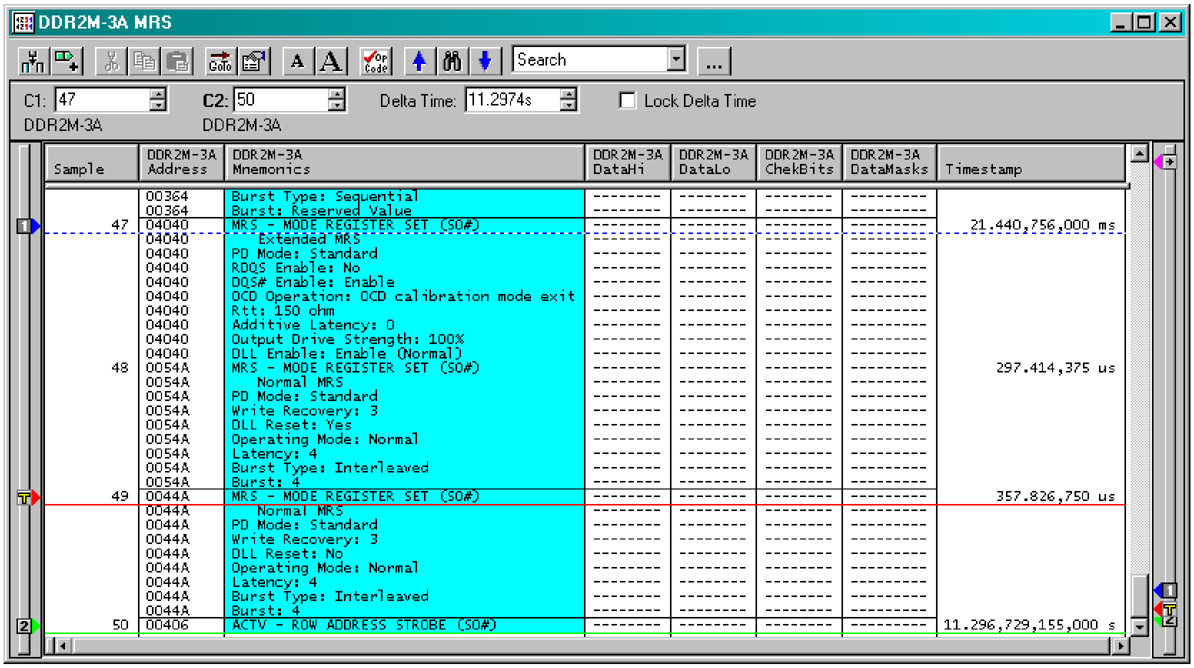


Figure 28- MRS Cycle Acquisition Disassembly

8.0 DEBUGGING HINTS

8.1 Required NEXVu-DIMM that is Unavailable

Nexus Technology is pursuing this new NEXVu-DIMM approach for debug with the belief that old fashioned Interposers and built-in foot prints on motherboards will not reliably capture DDRII signals above 400MT/s. While we have a growing variety of NEXVu-DIMMs available there is the possibility that we do not have the variation of DIMM that may be needed for a specific debug task. To help facilitate our customers we are working hard to increase the variety of NEXVu-DIMMs available. If the NEXVu-DIMM you desire is not available Nexus recommends the debug techniques listed below:

Each major family of NEXVu-DIMMs supported by Nexus Technology will have an NEXVu-DIMM available that has not been populated with memory components. This DIMM can be custom configured by the customer to a desired configuration by the addition of memory chips that may be available to the customer but not to Nexus.

In user testing a customer may have a DIMM that is exhibiting a problem. The equivalent NEXVu-DIMM may not exhibit the problem for a number of reasons. Among these reason are:
Problem DIMM has a different version level of memory chips available

Problem DIMM has an alternate vendor's memory chips.

Facing this situation the customer has the option of:

Implementing the suggestion in bullet #1 above.

Using to signals available in an adjacent NEXVu-DIMM to trigger on a known Address/Data access to the Problem DIMM and then view the timing measurements in the Logic Analyzers MagniVu Timing display – realizing that the timing at the adjacent NEXVu-DIMM is slightly different from that of the problem DIMM.   NOTE: Some signals, like RAS#, may go low in idle cycles making triggering difficult.

Use the Logic Analyzer connection pads on an adjacent NEXVu-DIMM for an easy connection point for a high quality scope to view the DDRII signals and determine the signal quality. This can be easily done by using the Analog Mux feature of the Tektronix Logic Analyzer where selected inputs to the Logic Analyzer module may be passed through to an external oscilloscope for analog analysis.

8.2 Handling the NEXVu-DIMM

The NEXVu-DIMMs have the memory chips under-filled (memory chips held in place with an epoxy-like glue) to protect them from contact fractures caused by torque from the Logic Analyzer probe. However, care must still be taken to avoid excessive torque on the NEXVu-DIMMs by the Logic Analyzer probes to prevent damage to the DIMM.

User Configurable NEXVu-DIMMs will not have under-fill, thus extra care must be taken to avoid torque on the NEXVu-DIMM by the Logic Analyzer probes.

APPENDIX A - How DDR Data is Clocked

A.1 Background

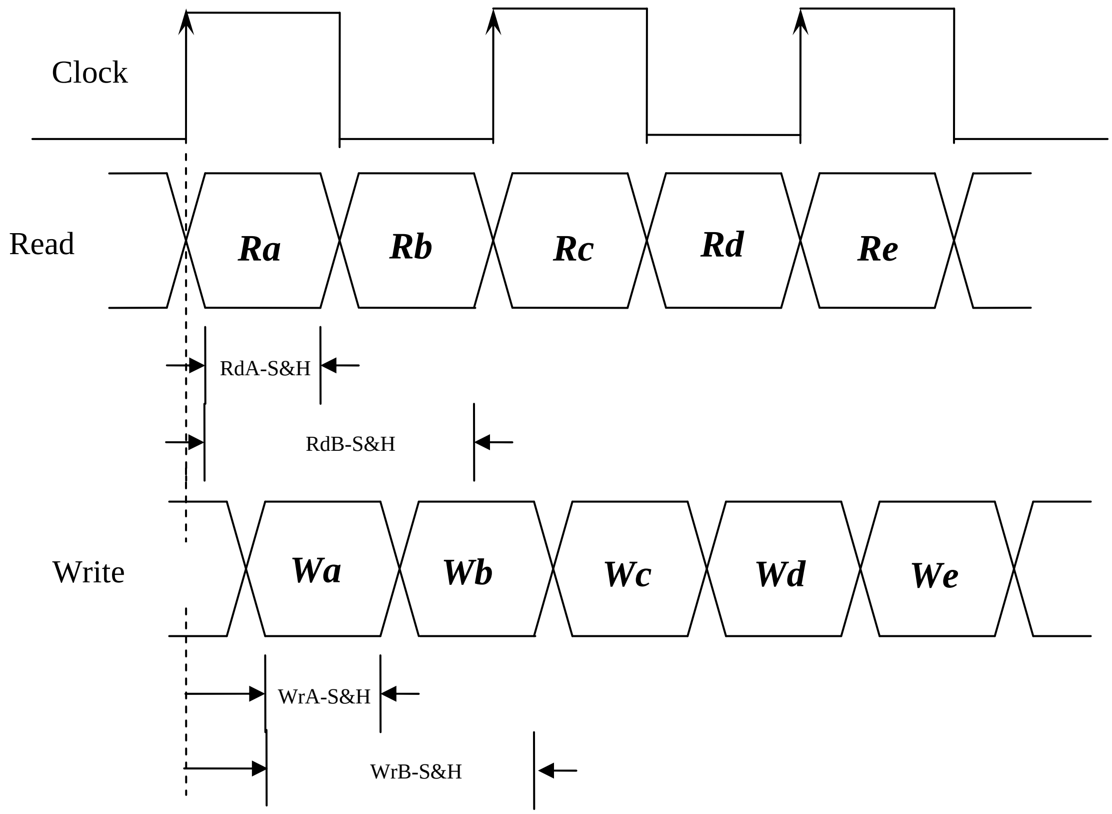
Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two or four separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section ***and*** the D3 section. Using 4X demux, connections made to the A3 channels permit data to be stored in the A3, A2, D3 and D2 sections. A very useful side benefit of using demux is that, since only one set of TLA data channels has to be connected, only one probe load is added to the target, even though data is stored in two or four different locations of the acquisition card.

A.2 DDR Acquisition - General

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. The speeds of DDR (400 and 667MT/s) require different setups to enable proper data acquisition. In addition, instead of trying to use the 8 Data Strobes to acquire data our solution uses one of the DDR SDRAM Clocks (either CK0 or CK1, user selectable) and all data acquisition is adjusted in relation to the clock edges. The 8 Data Strobes cannot be easily used to acquire data as some TLA configurations only support 4 Clock Inputs. Also, the Strobes cannot be used to acquire Address and Command information.

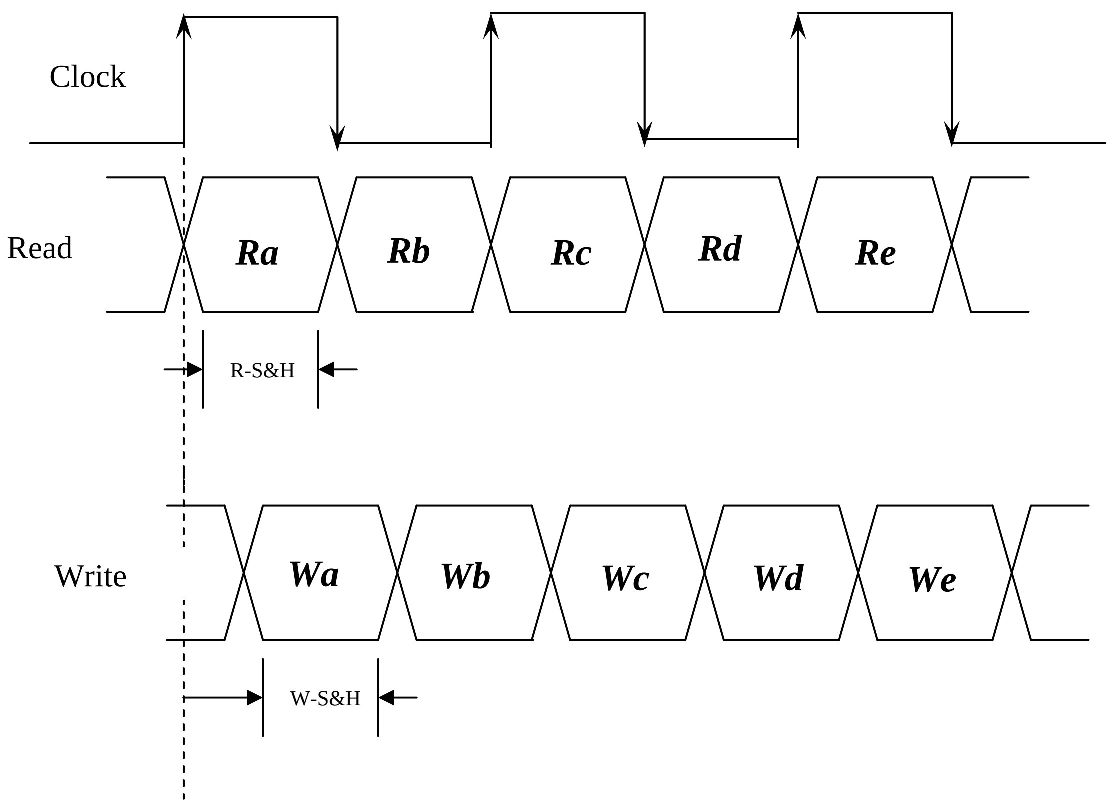
A.3 DDR2M-3A Support

This support requires three (3) merged 136-channel 450MHz acquisition cards used in a TLA7XX logic analyzer. Data is acquired using the rising edge of the 266MHz DDR clock, and 4X demultiplexing is done to permit acquiring two samples each of 64-bit Read and Write data relative to the clock edge (for a total of 4 64-bit data samples for each DDR clock cycle). A_Data information is earlier (older) data than the information stored in B_Data. Again, different Sample Points must be set for each of the four 32-bit Data groups, and again, if necessary, sample points can be set for any of the 8-bit data groups.



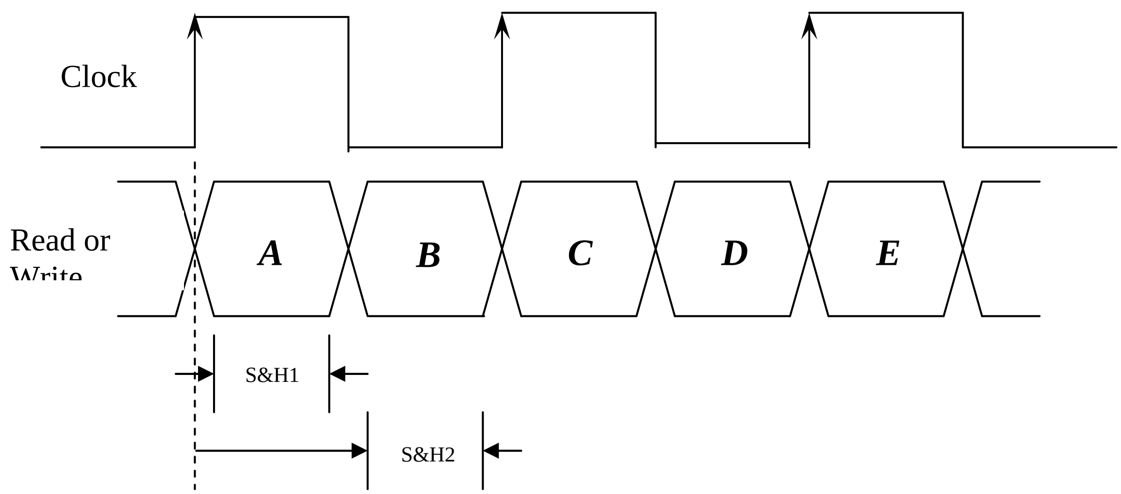
A.4 DDR2M-2A Support

This support requires two (2) merged 136-channel 450MHz TLA7Ax4 acquisition cards used in a TLA7XX. The merged cards enable 400MT/s Read and Write data to be acquired simultaneously from a DDR system. Data is acquired using both edges of the DDR clock, and 2X demultiplexing is done to permit acquiring both Read and Write data on every clock edge. One Sample Point must be set to acquire valid Read data in reference to the clock edge; a second Sample Point must be set to acquire valid Write data in relation to that edge. Again, different Sample Points must be set for each of the Read / Write data groups, and if necessary, sample points can be set for any of the 8-bit data groups.



A.5 DDR2M-2B Support

This support requires two 450MHz 136-channel TLA7AA4 acquisition cards. Because of the speed and channel count requirements only Read or Write data from a 667MT/s DDRII target can be acquired. Data is acquired using the rising edge of the 333MHz DDR clock, and 2X demultiplexing is done to permit acquiring two samples of 64-bit Read or Write data relative to the clock edge. A_Data information is earlier (older) data than the information stored in B_Data. Again, different Sample Points must be set for each of the four 32-bit Data groups, and again, if necessary, sample points can be set for any of the 8-bit data groups.



APPENDIX B - Considerations

B.1 NEX-NEXVUDDR667XU Bus Loading

It must be noted that the NEX-NEXVUDDR667XU NEXVu-DIMMs are designed to meet JEDEC standards. The acquired signals are sampled at the pins of the memory chips, and then passed through stub resistors to reduce capacitive loading. The NEXVu-DIMM has been tested via detailed simulations, and by actual in circuit testing.

Unlike Interposers that were commonly used at slower frequencies, the NEXVu-DIMM does not add to the signal lengths from the memory control to the DIMM, thus ensuring correct system operation.

APPENDIX C - NEX-NEXVUDDR667XU Compression Pinouts

For further information on the P6860 and P6864 Connectorless probe compression footprints please refer to the “P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-03.

Pad #	TLA Channel	DDR Signal
A15	Q3-	Spare3#
A13	Q3+	Spare3
B12	E3:7	DQ0
B10	E3:6	DQ1
A12	E3:5	DQ2
A10	E3:4	DQ3
B9	E3:3	DQ4
B7	E3:2	DQ5
A9	E3:1	DQ8
A7	E3:0	DQ9
B6	E2:7	
B4	E2:6	
A6	E2:5	
A4	E2:4	
B3	E2:3	
B1	E2:2	
A3	E2:1	
A1	E2:0	

Probe Connection
M – E3 / E2

Pad #	TLA Channel	DDR Signal
A15	CK0-	DDRCK2#
A13	CK0+	DDRCK2
B12	A3:7	DM5
B10	A3:6	GND
A12	A3:5	SA2
A10	A3:4	NC_TEST
B9	A3:3	DM6
B7	A3:2	GND
A9	A3:1	DQS6#
A7	A3:0	DQS6
B6	A2:7	DM7
B4	A2:6	GND
A6	A2:5	DQS7#
A4	A2:4	DQS7
B3	A2:3	SA0
B1	A2:2	SA1
A3	A2:1	SDA
A1	A2:0	SCL

Probe Connection
M-A3 /A2

Pad # #	TLA Channel	DDR Signal
A15	CK1-	GND
A13	CK1+	CKE0
B12	A1:7	GND
B10	A1:6	GND
A12	A1:5	GND
A10	A1:4	BA2
B9	A1:3	RC0
B7	A1:2	A11
A9	A1:1	A7
A7	A1:0	GND
B6	A0:7	A8
B4	A0:6	A6
A6	A0:5	A5
A4	A0:4	A4
B3	A0:3	A3
B1	A0:2	A1
A3	A0:1	A2
A1	A0:0	GND

Probe Connection
M – A1 / A0

APPENDIX C - NEX-NEXVUDDR667XU Compression Pinouts (cont'd.)

Pad #	TLA Channel	DDR Signal
A15	Q0-	GND
A13	Q0+	S1#/GND
B12	D3:7	GND
B10	D3:6	A0
A12	D3:5	ODT1/GND
A10	D3:4	GND
B9	D3:3	GND
B7	D3:2	BA1
A9	D3:1	DQS4#
A7	D3:0	DQS4
B6	D2:7	GND
B4	D2:6	GND
A6	D2:5	DQS5#
A4	D2:4	DQS5
B3	D2:3	ODT0
B1	D2:2	A13
A3	D2:1	GND
A1	D2:0	GND

Probe Connection
M – D3 / D2

Pad #	TLA Channel	DDR Signal
A15	CK2-	DDRCK1#
A13	CK2+	DDRCK1
B12	D1:7	NC147
B10	D1:6	DM2
A12	D1:5	DQS2
A10	D1:4	DQS2#
B9	D1:3	GND
B7	D1:2	GND
A9	D1:1	GND
A7	D1:0	DM1
B6	D0:7	DQS1
B4	D0:6	DQS1#
A6	D0:5	Spare2
A4	D0:4	GND
B3	D0:3	DQS0
B1	D0:2	DQS0/
A3	D0:1	NC126
A1	D0:0	DM0

Probe Connection
M – D1 / D0

Pad #	TLA Channel	DDR Signal
A15	CK3-	DDRCK0#
A13	CK3+	DDRCK0
B12	C3:7	GND
B10	C3:6	GND
A12	C3:5	GND
A10	C3:4	GND
B9	C3:3	GND
B7	C3:2	A10/AP
A9	C3:1	BA0
A7	C3:0	GND
B6	C2:7	GND
B4	C2:6	GND
A6	C2:5	DM4
A4	C2:4	GND
B3	C2:3	RAS#
B1	C2:2	S0#
A3	C2:1	WE#
A1	C2:0	CAS#

Probe Connection
M – C3 / C2

Pad #	TLA Channel	DDR Signal
A15	Q1-	GND
A13	Q1+	CKE1/GND
B12	C1:7	A9
B10	C1:6	A12
A12	C1:5	GND
A10	C1:4	DM3
B9	C1:3	A14
B7	C1:2	A15
A9	C1:1	GND
A7	C1:0	DM8
B6	C0:7	DQS8
B4	C0:6	DQS8#
A6	C0:5	GND
A4	C0:4	GND
B3	C0:3	DQS3
B1	C0:2	DQS3#
A3	C0:1	GND
A1	C0:0	Spare1

Probe Connection
M– C1 / C0

Pad #	TLA Channel	DDR Signal
A15	CK3-	GND
A13	CK3+	GND
B12	E3:0	DQ21
B10	E3:1	DQ20
A12	C3:7	DQ10
A10	C3:6	DQ11
B9	E3:2	DQ15
B7	E3:3	DQ14
A9	C3:5	DQ16
A7	C3:4	DQ17
B6	E3:4	DQ13
B4	E3:5	DQ12
A6	C3:3	DQ18
A4	C3:2	DQ19
B3	E3:6	DQ7
B1	E3:7	DQ6
A3	C3:1	DQ22
A1	C3:0	DQ23

Probe Connection
S – C3 / E3

Pad # #	TLA Channel	DDR Signal
A15	CK1-	GND
A13	CK1+	GND
B12	A3:0	DQ49
B10	A3:1	DQ48
A12	A1:7	DQ32
A10	A1:6	DQ33
B9	A3:2	DQ45
B7	A3:3	DQ44
A9	A1:5	DQ34
A7	A1:4	DQ35
B6	A3:4	DQ39
B4	A3:5	DQ38
A6	A1:3	DQ40
A4	A1:2	DQ41
B3	A3:6	DQ37
B1	A3:7	DQ36
A3	A1:1	DQ42
A1	A1:0	DQ43

Probe Connection
S – A1 / A3

Pad #	TLA Channel	DDR Signal
A15	CK3-	GND
A13	CK3+	GND
B12	E3:0	DQ61
B10	E3:1	DQ60
A12	C3:7	DQ52
A10	C3:6	DQ53
B9	E3:2	DQ55
B7	E3:3	DQ54
A9	C3:5	DQ56
A7	C3:4	DQ57
B6	E3:4	DQ51
B4	E3:5	DQ50
A6	C3:3	DQ58
A4	C3:2	DQ59
B3	E3:6	DQ47
B1	E3:7	DQ46
A3	C3:1	DQ62
A1	C3:0	DQ63

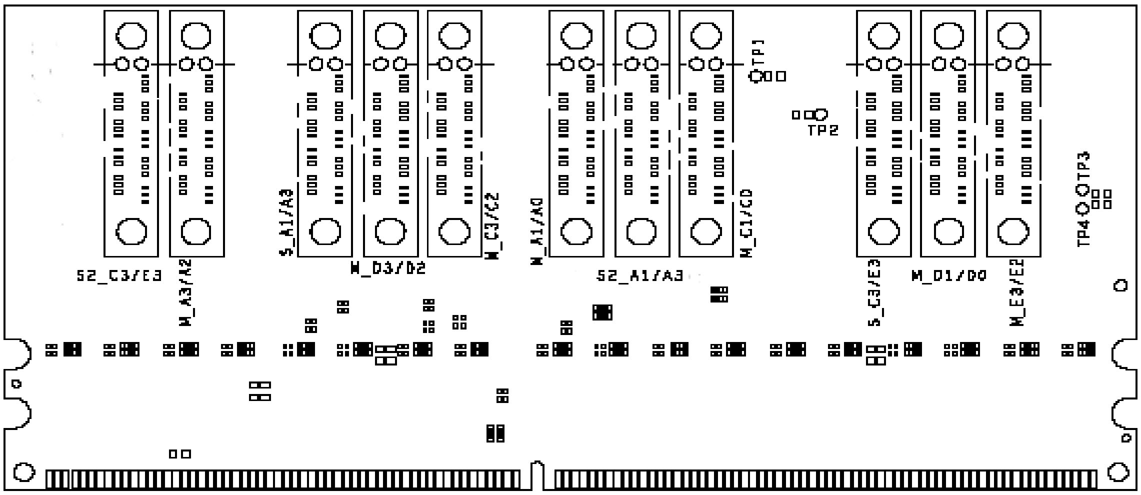
Probe Connection
S2 – C3 / E3

Pad # #	TLA Channel	DDR Signal
A15	CK1-	GND
A13	CK1+	GND
B12	A3:0	DQ28
B10	A3:1	DQ29
A12	A1:7	NC_CB5
A10	A1:6	NC_CB4
B9	A3:2	NC_CB0
B7	A3:3	NC_CB1
A9	A1:5	DQ31
A7	A1:4	DQ30
B6	A3:4	NC_CB2
B4	A3:5	NC_CB3
A6	A1:3	DQ27
A4	A1:2	DQ26
B3	A3:6	NC_CB6
B1	A3:7	NC_CB7
A3	A1:1	DQ25
A1	A1:0	DQ24

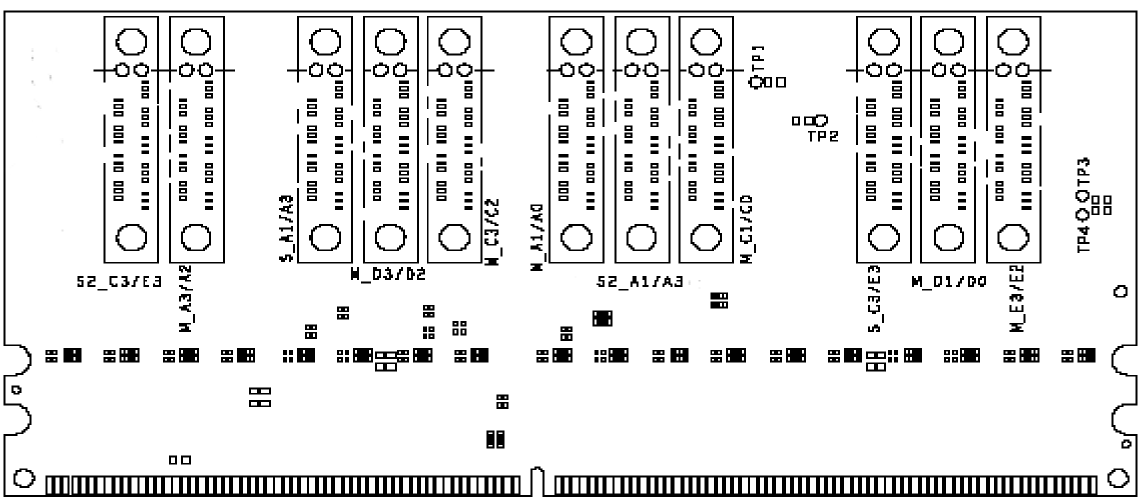
Probe Connection
S2 – A1 / A3

APPENDIX D – NEX-NEXVUDDR667XU-A Silkscreen

Other Family DIMMs may have different silkscreen, or silkscreen on both front and back.



Front Silk Screen



Back Silk Screen

APPENDIX E – Data Group / Data Byte / Strobe Cross-Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
RdADatHi	RdADatB7	DQS7	63,62,61,60,59,58,57,56
	RdADatB6	DQS6	55,54,53,52,51,50,49,48
	RdADatB5	DQS5	47,46,45,44,43,42,41,40
	RdADatB4	DQS4	39,38,37,36,35,34,33,32
RdADatLo	RdADatB3	DQS3	31,30,29,28,27,26,25,24
	RdADatB2	DQS2	23,22,21,20,19,18,17,16
	RdADatB1	DQS1	15,14,13,12,11,10,9,8
	RdADatB0	DQS0	7,6,5,4,3,2,1,0
WrADatHi	WrADatB7	DQS7	63,62,61,60,59,58,57,56
	WrADatB6	DQS6	55,54,53,52,51,50,49,48
	WrADatB5	DQS5	47,46,45,44,43,42,41,40
	WrADatB4	DQS4	39,38,37,36,35,34,33,32
WrADatLo	WrADatB3	DQS3	31,30,29,28,27,26,25,24
	WrADatB2	DQS2	23,22,21,20,19,18,17,16
	WrADatB1	DQS1	15,14,13,12,11,10,9,8
	WrBDatB0	DQS0	7,6,5,4,3,2,1,0
RdBDatHi	RdBDatB7	DQS7	63,62,61,60,59,58,57,56
	RdBDatB6	DQS6	55,54,53,52,51,50,49,48
	RdBDatB5	DQS5	47,46,45,44,43,42,41,40
	RdBDatB4	DQS4	39,38,37,36,35,34,33,32
RdBDatLo	RdBDatB3	DQS3	31,30,29,28,27,26,25,24
	RdBDatB2	DQS2	23,22,21,20,19,18,17,16
	RdBDatB1	DQS1	15,14,13,12,11,10,9,8
	RdBDatB0	DQS0	7,6,5,4,3,2,1,0
WrBDatHi	WrBDatB7	DQS7	63,62,61,60,59,58,57,56
	WrBDatB6	DQS6	55,54,53,52,51,50,49,48
	WrBDatB5	DQS5	47,46,45,44,43,42,41,40
	WrBDatB4	DQS4	39,38,37,36,35,34,33,32
WrBDatLo	WrBDatB3	DQS3	31,30,29,28,27,26,25,24
	WrBDatB2	DQS2	23,22,21,20,19,18,17,16
	WrBDatB1	DQS1	15,14,13,12,11,10,9,8
	WrBDatB0	DQS0	7,6,5,4,3,2,1,0

DDR2M-3A Groups/Bytes/Strobes Cross Reference

APPENDIX E (cont.) – Data Group / Data Byte / Strobe Cross-Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
RDDatHi	RDDatB7	DQS7	63,62,61,60,59,58,57,56
	RDDatB6	DQS6	55,54,53,52,51,50,49,48
	RDDatB5	DQS5	47,46,45,44,43,42,41,40
	RDDatB4	DQS4	39,38,37,36,35,34,33,32
RDDatLo	RDDatB3	DQS3	31,30,29,28,27,26,25,24
	RDDatB2	DQS2	23,22,21,20,19,18,17,16
	RDDatB1	DQS1	15,14,13,12,11,10,9,8
	RDDatB0	DQS0	7,6,5,4,3,2,1,0
WRDatHi	WRDatB7	DQS7	63,62,61,60,59,58,57,56
	WRDatB6	DQS6	55,54,53,52,51,50,49,48
	WRDatB5	DQS5	47,46,45,44,43,42,41,40
	WRDatB4	DQS4	39,38,37,36,35,34,33,32
WRDatLo	WRDatB3	DQS3	31,30,29,28,27,26,25,24
	WRDatB2	DQS2	23,22,21,20,19,18,17,16
	WRDatB1	DQS1	15,14,13,12,11,10,9,8
	WRDatB0	DQS0	7,6,5,4,3,2,1,0

DDR2M-2A Groups/Bytes/Strobes Cross Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
A_DatHi	A_DatB7	DQS7	63,62,61,60,59,58,57,56
	A_DatB6	DQS6	55,54,53,52,51,50,49,48
	A_DatB5	DQS5	47,46,45,44,43,42,41,40
	A_DatB4	DQS4	39,38,37,36,35,34,33,32
A_DatLo	A_DatB3	DQS3	31,30,29,28,27,26,25,24
	A_DatB2	DQS2	23,22,21,20,19,18,17,16
	A_DatB1	DQS1	15,14,13,12,11,10,9,8
	A_DatB0	DQS0	7,6,5,4,3,2,1,0
B_DatHi	B_DatB7	DQS7	63,62,61,60,59,58,57,56
	B_DatB6	DQS6	55,54,53,52,51,50,49,48
	B_DatB5	DQS5	47,46,45,44,43,42,41,40
	B_DatB4	DQS4	39,38,37,36,35,34,33,32
B_DatLo	B_DatB3	DQS3	31,30,29,28,27,26,25,24
	B_DatB2	DQS2	23,22,21,20,19,18,17,16
	B_DatB1	DQS1	15,14,13,12,11,10,9,8
	B_DatB0	DQS0	7,6,5,4,3,2,1,0

DDR2M-2B Groups/Bytes/Strobes Cross Reference

APPENDIX F - References

JEDEC Double Data Rate (DDR) SDRAM Specification
JESD-79-R2 – February 2002

Micron DDR2 SDRAM, SNOOP™-DIMM
October 2003

Tektronix TLA700 System User’s Manual

Tektronix TLA700 Logic Analyzer User’s Manual

P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual
Tektronix part number 071-1059-03

APPENDIX G - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Web site: http://**www.nexustechnology.com**

Support Contact Information

Technical Support	**techsupport@nexustechnology.com**
General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.