NEX-NVD2M667x8SRxR

NEXVu Validation DIMM, MINI DIMM form factor, DDR2 667 max data speed, x8 memory configuration, Registered

Including these Software Support package:
MDDR2-3A

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1.0 OVERVIEW

1.1 General Information

The NEXVu families of Logic Analyzer DIMMs (**NEX-NVD2M667x8SRxR**) have been designed to provide a quick and easy connection to interface a Tektronix TLA700/7000-series Logic Analyzer to a ??-pin DDRII (Double Data Rate II) Synchronous DRAM Mini Dual In-Line Memory Module (SDRAM MiniDIMM). **Contact Nexus Technology for other available DDRII NEXVu-DIMM supports, and current DIMMs and software this manual covers**.

This manual covers all Registered NEXVu DDR MiniDIMM products from NEXUS. While it refers to the latest version, the information is directly applicable to the lower speed 400 and 533 versions.

Note: The NEX-NVD2M667x8SRxR DIMMs will operate at 667MT/s.
At printing this manual covered the following Nexus products: All Registered Mini DIMM NEXVu DDR2 products and options. Call for a full list of available products.

Logic Analyzer connections are made using Nexus Low Profile Family of probes. These probes help minimize the size of the Logic Analyzer DIMM board, thus reducing interference between the system under test and the NEXVu product.

The NEX-NVD2M667x8SRxR support includes one software packages to acquire DDR2 data at up to 667MT/s speeds:

> **MDDR2-3A** - allows the user to acquire DDRII Read **AND** Write data at speeds up to and including 667MT/s from a target. This support requires 4ea. NEX-PRB1X and 2ea. NEX-PRB4X Low Profile probes, and three merged Tektronix TLA7AA4 or TLA7AB4 136-channel 450MHz state speed acquisition cards.

2.0 SOFTWARE INSTALLATION

The **NEX-NVD2M667x8SRxR** software is installed using the same method as other Windows programs. Place the MDDR2-3A Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer module in the Setup window, select Load Support Package from the File pull-down, then choose either MDDR2-3A and click on **Okay**. Note that the selected support may require two or three merged modules and that the TLA acquisition cards must be configured properly for the software to load.

3.0 CONNECTING to the NEX-NVD2M667x8SRxR DIMM

3.1 General

Care should be taken to support the weight of the acquisition probes so that the Logic Analyzer DIMM board and/or target socket are not damaged

To acquire DDRII Read **and** Write data at speeds up to 667MT/s will require three merged TLA7Ax4 136-channel 450MHz state speed acquisition cards and the use of the **MDDR2-3A** support software. The Master card will be in the center of the three cards; Slave card #1 is in the adjacent high-numbered slots and Slave card #2 will be in the adjacent lower-numbered slots. The logic analyzer modules should be connected to the **NEX-NVD2M667X8SRxR** DIMM as follows using four (4) NEX-PRB1X probes and four (2) NEX-PRB4X probes:

TLA Master NEX-PRB1X **A3/2/D3/2** probe head to DDRII DIMM **M_ A3/2 D3/2** position
TLA Master NEX-PRB1X **A1/0/D1/0** probe head to DDRII DIMM **M_ A1/0 D1/0** position
TLA Master NEX-PRB1X **C3/2/1/0** probe head to DDRII DIMM **M_C3/2/1/0** position
TLA Master NEX-PRB1X **E3/2/1/0** probe head to DDRII DIMM **M_E3/2/1/0** position
TLA Slave #1 NEX-PRB4X **C3/E3/A1/A3** probe head to DDRII DIMM **S_C3/E3/A3/A1** position
TLA Slave #2 NEX-PRB4X **C3/E3/A1/A3** probe head to DDRII DIMM **S2_C3/E3/A3/A1** position

Table 1 shows the Channel Grouping / Wiring for use with the **MDDR2-3A** support.
Note that Logic Analyzer connections are made on both the front and back of the NEXVu MiniDIMM.

Group Name	Signal Name	DDRII Pin #	TLA Input	Group Name	Signal Name	DDRII Pin #	TLA Input
RdA_DatHi (Hex)	RD_A_DQ63	240	S2_A1:6	RdA_DatLo (Hex)	RD_A_DQ31	161	S_ A1:7
	RD_A_DQ62	239	S2_A1:7		RD_A_DQ30	160	S_ A1:6
	RD_A_DQ61	234	S2_A1:5		RD_A_DQ29	155	S_ A1:5
	RD_A_DQ60	233	S2_A1:4		RD_A_DQ28	154	S_ A1:4
	RD_A_DQ59	119	S2_A3:0		RD_A_DQ27	40	S_ A3:0
	RD_A_DQ58	118	S2_A3:1		RD_A_DQ26	39	S_ A3:1
	RD_A_DQ57	113	S2_A3:2		RD_A_DQ25	34	S_ A3:2
	RD_A_DQ56	112	S2_A3:3		RD_A_DQ24	33	S_ A3:3
	RD_A_DQ55	231	S2_A3:4		RD_A_DQ23	152	S_A3:4
	RD_A_DQ54	230	S2_A3:5		RD_A_DQ22	151	S_A3:5
	RD_A_DQ53	222	S2_A3:6		RD_A_DQ21	146	S_A3:6
	RD_A_DQ52	221	S2_A3:7		RD_A_DQ20	145	S_A3:7
	RD_A_DQ51	110	S2_A1:3		RD_A_DQ19	31	S_ A1:3
	RD_A_DQ50	109	S2_A1:2		RD_A_DQ18	30	S_ A1:2
	RD_A_DQ49	101	S2_A1:1		RD_A_DQ17	25	S_A1:1
	RD_A_DQ48	100	S2_A1:0		RD_A_DQ16	24	S_A1:0
	RD_A_DQ47	219	S2_C3:0		RD_A_DQ15	143	S_E3:7
	RD_A_DQ46	218	S2_C3:1		RD_A_DQ14	142	S_E3:6
	RD_A_DQ45	213	S2_E3:4		RD_A_DQ13	134	S_E3:5
	RD_A_DQ44	212	S2_E3:5		RD_A_DQ12	133	S_E3:4
	RD_A_DQ43	98	S2_E3:7		RD_A_DQ11	22	S_C3:0
	RD_A_DQ42	97	S2_E3:6		RD_A_DQ10	21	S_C3:1
	RD_A_DQ41	92	S2_C3:2		RD_A_DQ9	13	S_C3:2
	RD_A_DQ40	91	S2_C3:3		RD_A_DQ8	12	S_C3:3
	RD_A_DQ39	210	S2_C3:4		RD_A_DQ7	131	S_C3:4
	RD_A_DQ38	209	S2_C3:5		RD_A_DQ6	130	S_C3:5
	RD_A_DQ37	204	S2_C3:6		RD_A_DQ5	125	S_C3:6
	RD_A_DQ36	203	S2_C3:7		RD_A_DQ4	124	S_C3:7
	RD_A_DQ35	89	S2_E3:3		RD_A_DQ3	10	S_E3:3
	RD_A_DQ34	88	S2_E3:2		RD_A_DQ2	9	S_E3:2
	RD_A_DQ33	83	S2_E3:1		RD_A_DQ1	4	S_E3:1
	RD_A_DQ32	82	S2_E3:0		RD_A_DQ0	3	S_E3:0

Table 1- MDDR2-3A (667 Read & Write) TLA Channel Grouping

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The ‘S’ in front of a TLA channel denotes Slave card #1 of the merged set
3. The ‘S2’ in front of a TLA channel denotes Slave card #2 of the merged set
4. The ‘M’ in front of a TLA channel denotes the Master card of the merged set

Group Name	Signal Name	DDRII Pin #	TLA Input	Group Name	Signal Name	DDRII Pin #	TLA Input
RdB_DatHi (Hex)	RD_B_DQ63	240	S2_A0:6	RdB_DatLo (Hex)	RD_B_DQ31	161	S_A0:7
	RD_B_DQ62	239	S2_A0:7		RD_B_DQ30	160	S_A0:6
	RD_B_DQ61	234	S2_A0:5		RD_B_DQ29	155	S_A0:5
	RD_B_DQ60	233	S2_A0:4		RD_B_DQ28	154	S_A0:4
	RD_B_DQ59	119	S2_A2:0		RD_B_DQ27	40	S_ A2:0
	RD_B_DQ58	118	S2_A2:1		RD_B_DQ26	39	S_ A2:1
	RD_B_DQ57	113	S2_A2:2		RD_B_DQ25	34	S_ A2:2
	RD_B_DQ56	112	S2_A2:3		RD_B_DQ24	33	S_ A2:3
	RD_B_DQ55	231	S2_A2:4		RD_B_DQ23	152	S_A2:4
	RD_B_DQ54	230	S2_A2:5		RD_B_DQ22	151	S_A2:5
	RD_B_DQ53	222	S2_A2:6		RD_B_DQ21	146	S_A2:6
	RD_B_DQ52	221	S2_A2:7		RD_B_DQ20	145	S_A2:7
	RD_B_DQ51	110	S2_A0:3		RD_B_DQ19	31	S_A0:3
	RD_B_DQ50	109	S2_A0:2		RD_B_DQ18	30	S_A0:2
	RD_B_DQ49	101	S2_A0:1		RD_B_DQ17	25	S_A0:1
	RD_B_DQ48	100	S2_A0:0		RD_B_DQ16	24	S_A0:0
	RD_B_DQ47	219	S2_C2:0		RD_B_DQ15	143	S_E2:7
	RD_B_DQ46	218	S2_C2:1		RD_B_DQ14	142	S_E2:6
	RD_B_DQ45	213	S2_E2:4		RD_B_DQ13	134	S_E2:5
	RD_B_DQ44	212	S2_E2:5		RD_B_DQ12	133	S_E2:4
	RD_B_DQ43	98	S2_E2:7		RD_B_DQ11	22	S_C2:0
	RD_B_DQ42	97	S2_E2:6		RD_B_DQ10	21	S_C2:1
	RD_B_DQ41	92	S2_C2:2		RD_B_DQ9	13	S_C2:2
	RD_B_DQ40	91	S2_C2:3		RD_B_DQ8	12	S_C2:3
	RD_B_DQ39	210	S2_C2:4		RD_B_DQ7	131	S_C2:4
	RD_B_DQ38	209	S2_C2:5		RD_B_DQ6	130	S_C2:5
	RD_B_DQ37	204	S2_C2:6		RD_B_DQ5	125	S_C2:6
	RD_B_DQ36	203	S2_C2:7		RD_B_DQ4	124	S_C2:7
	RD_B_DQ35	89	S2_E2:3		RD_B_DQ3	10	S_E2:3
	RD_B_DQ34	88	S2_E2:2		RD_B_DQ2	9	S_E2:2
	RD_B_DQ33	83	S2_E2:1		RD_B_DQ1	4	S_E2:1
	RD_B_DQ32	82	S2_E2:0		RD_B_DQ0	3	S_E2:0

Table 2- MDDR2-3A (667 Read & Write) TLA Channel Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'S' in front of a TLA channel denotes the Slave card of the merged set
3. The 'S2' in front of a TLA channel denotes the Slave 2 card of the merged set
4. The 'M' in front of a TLA channel denotes the Master card of the merged set
5. All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA Input	Group Name	Signal Name	DDRII Pin #	TLA Input
WrA_DatHi	WR_A_DQ63	240	S2_D1:6	WrA_DatLo	WR_A_DQ31	161	S_D1:7
(Hex)	WR_A_DQ62	239	S2_D1:7	(Hex)	WR_A_DQ30	160	S_D1:6
	WR_A_DQ61	234	S2_D1:5		WR_A_DQ29	155	S_D1:5
	WR_A_DQ60	233	S2_D1:4		WR_A_DQ28	154	S_D1:4
	WR_A_DQ59	119	S2_D3:0		WR_A_DQ27	40	S_ D3:0
	WR_A_DQ58	118	S2_D3:1		WR_A_DQ26	39	S_ D3:1
	WR_A_DQ57	113	S2_D3:2		WR_A_DQ25	34	S_ D3:2
	WR_A_DQ56	112	S2_D3:3		WR_A_DQ24	33	S_ D3:3
	WR_A_DQ55	231	S2_D3:4		WR_A_DQ23	152	S_D3:4
	WR_A_DQ54	230	S2_D3:5		WR_A_DQ22	151	S_D3:5
	WR_A_DQ53	222	S2_D3:6		WR_A_DQ21	146	S_D3:6
	WR_A_DQ52	221	S2_D3:7		WR_A_DQ20	145	S_D3:7
	WR_A_DQ51	110	S2_D1:3		WR_A_DQ19	31	S_D1:3
	WR_A_DQ50	109	S2_D1:2		WR_A_DQ18	30	S_D1:2
	WR_A_DQ49	101	S2_D1:1		WR_A_DQ17	25	S_D1:1
	WR_A_DQ48	100	S2_D1:0		WR_A_DQ16	24	S_D1:0
	WR_A_DQ47	219	S2_C1:0		WR_A_DQ15	143	S_E1:7
	WR_A_DQ46	218	S2_C1:1		WR_A_DQ14	142	S_E1:6
	WR_A_DQ45	213	S2_E1:4		WR_A_DQ13	134	S_E1:5
	WR_A_DQ44	212	S2_E1:5		WR_A_DQ12	133	S_E1:4
	WR_A_DQ43	98	S2_E1:7		WR_A_DQ11	22	S_C1:0
	WR_A_DQ42	97	S2_E1:6		WR_A_DQ10	21	S_C1:1
	WR_A_DQ41	92	S2_C1:2		WR_A_DQ9	13	S_C1:2
	WR_A_DQ40	91	S2_C1:3		WR_A_DQ8	12	S_C1:3
	WR_A_DQ39	210	S2_C1:4		WR_A_DQ7	131	S_C1:4
	WR_A_DQ38	209	S2_C1:5		WR_A_DQ6	130	S_C1:5
	WR_A_DQ37	204	S2_C1:6		WR_A_DQ5	125	S_C1:6
	WR_A_DQ36	203	S2_C1:7		WR_A_DQ4	124	S_C1:7
	WR_A_DQ35	89	S2_E1:3		WR_A_DQ3	10	S_E1:3
	WR_A_DQ34	88	S2_E1:2		WR_A_DQ2	9	S_E1:2
	WR_A_DQ33	83	S2_E1:1		WR_A_DQ1	4	S_E1:1
	WR_A_DQ32	82	S2_E1:0		WR_A_DQ0	3	S_E1:0

Table 3- MDDR2-3A (667 Read & Write) TLA Channel Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
3. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
4. The 'M' in front of a TLA channel denotes the Master card of the merged set
5. All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group	Signal	DDRII	TLA	Group	Signal	DDRII	TLA

Name	Name	Pin #	Input	Name	Name	Pin #	Input
WrB_DatHi	WR_B_DQ63	240	S2_D0:6	WrB_DatLo	WR_B_DQ31	161	S_D0:7
(Hex)	WR_B_DQ62	239	S2_D0:7	(Hex)	WR_B_DQ30	160	S_D0:6
	WR_B_DQ61	234	S2_D0:5		WR_B_DQ29	155	S_D0:5
	WR_B_DQ60	233	S2_D0:4		WR_B_DQ28	154	S_D0:4
	WR_B_DQ59	119	S2_D2:0		WR_B_DQ27	40	S_ D2:0
	WR_B_DQ58	118	S2_D2:1		WR_B_DQ26	39	S_ D2:1
	WR_B_DQ57	113	S2_D2:2		WR_B_DQ25	34	S_ D2:2
	WR_B_DQ56	112	S2_D2:3		WR_B_DQ24	33	S_ D2:3
	WR_B_DQ55	231	S2_D2:4		WR_B_DQ23	152	S_D2:4
	WR_B_DQ54	230	S2_D2:5		WR_B_DQ22	151	S_D2:5
	WR_B_DQ53	222	S2_D2:6		WR_B_DQ21	146	S_D2:6
	WR_B_DQ52	221	S2_D2:7		WR_B_DQ20	145	S_D2:7
	WR_B_DQ51	110	S2_D0:3		WR_B_DQ19	31	S_D0:3
	WR_B_DQ50	109	S2_D0:2		WR_B_DQ18	30	S_D0:2
	WR_B_DQ49	101	S2_D0:1		WR_B_DQ17	25	S_D0:1
	WR_B_DQ48	100	S2_D0:0		WR_B_DQ16	24	S_D0:0
	WR_B_DQ47	219	S2_C0:0		WR_B_DQ15	143	S_E0:7
	WR_B_DQ46	218	S2_C0:1		WR_B_DQ14	142	S_E0:6
	WR_B_DQ45	213	S2_E0:4		WR_B_DQ13	134	S_E0:5
	WR_B_DQ44	212	S2_E0:5		WR_B_DQ12	133	S_E0:4
	WR_B_DQ43	98	S2_E0:7		WR_B_DQ11	22	S_C0:0
	WR_B_DQ42	97	S2_E0:6		WR_B_DQ10	21	S_C0:1
	WR_B_DQ41	92	S2_C0:2		WR_B_DQ9	13	S_C0:2
	WR_B_DQ40	91	S2_C0:3		WR_B_DQ8	12	S_C0:3
	WR_B_DQ39	210	S2_C0:4		WR_B_DQ7	131	S_C0:4
	WR_B_DQ38	209	S2_C0:5		WR_B_DQ6	130	S_C0:5
	WR_B_DQ37	204	S2_C0:6		WR_B_DQ5	125	S_C0:6
	WR_B_DQ36	203	S2_C0:7		WR_B_DQ4	124	S_C0:7
	WR_B_DQ35	89	S2_E0:3		WR_B_DQ3	10	S_E0:3
	WR_B_DQ34	88	S2_E0:2		WR_B_DQ2	9	S_E0:2
	WR_B_DQ33	83	S2_E0:1		WR_B_DQ1	4	S_E0:1
	WR_B_DQ32	82	S2_E0:0		WR_B_DQ0	3	S_E0:0

Table 1 – MDDR2-3A (667 Read and Write) TLA Channel Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
3. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
4. The 'M' in front of a TLA channel denotes the Master card of the merged set
5. All signals on this page are acquired using the TLA's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDRII Pin #	TLA700 Input	Group Name	Signal Name	DDRII Pin #	TLA700 Input
RdAChkBits	RD_A_CB7	168	M_E3:7	WrAChkBits[5]	WR_A_CB7	168	M_E1:7
(OFF)	RD_A_CB6	167	M_E3:6	(OFF)	WR_A_CB6	167	M_E1:6
	RD_A_CB5	162	M_E3:3		WR_A_CB5	162	M_E1:3
	RD_A_CB4	161	M_E3:2		WR_A_CB4	161	M_E1:2
	RD_A_CB3	49	M_E3:5		WR_A_CB3	49	M_E1:5
	RD_A_CB2	48	M_E3:4		WR_A_CB2	48	M_E1:4
	RD_A_CB1	43	M_E3:1		WR_A_CB1	43	M_E1:1
	RD_A_CB0	42	M_E3:0		WR_A_CB0	42	M_E1:0
RdBChkBits[5]	RD_B_CB7	170	M_E2:7	WrBChkBits[5]	WR_B_CB7	168	M_E0:7
(OFF)	RD_B_CB6	169	M_E2:6	(OFF)	WR_B_CB6	167	M_E0:6
	RD_B_CB5	164	M_E2:3		WR_B_CB5	162	M_E0:3
	RD_B_CB4	163	M_E2:2		WR_B_CB4	161	M_E0:2
	RD_B_CB3	49	M_E2:5		WR_B_CB3	49	M_E0:5
	RD_B_CB2	48	M_E2:4		WR_B_CB2	48	M_E0:4
	RD_B_CB1	43	M_E2:1		WR_B_CB1	43	M_E0:1
	RD_B_CB0	42	M_E2:0		WR_B_CB0	42	M_E0:0
ADatMsks	A_DM7	236	M_ A0:0	BDatMsks[5]	B_DM7	232	M_ D0:0
(BIN)	A_DM6	227	M_A1:2	(BIN)	B_DM6	223	M_D1:2
	A_DM5	215	M_D1:3		B_DM5	211	M_A1:3
	A_DM4	206	M_D0:1		B_DM4	202	M_A0:1
	A_DM3	157	M_A3:2		B_DM3	155	M_D3:2
	A_DM2	148	M_A3:6		B_DM2	146	M_D3:6
	A_DM1	136	M_D3:3		B_DM1	134	M_A3:3
	A_DM0	127	M_ D2:0		B_DM0	125	M_ A2:0
Strobes[6]	DQS7	115	M_ A0:2	Address	BA2	55	M_C1:0
(HEX)	DQS6	107	M_A1:0	(Hex)	BA1	192	M_C2:5
	DQS5	95	M_D1:5		BA0	71	M_C2:7
	DQS4	86	M_D0:7		A13	199	M_C2:4
	DQS3	37	M_A3:4		A12	179	M_C1:3
	DQS2	28	M_D3:1		A11	58	M_C1:1
	DQS1	16	M_ D2:5		A10/AP	70	M_C3:0
	DQS0	7	M_ D2:3		A9	180	M_C1:6
Control	CKE0	53	M_Q1		A8	182	M_C1:7
(Sym)	S0#	196	M_C2:0		A7	59	M_C1:4
	RAS#	194	M_C2:1		A6	183	M_C3:7
	CAS#	75	M_C2:2		A5	61	M_C1:5
	WE#	73	M_C2:3		A4	62	M_C3:5
Misc	DDRCK2+/-	220/221	None		A3	185	M_C3:6
(OFF)	DDRCK1+/-	137/138	None		A2	64	M_C3:4
	DDRCK0+/-	188/189	M_CK3		A1	186	M_C3:3
					A0	191	M_C3:2

Table 1 – MDDR2-3A (667 Read and Write) TLA Channel Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. All signals on this page are required for accurate post-processing of acquired data
3. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
4. The 'M' in front of a TLA channel denotes the Master card of the merged set
5. Signals in these groups are acquired using the TLA's demux capability and will not have a MagniVu display value
6. DQS0 in this group will only have valid MagniVu data

Group Name	Signal Name	DDRII Pin #	TLA Input	Group Name	Signal Name	DDRII Pin #	TLA Input
Ungrouped				Ungrouped			
	ODT0	198	M_C2:6		CKE0	52	M_Q1
	DQS8#		M_A2:7		A15	176	M_C0:4
	DQS7#		M_A0:3		A14	177	M_C1:2
	DQS6#		M_A1:1				
	DQS5#		M_D1:4				
	DQS4#		M_D0:6		A_DM8	166	M_A2:1
	DQS3#		M_A3:5		B_DM8	164	M_D2:1
	DQS2#		M_D3:0		DQS8	45	M_A2:6
	DQS1#		M_D2:4				
	DQS0#		M_D2:2				

Table 1 – MDDR2-3A (667 Read and Write) TLA Channel Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. The 'M' in front of a TLA channel denotes the Master card of the merged set

3.2 Display Groups not in Tables 1, 2 or 3

There are several groups in the List window that are not documented in the tables as these groups are used only by the post-processing display software. To ensure correct data display these groups must not be modified. These groups are:

- DataHi
- DataLo
- ChekBits
- Command
- DataMasks
- MRSAddr

4.0 CLOCK SELECTION

There are three clocking option fields available when using the support packages. These select fields permit the user to setup the TLA acquisition as follows:

SDRAM Clocking: – Permits selecting the DDR Clock to be used to acquire data. Only one choice is available:

DDR CK0; S0~ only active (default)

Clock Mode – Allows the user to choose the kind of data acquisition that will be made:

Selective Clocking (default) **-** This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS# or CAS# is asserted low along with S0# or S1#. After every assertion of CAS# (with either S0# or S1#) a samples are taken during the next 17 DDR Clock cycles to ensure that all valid memory cycles have been acquired, then acquisition pauses and waits for the next Command. If CAS# and a Chip Select are asserted during these 17 clock cycles the count is reset. The 17-clock cycle value was determined by adding the maximum Burst Length, CAS Latency, Additive Latency and Registered Delay values together to determine worst case delay from Command to the last cycle containing valid data.

Every SDRAM CK Rising Edge – As the name implies this will cause the acquisition card to store data on every Rising edge of the selected SDRAM clock.

Refresh Cycles: – Permits choosing whether Refresh Cycles will be stored or not. The field choices are:

Do Not Acquire (default) **–** This mode will reduce the number of Refresh cycles stored by the acquisition card to provide optimum use of the acquisition memory.

Acquire – Refresh Cycles will be stored.

5.0 CONFIGURING FOR READ / WRITE DATA ACQUISITION

IMPORTANT !

Prior to configuring your **NEX-NVD2M667X8SRxR** support package it is ***strongly*** recommended that Appendix A ("How DDR Data is Clocked"), section 5.2 ("Selecting DDR Read Sample Points") and section 5.3 ("Selecting DDR Write Sample Points") be read. This background information is very helpful in properly configuring the support.

5.1 Adjusting Input Thresholds for Proper Data Acquisition

The voltage threshold must be properly set on the TLA for proper acquisition of the DDR bus. We recommend that you verify the center point of the SDRAM Clock, any DDR strobe, and any DDR data bit. The CLK threshold should be set close to 0v because the clock is a differential signal. The threshold setting can be verified as correct by taking a TLA acquisition and verifying a 50% duty cycle on the clock by looking at DDRCK0 MagniVu trace. All other signals should be set close to the center of the voltage swing. Please note that synchronous acquisition using a TLA7AAx or TLA7ABx card requires a valid data window of 750ps.

Although you should measure and set the thresholds as described, you can start with a 0.9V threshold value for all signals except for TLA CLK0 which should be set to 0.07V because they are differential signals. These values can be used as a starting point.

5.2 Selecting DDRII Read Sample Points

For the **NEX-NVD2M667X8SRXR** post-processing software packages to accurately show valid data it is necessary to choose the proper sample point to ensure that valid data is acquired when the software expects it. Since valid DDR2 Read data is straddled by the Strobes (see Figure 1) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Reads is determined by adding the Additive Latency value to the CAS Latency value, resulting in the total number of clock cycles from the Read Command to the first valid Read Data. (If these values are not known the technique described in Section 7.3 can be used to determine them.) In Figure 1 the total Read latency is 5 cycles.

The **MDDR2-3A** support acquires four samples of Read/Write data on each rising edge of the DDR2 clock. So to acquire all potential read and write activity sample points must be set up for all four of these possible data (DQ) locations. The figure below is showing the two sample points that must be set for a read. The other two sample points that must be set are for write.
I the figure below to acquire both pieces of Read data the RdA_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #1 in the Figure, and the RdB_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #2.

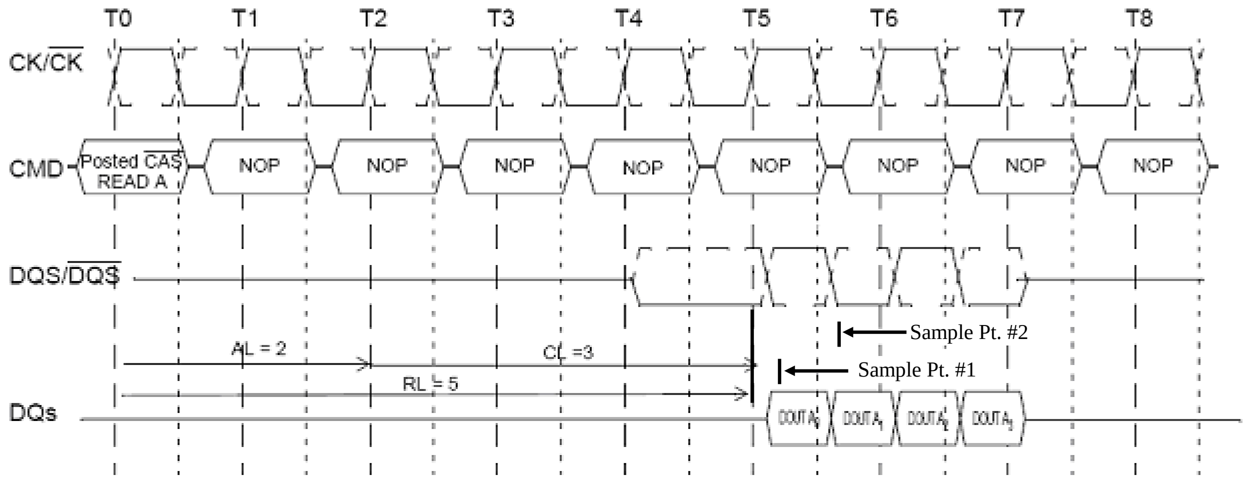


Figure 1- Read Cycle Latency = CAS Latency + Additive Latency (3+2=5 cycles)

5.3 Selecting DDRII Write Sample Points

Unlike valid DDR Read data, valid Write data is bisected by the Strobes. Since valid DDR2 Write data is bisected by the Strobes (see Figure 2) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Writes is determined by adding the Additive Latency value to the CAS Latency value and then subtracting one, resulting in the total number of clock cycles from the Write Command to the first valid Write Data. (If these values are not known the technique described in Section 7.3 can be used to determine them.) In Figure 2 the total Write latency is 4 cycles.

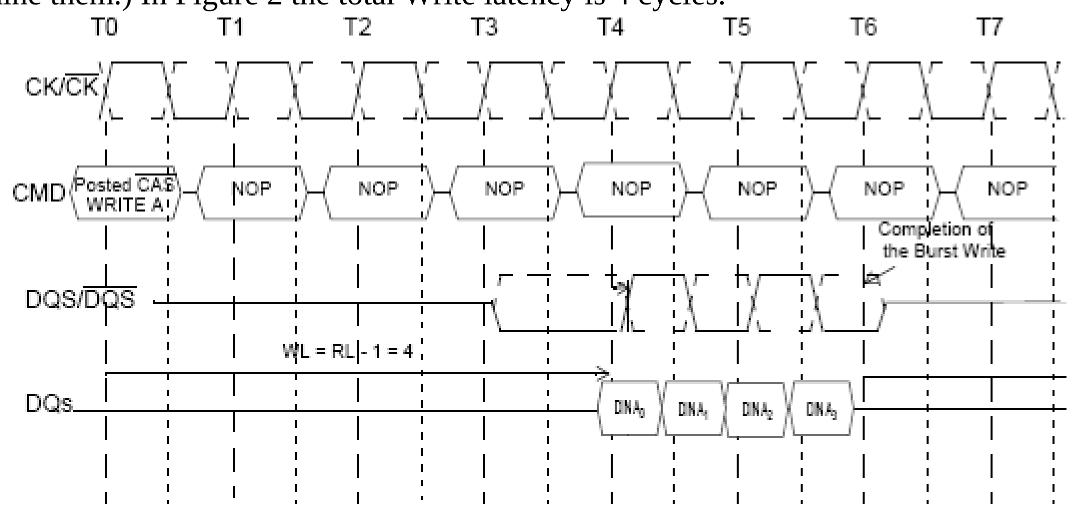


Figure 2- Write Cycle Latency = CAS Latency + Additive Latency -1 (3+2-1=4 cycles)

The **MDDR2-3A** support acquires two samples of valid Write data on each rising edge of the DDR2 clock. So to acquire both pieces of data the WrA_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #1 in the Figure, and the WrB_DatHi/Lo data groups must have their sample point set to that shown by Sample Pt. #2.

5.4 MDDR2-3A Support Setup

Using the **MDDR2-3A** support it is possible to acquire both Read and Write data by setting the sample point of the data groups appropriately. To adjust the Read Data group sample points first make an appropriate acquisition of either Read data by triggering on the cycle of interest. Then create a timing window display of MagniVu data and display the RdA_DatHi and RdA_DatLo 32-bit data groups, the individual Command group signals and the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2). A sample waveform display of MagniVu Read data is shown in Figure 3. To determine the sample point, locate the worst-case Setup & Hold timing of valid Read data during the acquired burst (see Figure 3).

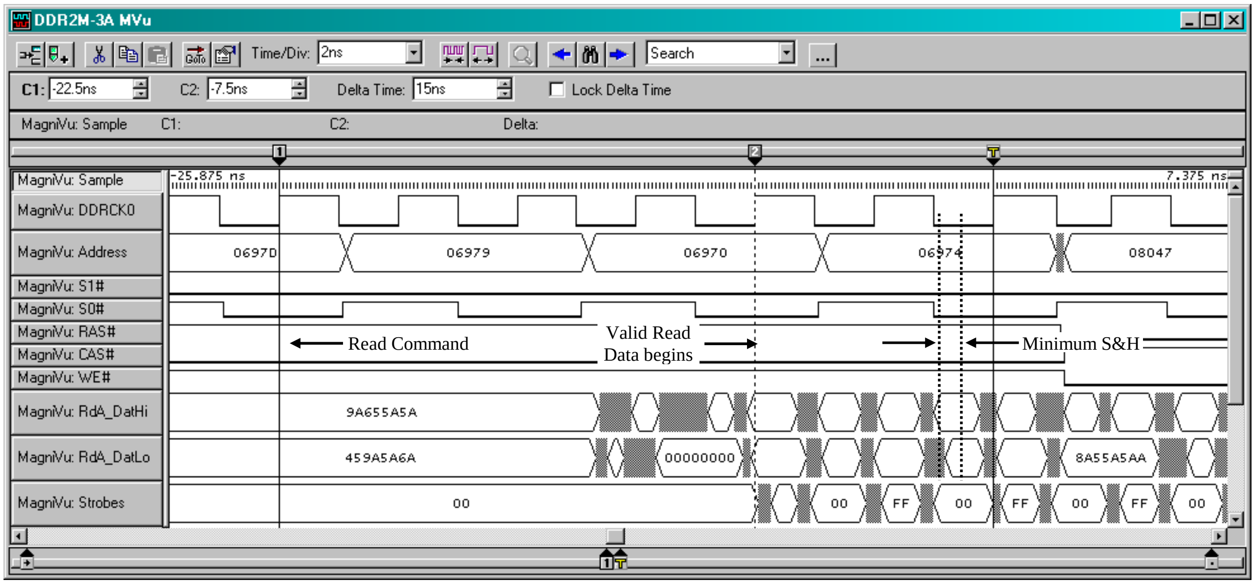


Figure 3- Locating Minimum Valid MDDR2-3A Read Data Window

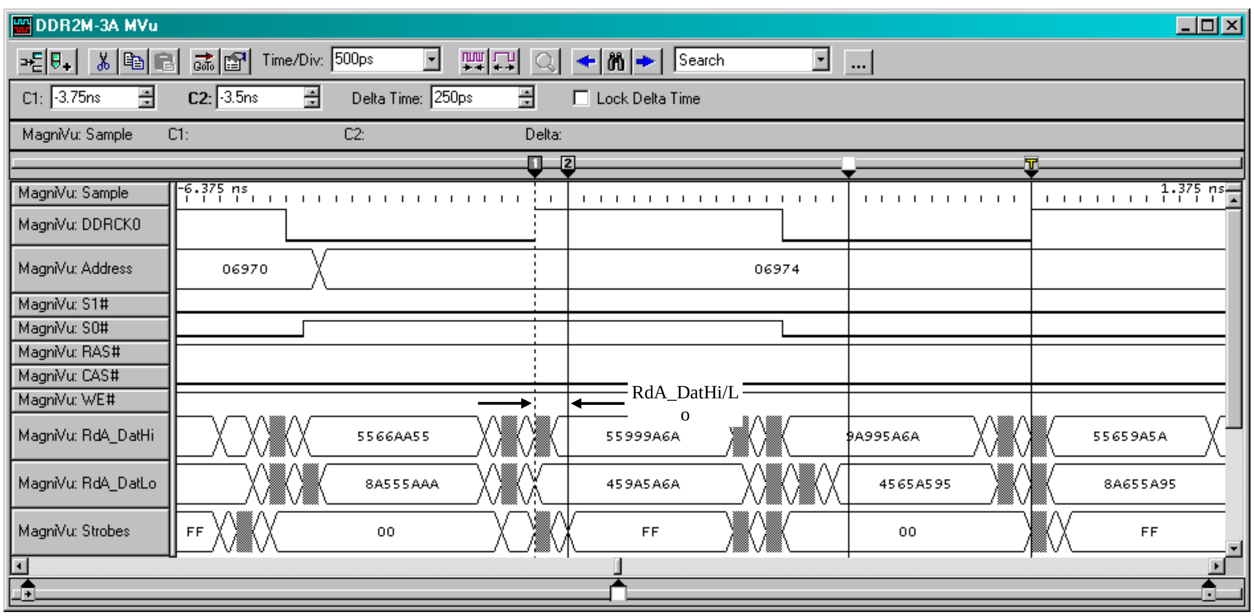


Figure 4- Measuring MDDR2-3A RdA_Dat/Hi/Lo Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 4) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is ~500ps, meaning that a suitable Setup & Hold value would be –500ps/1.125ns. Now the sample point for the RdB_DatHi and RdB_DatLo groups must be determined (see Figure 5). The next valid Read data (after the cycle measured above) occurs approximately 2.37ns after the rising edge of DDRCK0, so a suitable Setup & Hold value would be –2.375ns/3ns.

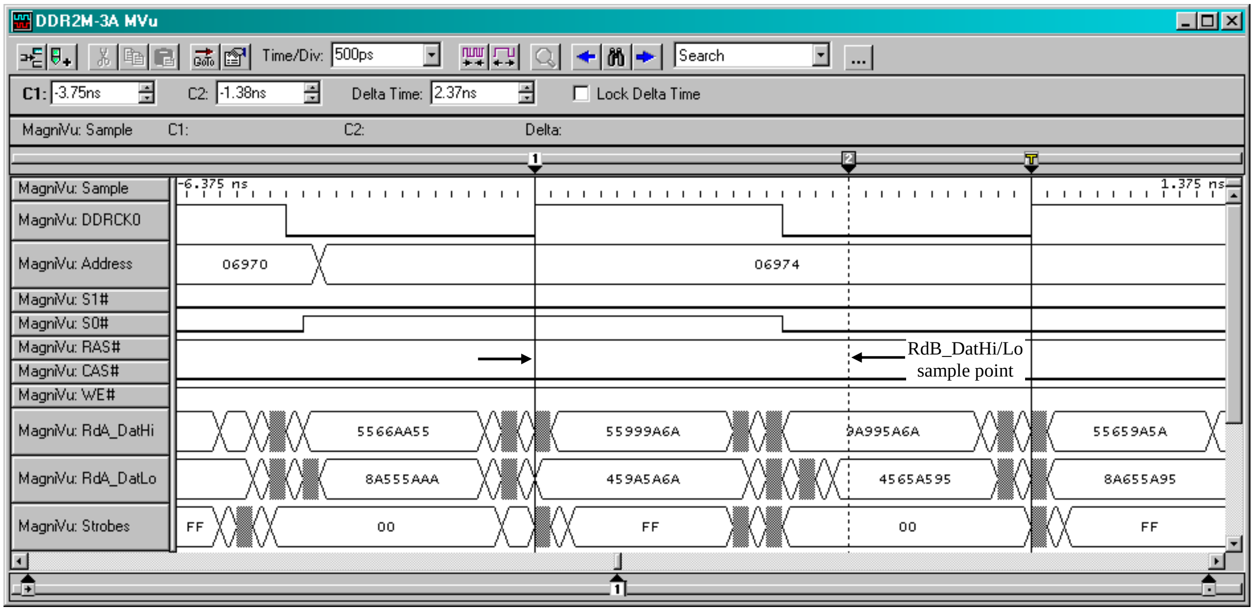


Figure 5- Measuring MDDR2-3A RdB_Dat/Hi/Lo Read Data Setup & Hold

Now the sample point positions must be set for the RdA_DatHi, RdA_DatLo, RdB_DatHi and RdB_DatLo groups in the Setup window. This window is found by going to the LA Card's Setup window, then clicking on the More button to the right of the clock select field. The TLA acquisition cards require a valid data window of 625ps, and this window can be placed to begin from 16.25ns prior to the clock edge to 7.625ns after the edge in 125ps increments. Each 32-bit data group (RdA_DatHi, RdA_DatLo, RdB_DatHi, RdB_DatLo) will require its own value programmed from the measurements noted in the MagniVu window (Figure 6).

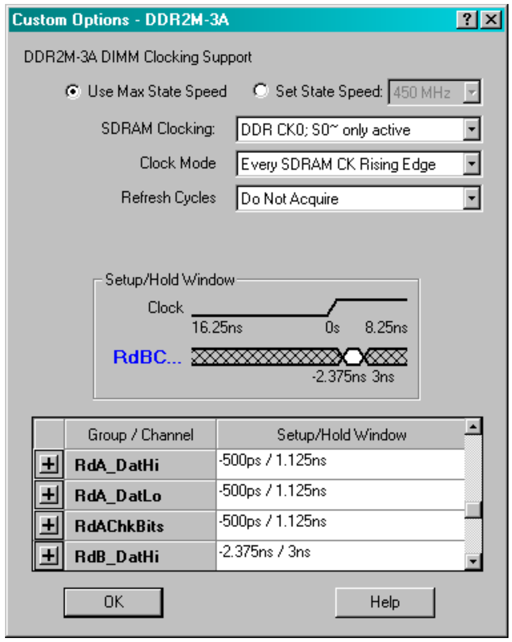


Figure 6- Setting MDDR2-3A RdA_DatHi/Lo and RdB_DatHi/Lo Sample Points

Setting the Setup & Hold values for acquiring Write data is a similar process. To determine the Write Data group sample points first make an appropriate acquisition of Write data by triggering on a Write Command cycle. Then create a timing window display of MagniVu data and display the two 32-bits groups RdA_DatHi, and RdA_DatLo along with the DDR clock that was used for the data acquisition (DDRCK0, DDRCK1, or DDRCK2).

Note: Because of the method used to acquire Write Data using the **MDDR2-3A** support, the MagniVu data from the RdA_DatHi/Lo data groups must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A "How DDR Data is Clocked".

A sample waveform display of MagniVu Write data is shown in Figure 7. To determine the sample point, locate the worst-case Setup & Hold timing of valid Write data during the acquired burst (note arrows in Figure 7). Refer to section 5.3 for important information on properly determining the Write data sample points.

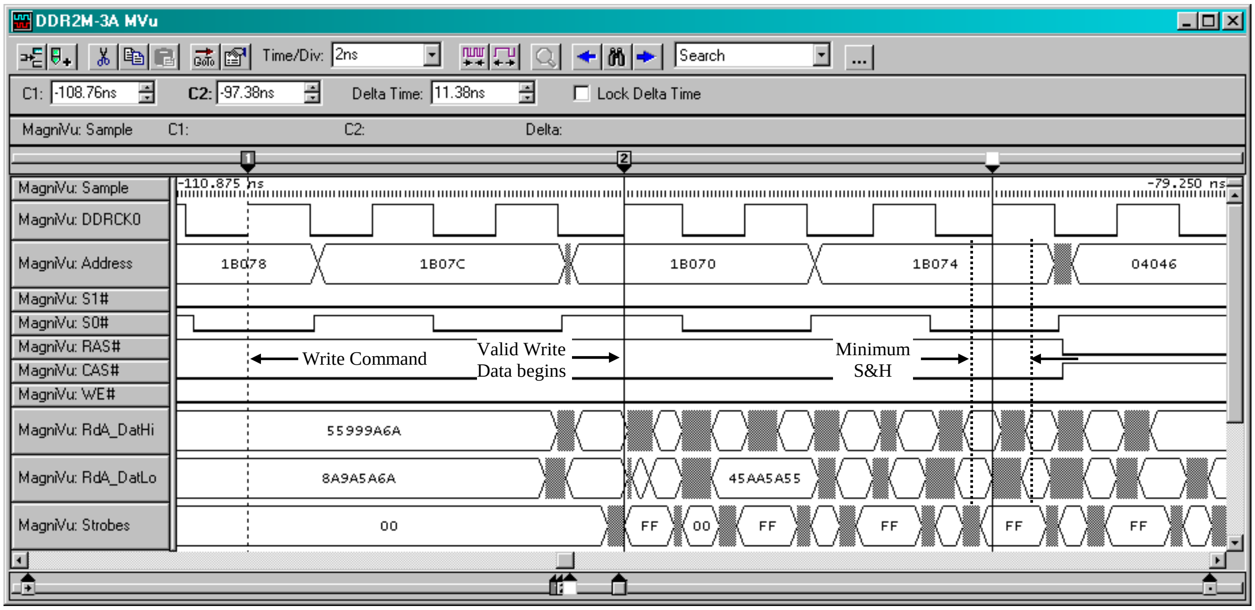


Figure 7- Locating Minimum Valid MDDR2-3A Write Data Window

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (Figure 8) and use the cursors to measure the time from the clock edge to the start of valid Write data. In this example the delay from edge to stable data transition is ~750ps, meaning that a suitable Setup & Hold value would be 750ps/-125ps.

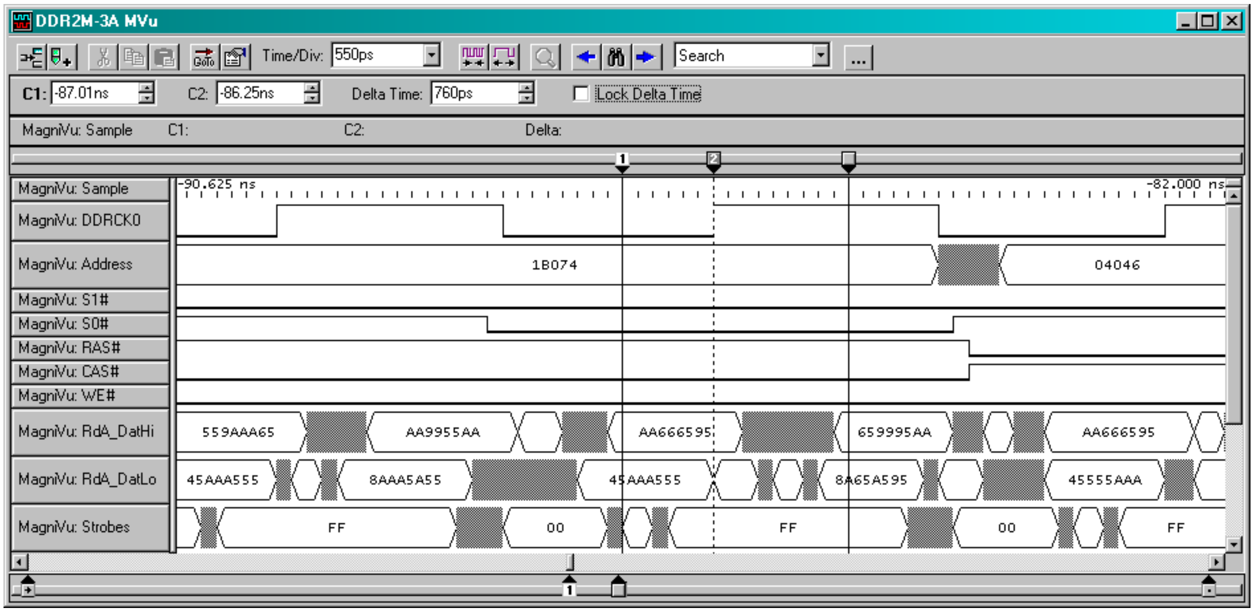


Figure 8- Measuring MDDR2-3A WrA_Dat/Hi/Lo Write Data Setup & Hold

Now the sample point for the WrB_DatHi and WrB_DatLo groups must be determined (see Figure 9). The next valid Write data (after the cycle measured above) occurs approximately 1.12ns after the rising edge of DDRCK0, so a suitable Setup & Hold value would be -1.125ns/1.750ns.

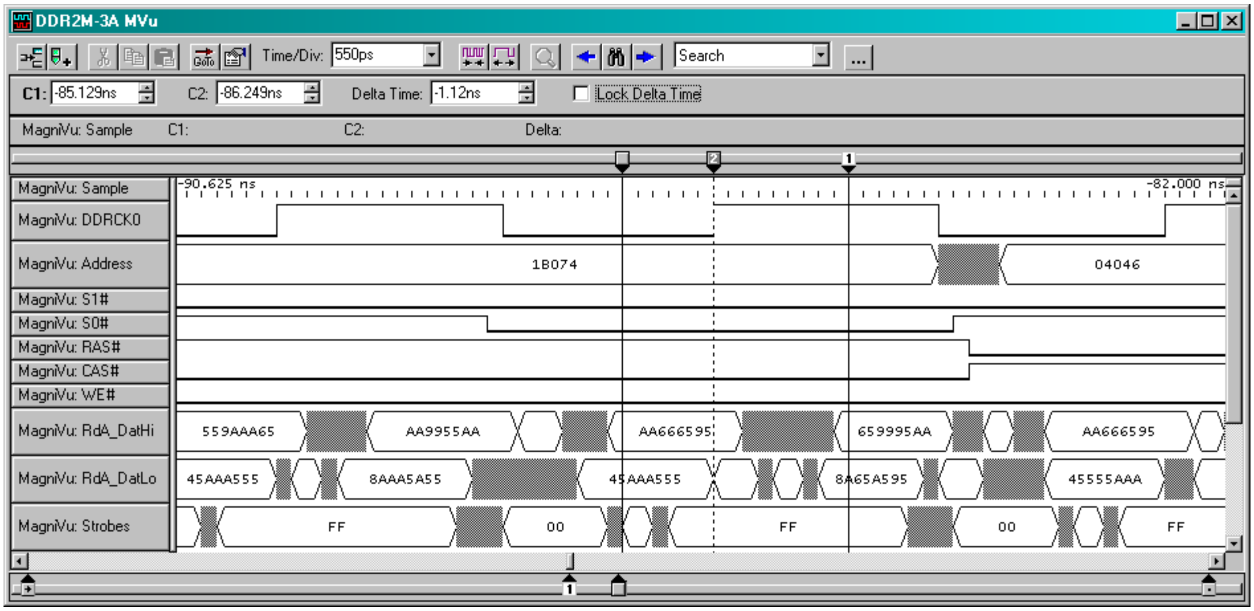


Figure 9- Measuring MDDR2-3A WrB_Dat/Hi/Lo Write Data Setup & Hold

The sample point positions must now be set for the WrA_DatHi, WrA_DatLo, WrB_DatHi, WrB_DatLo groups in the Setup window (Figure 10). Note that the WrtMasks group should have a Setup & Hold value that matches that of the Write Data groups.

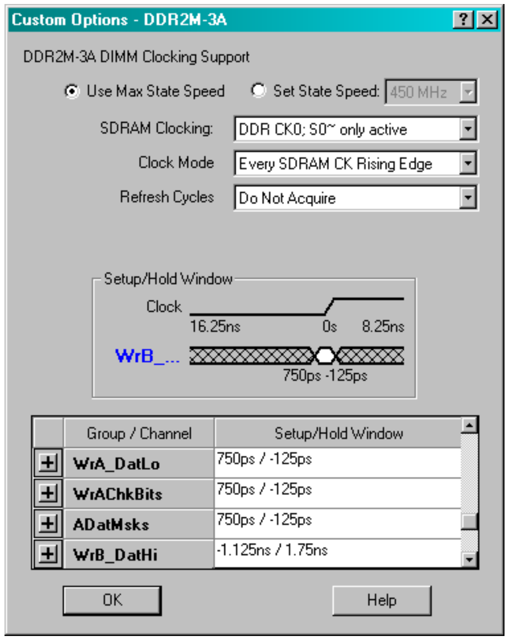


Figure 10- Setting MDDR2-3A WrA_DatHi/Lo and WrB_DatHi/Lo Sample Points

In rare instances it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. Figure 11 shows some of these additional data groups (RdADatB7-0) added to the same Waveform display shown in Figure 9. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see Figure 12). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit groups make up a 32-bit group.

Note: Again, it is very important to remember that, because of the method used to acquire Write Data using the **MDDR2-3A** support, the MagniVu data from the RdA_DatHi/Lo data groups must be used to determine both Read and Write sample points. For further explanation of this process refer to Appendix A “How DDR Data is Clocked”.

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group (RdADatHi, RdADatLo, RdBDatHi, RdBDatLo, WrADatHi, WrADatLo, WrBDatHi, WrBDatLo) be reset to “Support Package Default”. This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values – 625ps/0ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

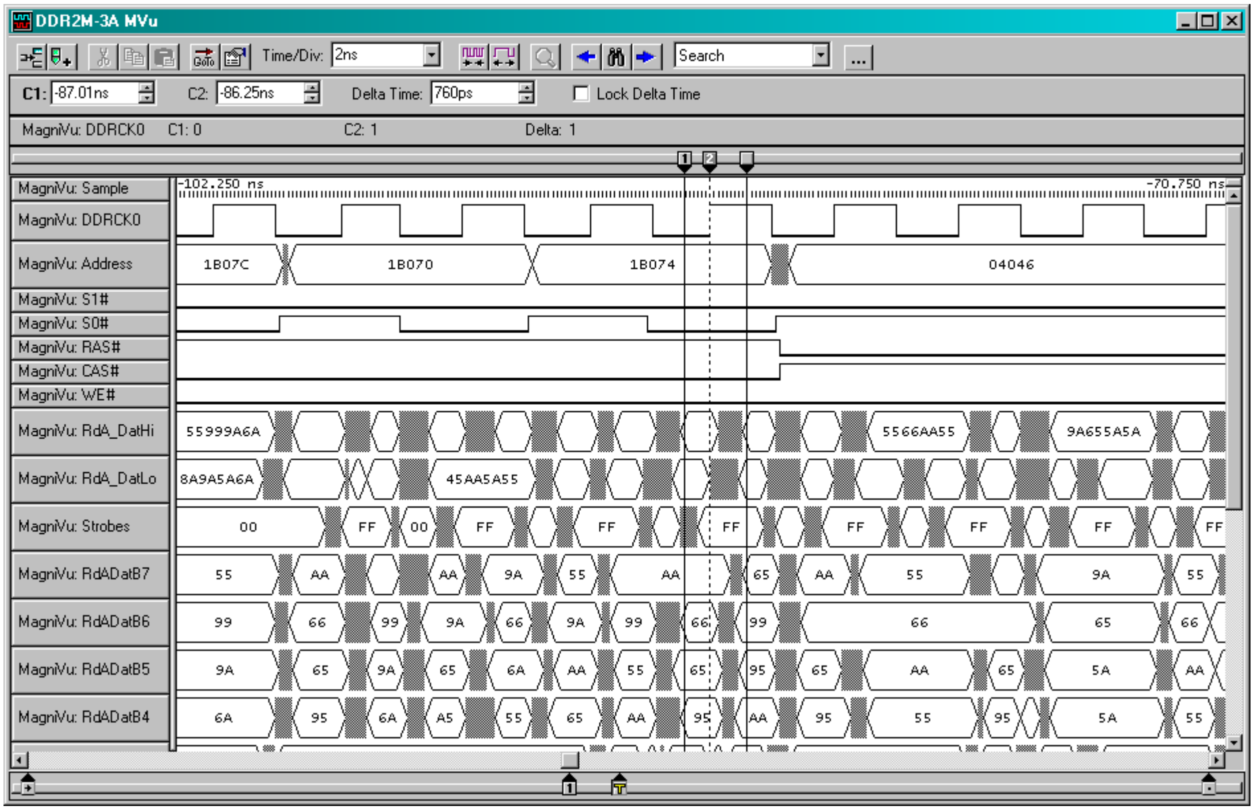


Figure 11- Viewing Individual 8-bit Read Data Groups

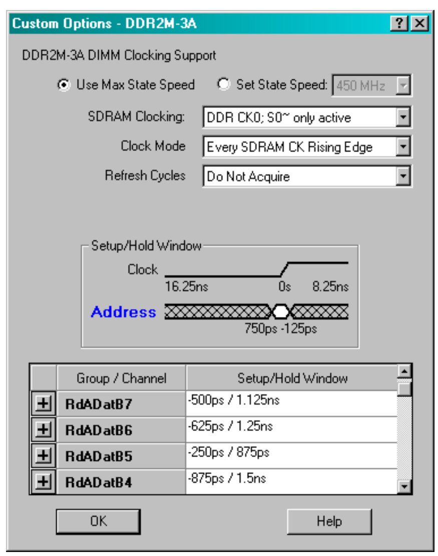


Figure 12- Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

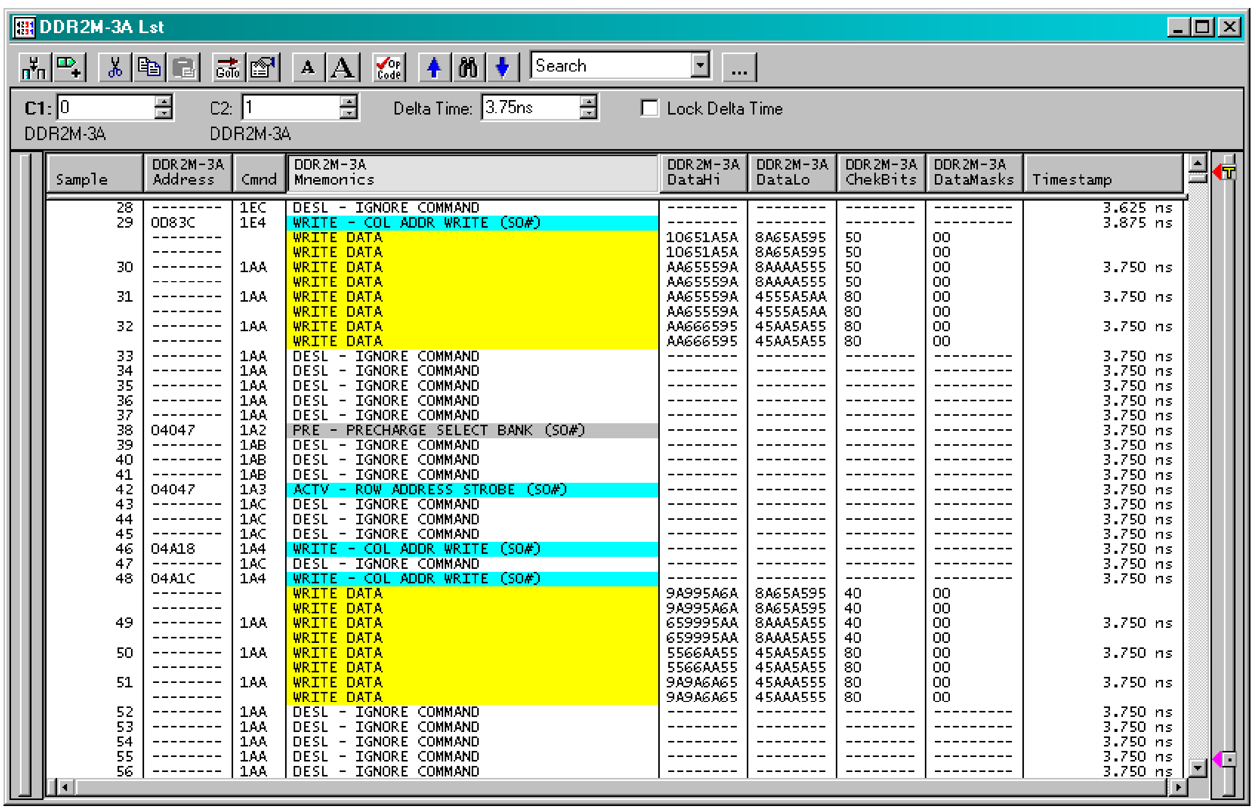
Note: Values shown are for illustration purposes only

6.0 VIEWING DATA

6.1 Viewing NEX-NVD2M667X8SRxR Data

When using the **NEX-NVD2M667X8SRxR** support packages the raw Address and Data groups are suppressed and are replaced with post-processed data in new groups. This data is displayed in new groups that have the support package name preceding it (i.e., **MDDR2-3A** Address, **MDDR2-3A** DataHi, etc.). The raw data groups are suppressed so that the display of data can be done in a more user-friendly fashion.

The Command group is suppressed because its function is replaced with a column labeled "**MDDR2-3A** Mnemonics", "DDR2M-2H Mnemonics" or "DDR2M-2J Mnemonics". The **NEX-NVD2M667X8SRxR** support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 13 shows the default **MDDR2-3A** display where all DDR data is displayed.



Sample	DDR2M-3A Address	Cmnd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChekBits	DDR2M-3A DataMasks	Timestamp
28	--------	1EC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.625 ns
29	0D83C	1E4	WRITE - COL ADDR WRITE (SO#)	--------	--------	--------	---------	3.875 ns
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
30	--------	1AA	WRITE DATA	AA65559A	8AAAA555	50	00	3.750 ns
	--------		WRITE DATA	AA65559A	8AAAA555	50	00	
31	--------	1AA	WRITE DATA	AA65559A	4555A5AA	80	00	3.750 ns
	--------		WRITE DATA	AA65559A	4555A5AA	80	00	
32	--------	1AA	WRITE DATA	AA666595	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	AA666595	45AA5A55	80	00	
33	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
34	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
35	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
36	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
37	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
38	04047	1A2	PRE - PRECHARGE SELECT BANK (SO#)	--------	--------	--------	---------	3.750 ns
39	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
40	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
41	--------	1AB	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
42	04047	1A3	ACTV - ROW ADDRESS STROBE (SO#)	--------	--------	--------	---------	3.750 ns
43	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
44	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
45	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (SO#)	--------	--------	--------	---------	3.750 ns
47	--------	1AC	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (SO#)	--------	--------	--------	---------	3.750 ns
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
49	--------	1AA	WRITE DATA	659995AA	8AAA5A55	40	00	3.750 ns
	--------		WRITE DATA	659995AA	8AAA5A55	40	00	
50	--------	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	5566AA55	45AA5A55	80	00	
51	--------	1AA	WRITE DATA	9A9A6A65	45AAA555	80	00	3.750 ns
	--------		WRITE DATA	9A9A6A65	45AAA555	80	00	
52	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
53	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
54	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
55	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns
56	--------	1AA	DESL - IGNORE COMMAND	--------	--------	--------	---------	3.750 ns

Figure 13- MDDR2-3A State Display

To change the display it is necessary to bring up the window's Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown below.

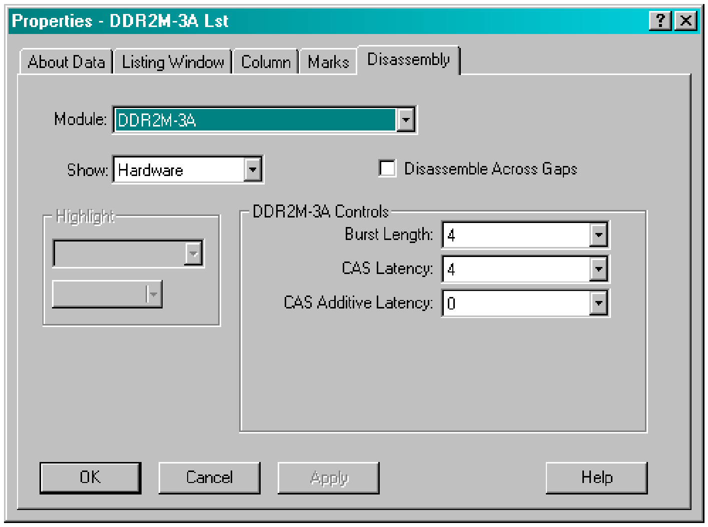


Figure 14- Disassembly Properties

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

Burst Length – permits setting the burst length for Read and Write data. Valid choices are 4 (the default) and 8. This value must be set properly for all valid Read and Write data to be displayed.

CAS Latency – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 2 (default), 3, 4, or 5 cycles.

CAS Additive Latency – additional latency for data cycles. This value must also be set properly for valid Read and Write Data to be displayed. Valid choices are 0 (default), 1, 2, 3, or 4 cycles.

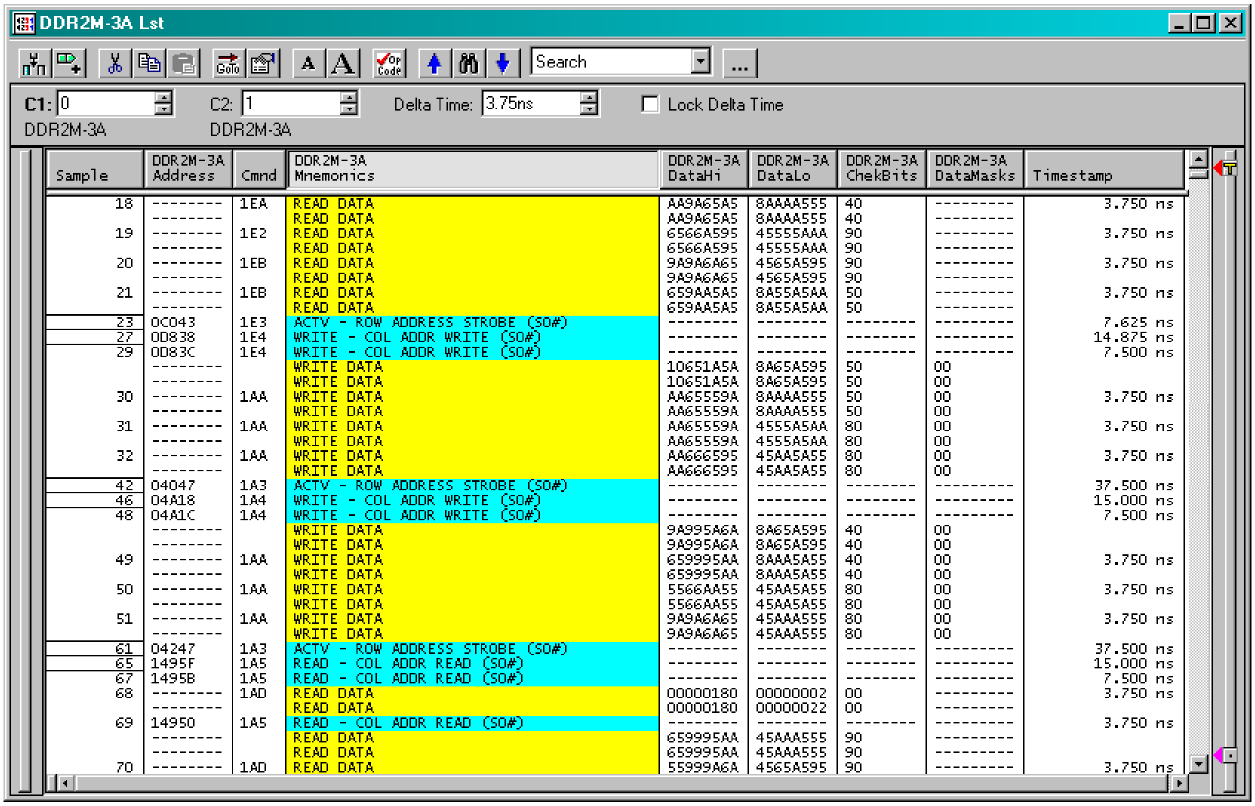
In addition to these Disassembly Properties selections, changing the settings in the **Show** field results in display changes as well:

Hardware – (default) displays all acquired cycles

Software – suppresses all idle or wait cycles

Control Flow – shows Address Command and valid Read / Write data cycles

Subroutine – shows valid Read / Write data cycles only



DDR2M-3A Lst

C1: 0 C2: 1 Delta Time: 3.75ns Lock Delta Time

DDR2M-3A DDR2M-3A

Sample	DDR2M-3A Address	Cmnd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChekBits	DDR2M-3A DataMasks	Timestamp
18	--------	1EA	READ DATA	AA9A65A5	8AAAA555	40	---------	3.750 ns
	--------		READ DATA	AA9A65A5	8AAAA555	40	---------	
19	--------	1E2	READ DATA	6566A595	45555AAA	90	---------	3.750 ns
	--------		READ DATA	6566A595	45555AAA	90	---------	
20	--------	1EB	READ DATA	9A9A6A65	4565A595	90	---------	3.750 ns
	--------		READ DATA	9A9A6A65	4565A595	90	---------	
21	--------	1EB	READ DATA	659AA5A5	8A55A5AA	50	---------	3.750 ns
	--------		READ DATA	659AA5A5	8A55A5AA	50	---------	
23	0C043	1E3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	7.625 ns
27	0D838	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	14.875 ns
29	0D83C	1E4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	7.500 ns
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
	--------		WRITE DATA	10651A5A	8A65A595	50	00	
30	--------	1AA	WRITE DATA	AA65559A	8AAAA555	50	00	3.750 ns
	--------		WRITE DATA	AA65559A	8AAAA555	50	00	
31	--------	1AA	WRITE DATA	AA65559A	4555A5AA	80	00	3.750 ns
	--------		WRITE DATA	AA65559A	4555A5AA	80	00	
32	--------	1AA	WRITE DATA	AA666595	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	AA666595	45AA5A55	80	00	
42	04047	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	37.500 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	15.000 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (S0#)	--------	--------	--------	---------	7.500 ns
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
	--------		WRITE DATA	9A995A6A	8A65A595	40	00	
49	--------	1AA	WRITE DATA	659995AA	8AAA5A55	40	00	3.750 ns
	--------		WRITE DATA	659995AA	8AAA5A55	40	00	
50	--------	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
	--------		WRITE DATA	5566AA55	45AA5A55	80	00	
51	--------	1AA	WRITE DATA	9A9A6A65	45AAA555	80	00	3.750 ns
	--------		WRITE DATA	9A9A6A65	45AAA555	80	00	
61	04247	1A3	ACTV - ROW ADDRESS STROBE (S0#)	--------	--------	--------	---------	37.500 ns
65	1495F	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	15.000 ns
67	1495B	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	7.500 ns
68	--------	1AD	READ DATA	00000180	00000002	00	---------	3.750 ns
	--------		READ DATA	00000180	00000022	00	---------	
69	14950	1A5	READ - COL ADDR READ (S0#)	--------	--------	--------	---------	3.750 ns
	--------		READ DATA	659995AA	45AAA555	90	---------	
	--------		READ DATA	659995AA	45AAA555	90	---------	
70	--------	1AD	READ DATA	55999A6A	4565A595	90	---------	3.750 ns

Figure 15- MDDR2-3A State Display- Control Flow

Changing the Show field setting in the display of Figure 13 from Hardware to Control Flow results in the display of Figure 15 where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

6.2 Viewing Raw DDR2 Data

In order to make the display of DDR2 data more user-friendly the raw data from the Address, all Data and other groups is suppressed in the Listing display. Instead the post-processing display software formats and reorders the data to tag and display valid DDR2 Address, Commands and Data. In the case of the **MDDR2-3A** support, which stores two Read and two Write data cycles in each TLA Sample location, the data is reordered chronologically in the display with the oldest data being shown on the line above the newer data.

To see the raw data using any of the **NEX-NVD2M667X8SRxR** support packages perform a right mouse click in the Listing window, select **Add Column…** then click on the group to be added. Refer to the TLA User's Manual or online help for further information on added or deleting data groups.

6.3 MDDR2-3A Mnemonics Description

Table 4 gives a brief description of each of the text lines displayed in the post-processing software display.

Mnemonic	Description
ACTV - ROW ADDRESS STROBE (S0~)	Active command – activate a row in a bank for subsequent access (chip select 0)
ACTV - ROW ADDRESS STROBE (S1~)	Active command – activate a row in a bank for subsequent access (chip select 1)
BST - BURST STOP (S0~)	Burst Terminate command – truncate current Read burst (chip select 0)
BST - BURST STOP (S1~)	Burst Terminate command – truncate current Read burst (chip select 1)
DESL - IGNORE COMMAND	Deselect function – no new command
MRS - MODE REGISTER SET (S0~)	Mode Register Set command – mode register load (chip select 0)
MRS - MODE REGISTER SET (S1~)	Mode Register Set command – mode register load (chip select 1)
NOP - NO OPERATION (S0~)	No Operation command (chip select 0)
NOP - NO OPERATION (S1~)	No Operation command (chip select 1)
PRE - PRECHARGE SELECT BANK (S0~)	Precharge command (chip select 0)
PRE - PRECHARGE SELECT BANK (S1~)	Precharge command (chip select 1)
READ - COL ADDR READ (S0~)	Read command – initiates a burst read access to active row (chip select 0)
READ - COL ADDR READ (S1~)	Read command – initiates a burst read access to active row (chip select 1)
READ DATA	Valid Read data on the bus
REF - REFRESH (S0~)	Self Refresh command (chip select 0)
REF - REFRESH (S1~)	Self Refresh command (chip select 1)
WRITE - COL ADDR WRITE (S0~)	Write command – initiates a burst write access to active row (chip select 0)
WRITE - COL ADDR WRITE (S1~)	Write command – initiates a burst write access to active row (chip select 1)
WRITE DATA	Valid Write data on the bus
(UNKNOWN)	Command Cycle on falling edge of clock

Table 4- MDDR2-3A Mnemonics Definition

6.4 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: **MDDR2-3A and MDDR2-3A MagniVu**. The M**DR2-3A** selection shows the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. MagniVu is very useful and in some cases necessary to see/resolve DDR data. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

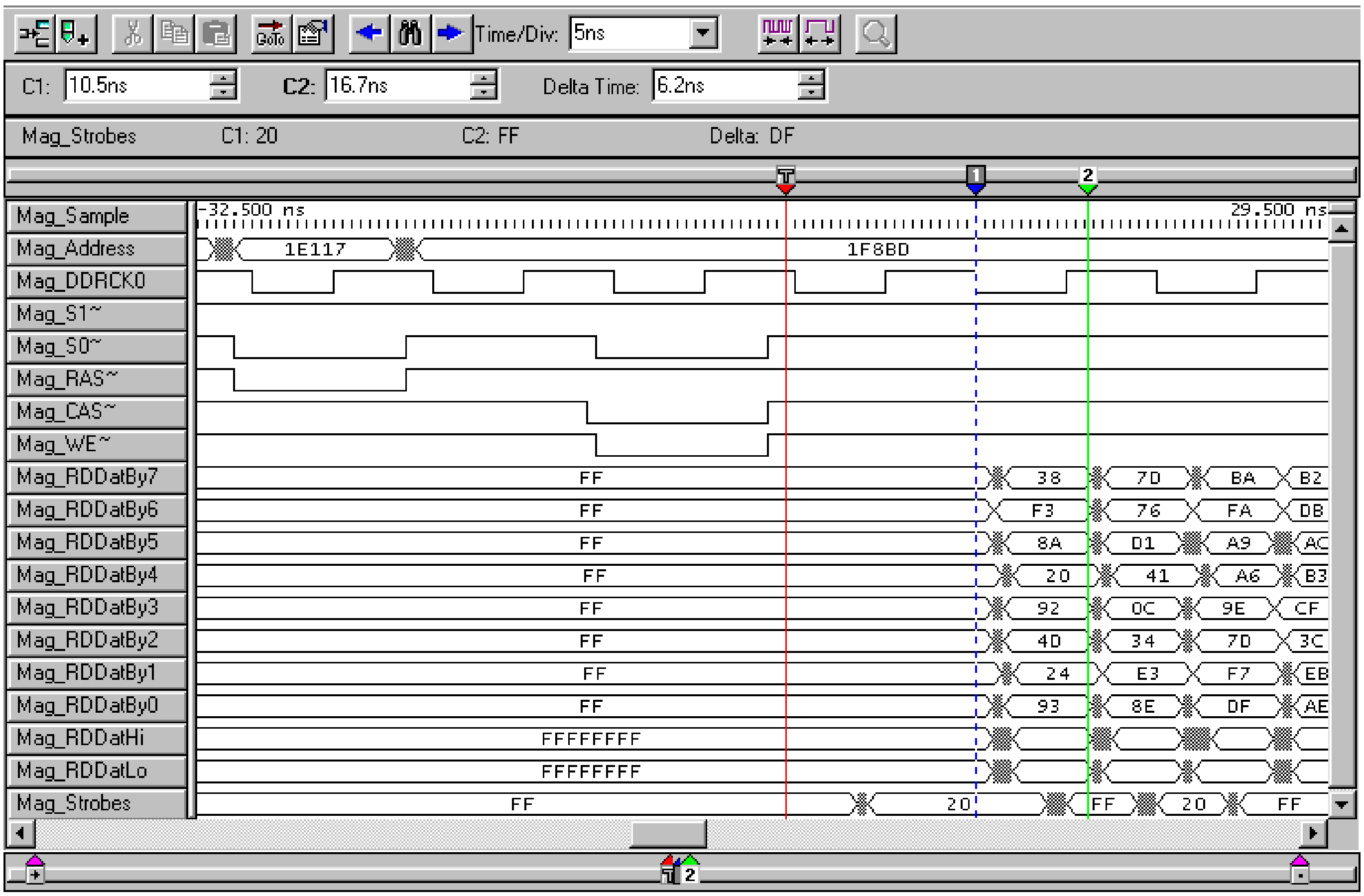


Figure 16- MDDR2-3A MagniVu Display on TLA

7.0 HINTS & TIPS

7.1 Symbolic Triggering on a Command using the NEX-NVD2M667X8SRxR Supports

A Symbol Table has been included in the support packages for the Control data group (see Table 5). The use of Symbol Tables when triggering makes it easier for the user to define a given cycle to be triggered on. Rather than trying to remember what signals make up the Command group, the Symbol Table has the appropriate bits already set for the given cycle.

It is important to note that changing the group, channel, or wiring of the Command group can result in incorrect symbol information being displayed.

Symbol	Definition
DESL--IGNORE_COMMAND--DATA?	x1 xxx
NOP--NO_OPERATION)	10 111
BST--BURST_STOP	10 110
READ--COL_ADDR_READ	10 101
WRITE--COL_ADDR_WRITE	10 100
ACTV--ROW_ADDRESS_STROBE	10 011
PRE--PRECHARGE_SELECT_BANK	10 010
PALL--PRECHARGE_ALL_BANK	10 010
REF--REFRESH	10 001
MRS--MODE_REGISTER_SET	10 000

Signals, left-to-right: CKE0, S0#, RAS#, CAS#, WE#

Table 5- MDDR2-3A Control Symbol Table

7.2 Installing Memories in a blank DIMM

If the user purchases a DIMM that will be configurable with alternate memory Vendor parts, or if the user wished to change memories on a purchased DIMM they should consider the flowing:

- The memory must be of the same configuration as the DIMM was designed for. Said another way, make sure that the memory that you are going to mount has the same data width configuration as the Module was designed for.
- Use a BGA rework station that has the ability to see the board and the replacement chip at the same time. This normally includes a prism / light alignment system.
- Nexus can recommend a vendor for BGA rework if you do not have the facilities. Please contact us for additional information.

7.3 Capturing MRS (Mode Register Set) Data

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the **NEX-NVD2M667X8SRxR** supports for the post-processing software to properly decode the acquisitions. The TLA trigger shown in Figure 17 can be used to acquire the MRS cycles when using either of these supports.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

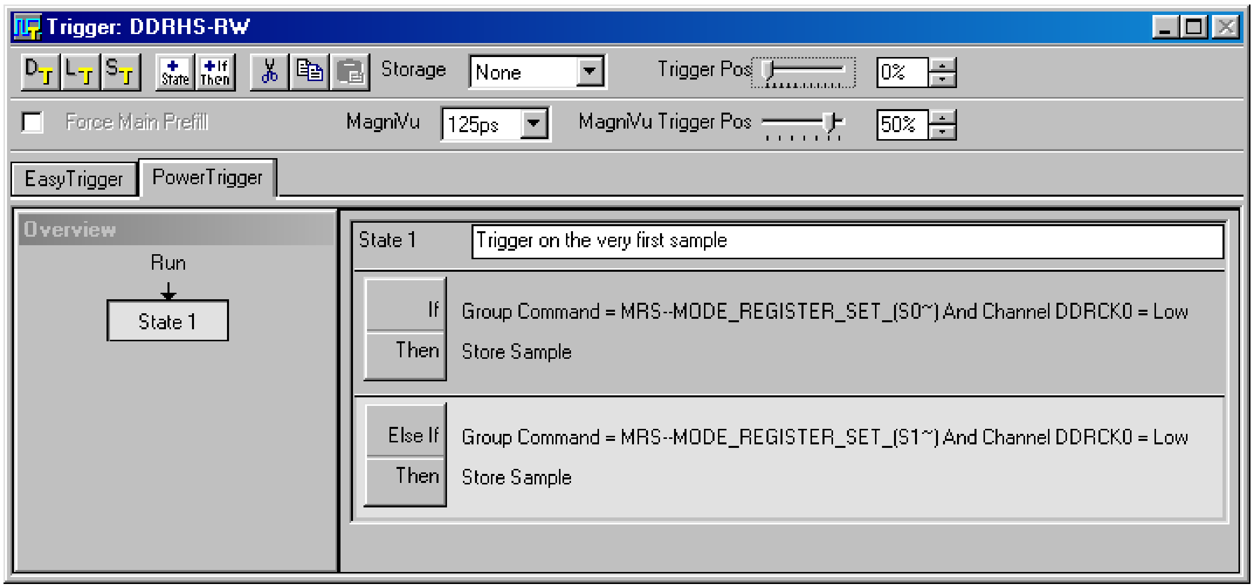


Figure 17- MDDR2-3A MRS Trigger

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in Figure 18. The last acquired MRS cycle will reflect the settings used in the DDR target – in this case, a CAS latency of 2 cycles with a Burst length of 8.

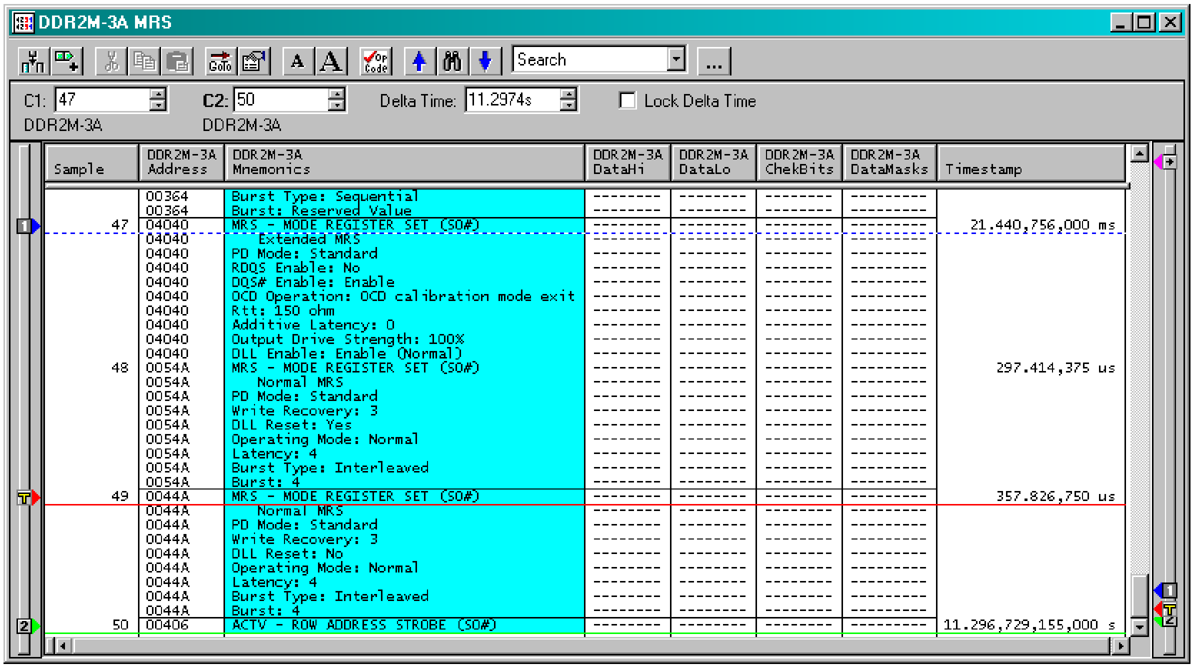


Figure 18- MRS Cycle Acquisition Disassembly

8.0 DEBUGGING HINTS

8.1 Required NEXVu-DIMM that is Unavailable

Nexus Technology is pursuing this new NEXVu-DIMM approach for debug with the belief that old fashioned Interposers and built-in foot prints on motherboards will not reliably capture DDRII signals above 400MT/s. While we have a growing variety of NEXVu-DIMMs available there is the possibility that we do not have the variation of DIMM that may be needed for a specific debug task. To help facilitate our customers we are working hard to increase the variety of NEXVu-DIMMs available. If the NEXVu-DIMM you desire is not available Nexus recommends the debug techniques listed below:

1. Each major family of NEXVu-DIMMs supported by Nexus Technology will have an NEXVu-DIMM available that has not been populated with memory components. This DIMM can be custom configured by the customer to a desired configuration by the addition of memory chips that may be available to the customer but not to Nexus.

2. In user testing a customer may have a DIMM that is exhibiting a problem. The equivalent NEXVu-DIMM may not exhibit the problem for a number of reasons. Among these reason are:
    a. Problem DIMM has a different version level of memory chips available

    b. Problem DIMM has an alternate vendor's memory chips.

Facing this situation the customer has the option of:

1. Implementing the suggestion in bullet #1 above.

2. Using to signals available in an adjacent NEXVu-DIMM to trigger on a known Address/Data access to the Problem DIMM and then view the timing measurements in the Logic Analyzers MagniVu Timing display – realizing that the timing at the adjacent NEXVu-DIMM is slightly different from that of the problem DIMM. NOTE: Some signals, like RAS#, may go low in idle cycles making triggering difficult.

3. Use the Logic Analyzer connection pads on an adjacent NEXVu-DIMM for an easy connection point for a high quality scope to view the DDRII signals and determine the signal quality. This can be easily done by using the Analog Mux feature of the Tektronix Logic Analyzer where selected inputs to the Logic Analyzer module may be passed through to an external oscilloscope for analog analysis.

8.2 Handling the NEXVu-DIMM

The NEXVu-DIMMs have the memory chips under-filled (memory chips held in place with an epoxy-like glue) to protect them from contact fractures caused by torque from the Logic Analyzer probe. However, care must still be taken to avoid excessive torque on the NEXVu-DIMMs by the Logic Analyzer probes to prevent damage to the DIMM.

User Configurable NEXVu-DIMMs will not have under-fill, thus extra care must be taken to avoid torque on the NEXVu-DIMM by the Logic Analyzer probes.

APPENDIX A - How DDR Data is Clocked

A.1 Background

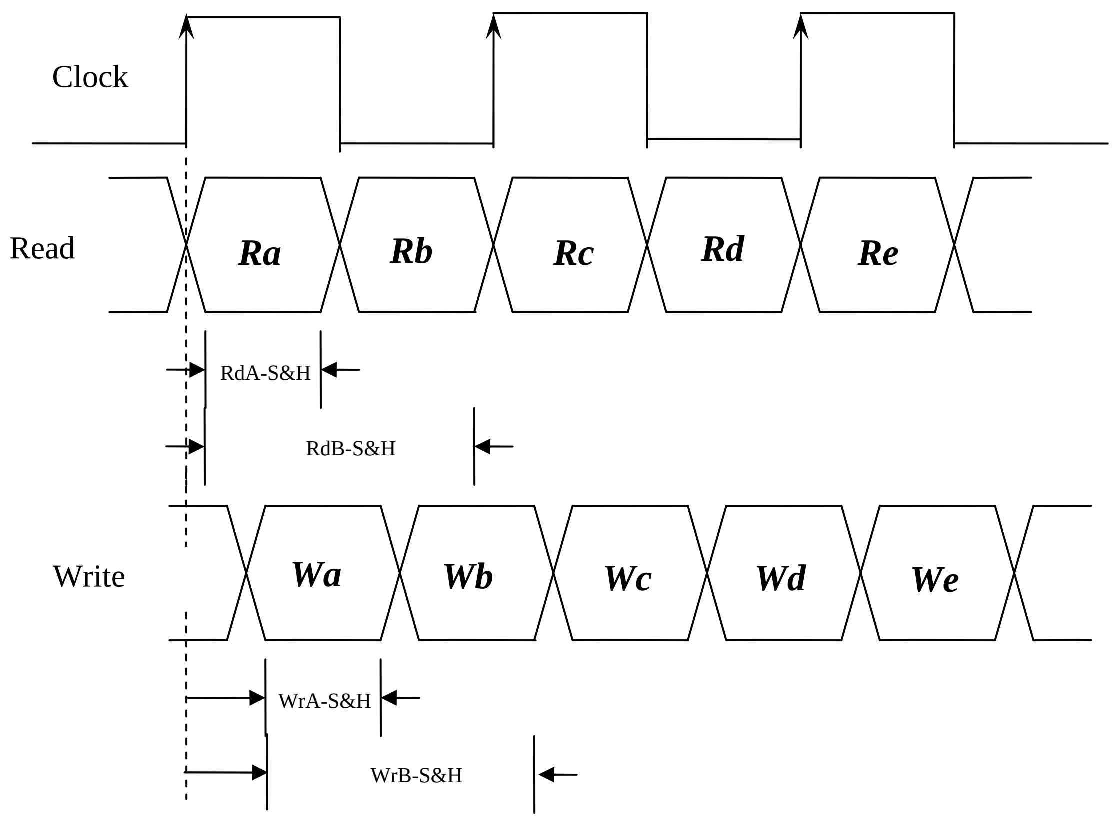
Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two or four separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section ***and*** the D3 section. Using 4X demux, connections made to the A3 channels permit data to be stored in the A3, A2, D3 and D2 sections. A very useful side benefit of using demux is that, since only one set of TLA data channels has to be connected, only one probe load is added to the target, even though data is stored in two or four different locations of the acquisition card.

A.2 DDR Acquisition - General

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. The speeds of DDR (400 and 667MT/s) require different setups to enable proper data acquisition. In addition, instead of trying to use the 8 Data Strobes to acquire data our solution uses one of the DDR SDRAM Clocks (either CK0 or CK1, user selectable) and all data acquisition is adjusted in relation to the clock edges. The 8 Data Strobes cannot be easily used to acquire data as some TLA configurations only support 4 Clock Inputs. Also, the Strobes cannot be used to acquire Address and Command information.

A.3 MDDR2-3A Support

This support requires three (3) merged 136-channel 450MHz acquisition cards used in a TLA7XX logic analyzer. Data is acquired using the rising edge of the 266MHz DDR clock, and 4X demultiplexing is done to permit acquiring two samples each of 64-bit Read and Write data relative to the clock edge (for a total of 4 64-bit data samples for each DDR clock cycle). A_Data information is earlier (older) data than the information stored in B_Data. Again, different Sample Points must be set for each of the four 32-bit Data groups, and again, if necessary, sample points can be set for any of the 8-bit data groups.



APPENDIX B - Considerations

B.1 NEX-NVD2M667X8SRXR Bus Loading

It must be noted that the **NEX-NVD2M667X8SRXR** NEXVu-DIMMs are designed to meet JEDEC standards. The acquired signals are sampled at the pins of the memory chips, and then passed through stub resistors to reduce capacitive loading. The NEXVu-DIMM has been tested via detailed simulations, and by actual in circuit testing.

Unlike Interposers that were commonly used at slower frequencies, the NEXVu-DIMM does not add to the signal lengths from the memory control to the DIMM, thus ensuring correct system operation.

APPENDIX C - NEX-NVD2M667X8SRXR Distributed Probe Pinouts

Samtec Pin	Coax Pin	TLA Channel	DDR3 Signal	DIMM Pin #	Samtec Pin	Coax Pin	TLA Channel	DDR3 Signal	DIMM Pin #
46	J16-6	CK0+			46	J16-6	CK1+		
32	J16-10	A3:7			32	J16-10	A1:7		
36	J16-9	A3:6	DM2	148	36	J16-9	A1:6		
33	J15-11	A3:5	DQS3#	36	33	J15-11	A1:5		
37	J15-12	A3:4	DQS3	37	37	J15-12	A1:4		
40	J16-8	A3:3			40	J16-8	A1:3		
42	J16-7	A3:2	DM3	157	42	J16-7	A1:2	DM6	227
41	J15-13	A3:1			41	J15-13	A1:1	DQS6#	106
45	J15-14	A3:0			45	J15-14	A1:0	DQS6	107
49	J15-15	A2:7	DQS8#	45	49	J15-15	A0:7		
51	J15-16	A2:6	DQS8	46	51	J15-16	A0:6		
50	J16-5	A2:5			50	J16-5	A0:5		
52	J16-4	A2:4			52	J16-4	A0:4		
55	J15-17	A2:3			55	J15-17	A0:3	DQS7#	115
57	J15-18	A2:2			57	J15-18	A0:2	DQS7	116
56	J16-3	A2:1	DM8	166	56	J16-3	A0:1		
58	J16-2	A2:0			58	J16-2	A0:0	DM7	236
15	J15-6	Q0+			15	J15-6	CK2+		
29	J15-10	D3:7			29	J15-10	D1:7	DQS5	95
25	J15-9	D3:6			25	J15-9	D1:6	DQS5#	94
28	J16-11	D3:5			28	J16-11	D1:5		
24	J16-12	D3:4			24	J16-12	D1:4		
21	J15-8	D3:3	DQS2	28	21	J15-8	D1:3		
19	J15-7	D3:2	DQS2#	27	19	J15-7	D1:2		
20	J16-13	D3:1	DM1	136	20	J16-13	D1:1	DM5	215
16	J16-14	D3:0			16	J16-14	D1:0		
12	J16-15	D2:7	DQS1	16	12	J16-15	D0:7		
10	J16-16	D2:6	DQS1#	15	10	J16-16	D0:6		
11	J15-5	D2:5			11	J15-5	D0:5	DQS4	86
9	J15-4	D2:4			9	J15-4	D0:4	DQS4#	85
6	J16-17	D2:3			6	J16-17	D0:3	DM4	206
4	J16-18	D2:2	DM0	127	4	J16-18	D0:2		
5	J15-3	D2:1	DQS0	7	5	J15-3	D0:1		
3	J15-2	D2:0	DQS0#	6	3	J15-2	D0:0		

Probe Connection
M - A3/A2/D3/D2

Probe Connection
M - A1/A0/D1/D0

APPENDIX C - NEX-NVD2M667X8SRXR Distributed Probe Pinouts (cont'd.)

Samtec Pin	Coax Pin	TLA Channel	DDR3 Signal	DIMM Pin #	Samtec Pin	Coax Pin	TLA Channel	DDR3 Signal	DIMM Pin #
46	J16-6	CK3+	CKO	188	46	J16-6	Q3+		
32	J16-10	C3:7	A6	183	32	J16-10	E3:7	NC__CB7	
36	J16-9	C3:6	A3	185	36	J16-9	E3:6	NC__CB6	
33	J15-11	C3:5	A4	62	33	J15-11	E3:5	NC__CB3	
37	J15-12	C3:4	A2	64	37	J15-12	E3:4	NC__CB2	
40	J16-8	C3:3	A1	186	40	J16-8	E3:3	NC__CB5	
42	J16-7	C3:2	A0	191	42	J16-7	E3:2	NC__CB4	
41	J15-13	C3:1	PAR_In		41	J15-13	E3:1	NC__CB1	
45	J15-14	C3:0	A10/AP	70	45	J15-14	E3:0	NC__CB0	
49	J15-15	C2:7	BA0	71	49	J15-15	E2:7		
51	J15-16	C2:6	OIDT		51	J15-16	E2:6		
50	J16-5	C2:5	BA1	192	50	J16-5	E2:5		
52	J16-4	C2:4	A13	199	52	J16-4	E2:4		
55	J15-17	C2:3	WE#	73	55	J15-17	E2:3		
57	J15-18	C2:2	CAS#	75	57	J15-18	E2:2		
56	J16-3	C2:1	RAS#	194	56	J16-3	E2:1		
58	J16-2	C2:0	S0#	196	58	J16-2	E2:0		
15	J15-6	Q1+	CKE0	53	15	J15-6	Q2+		
29	J15-10	C1:7	A5	61	29	J15-10	E1:7		
25	J15-9	C1:6	A7	59	25	J15-9	E1:6		
28	J16-11	C1:5	A8	182	28	J16-11	E1:5		
24	J16-12	C1:4	A9	180	24	J16-12	E1:4		
21	J15-8	C1:3	A11	58	21	J15-8	E1:3		
19	J15-7	C1:2	BA2	55	19	J15-7	E1:2		
20	J16-13	C1:1	A12	179	20	J16-13	E1:1		
16	J16-14	C1:0	A14	177	16	J16-14	E1:0		
12	J16-15	C0:7			12	J16-15	E0:7		
10	J16-16	C0:6	A15	176	10	J16-16	E0:6		
11	J15-5	C0:5	RA1		11	J15-5	E0:5		
9	J15-4	C0:4	RA0		9	J15-4	E0:4		
6	J16-17	C0:3			6	J16-17	E0:3		
4	J16-18	C0:2			4	J16-18	E0:2		
5	J15-3	C0:1	RCS		5	J15-3	E0:1		
3	J15-2	C0:0	RCAS		3	J15-2	E0:0		

Probe Connection M - C3/C2/C1/C0

Probe Connection M - E3/E2/E1/E0

APPENDIX C - NEX-NVD2M667X8SRXR Distributed Probe Pinouts (cont'd.)

Samtec Pin	Coax Pin	TLA Channel	DDR 3 Signal	DIMM Pin #	Samtec Pin	Coax Pin	TLA Channel	DDR 3 Signal	DIMM Pin #
46	J16-6	CK3+			46	J16-6	CK3+		
32	J16-10	C3:0	DQ15	143	32	J16-10	C3:0	DQ47	219
36	J16-9	C3:1	DQ14	142	36	J16-9	C3:1	DQ46	218
33	J15-11	E3:7	DQ11	22	33	J15-11	E3:7	DQ43	98
37	J15-12	E3:6	DQ10	21	37	J15-12	E3:6	DQ42	97
40	J16-8	C3:2	DQ13	134	40	J16-8	C3:2	DQ45	213
42	J16-7	C3:3	DQ12	133	42	J16-7	C3:3	DQ44	212
41	J15-13	E3:5	DQ9	13	41	J15-13	E3:5	DQ41	92
45	J15-14	E3:4	DQ8	12	45	J15-14	E3:4	DQ40	91
49	J15-15	E3:3	DQ3	10	49	J15-15	E3:3	DQ35	89
51	J15-16	E3:2	DQ2	9	51	J15-16	E3:2	DQ34	88
50	J16-5	C3:4	DQ7	131	50	J16-5	C3:4	DQ39	210
52	J16-4	C3:5	DQ6	130	52	J16-4	C3:5	DQ38	209
55	J15-17	E3:1	DQ1	4	55	J15-17	E3:1	DQ33	83
57	J15-18	E3:0	DQ0	3	57	J15-18	E3:0	DQ32	82
56	J16-3	C3:6	DQ5	125	56	J16-3	C3:6	DQ37	204
58	J16-2	C3:7	DQ4	124	58	J16-2	C3:7	DQ36	203
15	J15-6	CK1+			15	J15-6	CK1+		
29	J15-10	A1:0	DQ16	24	29	J15-10	A1:0	DQ48	100
25	J15-9	A1:1	DQ17	25	25	J15-9	A1:1	DQ49	101
28	J16-11	A3:7	DQ20	145	28	J16-11	A3:7	DQ52	221
24	J16-12	A3:6	DQ21	146	24	J16-12	A3:6	DQ53	222
21	J15-8	A1:2	DQ18	30	21	J15-8	A1:2	DQ50	109
19	J15-7	A1:3	DQ19	31	19	J15-7	A1:3	DQ51	110
20	J16-13	A3:5	DQ22	151	20	J16-13	A3:5	DQ54	230
16	J16-14	A3:4	DQ23	152	16	J16-14	A3:4	DQ55	231
12	J16-15	A3:3	DQ28	154	12	J16-15	A3:3	DQ60	233
10	J16-16	A3:2	DQ29	155	10	J16-16	A3:2	DQ61	234
11	J15-5	A1:4	DQ24	33	11	J15-5	A1:4	DQ56	112
9	J15-4	A1:5	DQ25	34	9	J15-4	A1:5	DQ57	113
6	J16-17	A3:1	DQ30	160	6	J16-17	A3:1	DQ62	239
4	J16-18	A3:0	DQ31	161	4	J16-18	A3:0	DQ63	240
5	J15-3	A1:6	DQ26	39	5	J15-3	A1:6	DQ58	118
3	J15-2	A1:7	DQ27	40	3	J15-2	A1:7	DQ59	119

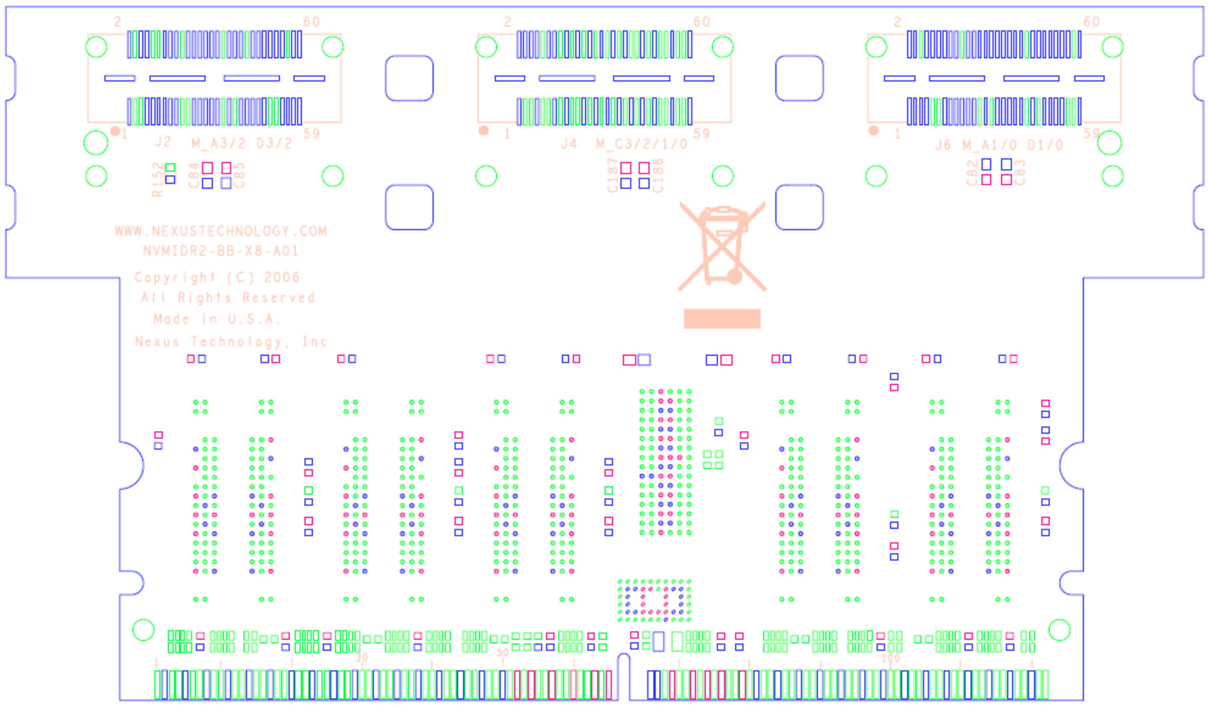
Probe Connection S - C3/E3/A1/A3 | **Probe Connection S2 - C3/E3/A1/A3**

APPENDIX D - MiniDIMM pinout

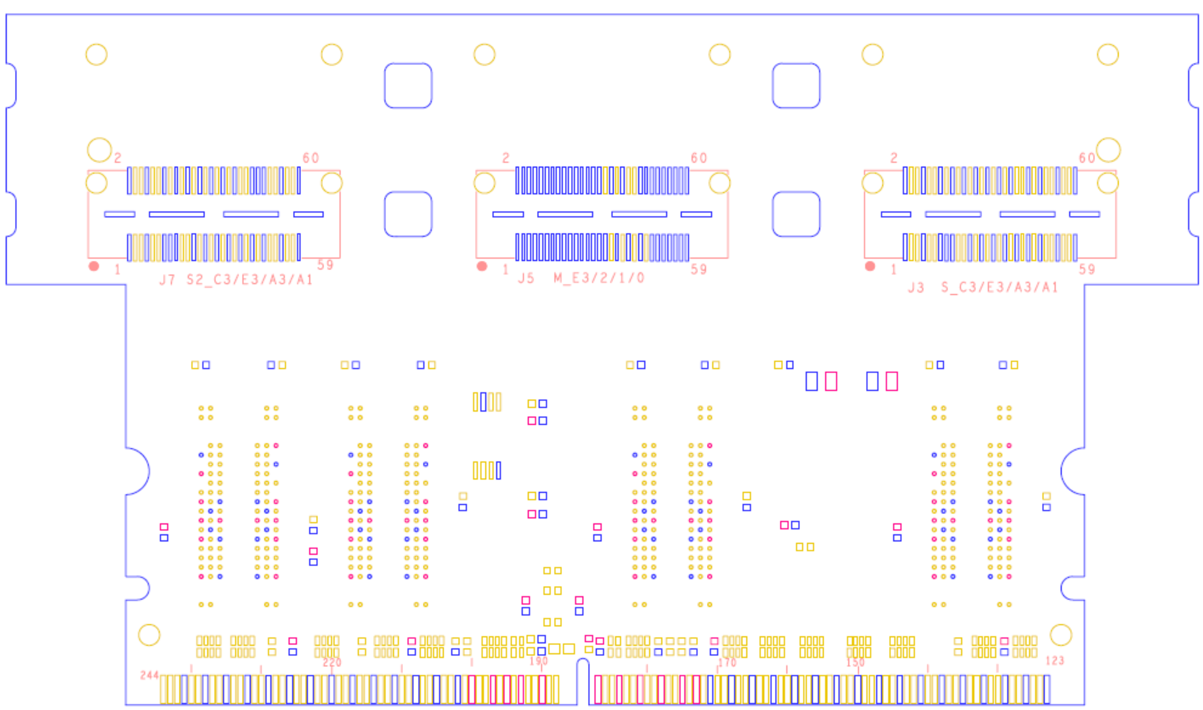
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{REF}	123	V_{SS}	32	V_{SS}	154	DQ28	63	V_{DDQ}	185	A3	92	DQ41	214	V_{SS}
2	V_{SS}	124	DQ4	33	DQ24	155	DQ29	64	A2	186	A1	93	V_{SS}	215	DM5
3	DQ0	125	DQ5	34	DQ25	156	V_{SS}	65	V_{DD}	187	V_{DD}	94	$\overline{DQS5}$	216	NC
4	DQ1	126	V_{SS}	35	V_{SS}	157	DM3	KEY				95	DQS5	217	V_{SS}
5	V_{SS}	127	DM0	36	$\overline{DQS3}$	158	NC					96	V_{SS}	218	DQ46
6	$\overline{DQS0}$	128	NC	37	DQS3	159	V_{SS}	66	V_{SS}	188	CK0	97	DQ42	219	DQ47
7	DQS0	129	V_{SS}	38	V_{SS}	160	DQ30	67	V_{SS}	189	$\overline{CK0}$	98	DQ43	220	V_{SS}
8	V_{SS}	130	DQ6	39	DQ26	161	DQ31	68	NC	190	V_{DD}	99	V_{SS}	221	DQ52
9	DQ2	131	DQ7	40	DQ27	162	V_{SS}	69	V_{DD}	191	A0	100	DQ48	222	DQ53
10	DQ3	132	V_{SS}	41	V_{SS}	163	CB4	70	A10/ AP	192	BA1	101	DQ49	223	V_{SS}
11	V_{SS}	133	DQ12	42	CB0	164	CB5	71	BA0	193	V_{DD}	102	V_{SS}	224	RFU
12	DQ8	134	DQ13	43	CB1	165	V_{SS}	72	V_{DD}	194	$\overline{RAS}$	103	SA2	225	RFU
13	DQ9	135	V_{SS}	44	V_{SS}	166	DM8	73	$\overline{WE}$	195	V_{DDQ}	104	NC(TEST)	226	V_{SS}
14	V_{SS}	136	DM1	45	$\overline{DQS8}$	167	NC	74	V_{DDQ}	196	$\overline{S0}$	105	V_{SS}	227	DM6
15	$\overline{DQS1}$	137	NC	46	DQS8	168	V_{SS}	75	$\overline{CAS}$	197	V_{DDQ}	106	$\overline{DQS6}$	228	NC
16	DQS1	138	VSS	47	V_{SS}	169	CB6	76	V_{DDQ}	198	ODT0	107	DQS6	229	V_{SS}
17	V_{SS}	139	RFU	48	CB2	170	CB7	77	NC, $\overline{S1}$	199	A13, NC	108	V_{SS}	230	DQ54
18	$\overline{RESET}$	140	RFU	49	CB3	171	V_{SS}	78	NC, ODT1	200	V_{DD}	109	DQ50	231	DQ55
19	NC	141	V_{SS}	50	V_{SS}	172	NC	79	V_{DDQ}	201	NC	110	DQ51	232	V_{SS}
20	V_{SS}	142	DQ14	51	NC	173	V_{DDQ}	80	NC	202	V_{SS}	111	V_{SS}	233	DQ60
21	DQ10	143	DQ15	52	V_{DDQ}	174	NC, CKE1	81	V_{SS}	203	DQ36	112	DQ56	234	DQ61
22	DQ11	144	V_{SS}	53	CKE0	175	V_{DD}	82	DQ32	204	DQ37	113	DQ57	235	V_{SS}
23	V_{SS}	145	DQ20	54	V_{DD}	176	A15, NC	83	DQ33	205	V_{SS}	114	V_{SS}	236	DM7
24	DQ16	146	DQ21	55	BA2	177	A14, NC	84	V_{SS}	206	DM4	115	$\overline{DQS7}$	237	NC
25	DQ17	147	V_{SS}	56	NC	178	V_{DDQ}	85	$\overline{DQS4}$	207	NC	116	DQS7	238	V_{SS}
26	V_{SS}	148	DM2	57	V_{DDQ}	179	A12	86	DQS4	208	V_{SS}	117	V_{SS}	239	DQ62
27	$\overline{DQS2}$	149	NC	58	A11	180	A9	87	V_{SS}	209	DQ38	118	DQ58	240	DQ63
28	DQS2	150	V_{SS}	59	A7	181	V_{DD}	88	DQ34	210	DQ39	119	DQ59	241	V_{SS}
29	V_{SS}	151	DQ22	60	V_{DD}	182	A8	89	DQ35	211	V_{SS}	120	V_{SS}	242	SDA
30	DQ18	152	DQ23	61	A5	183	A6	90	V_{SS}	212	DQ44	121	SA0	243	SCL
31	DQ19	153	V_{SS}	62	A4	184	V_{DDQ}	91	DQ40	213	DQ45	122	SA1	244	VDDSPD

NC = No Connect; NU = Not Useable, RFU = Reserved Future Use.
1. CK1,$\overline{CK1}$,CK2, $\overline{CK2}$ (pins 139,140,224,225) are for Unbuffered Mini-DIMM clock. These pins are RFU on registered Mini-DIMMs.
2. $\overline{RESET}$ (pin 18) is connected to both OE of the PLL and $\overline{Reset}$ of the register .
3. The TEST pin (pin 104) is reserved for bus analysis probes and is not connected on normal modules (Mini-DIMMs).

APPENDIX E - NEX-NVD2M667X8SRxR Silkscreen



Front Silk Screen



Back Silk Screen

APPENDIX F - Data Group / Data Byte / Strobe Cross-Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
RdADatHi	RdADatB7	DQS7	63,62,61,60,59,58,57,56
	RdADatB6	DQS6	55,54,53,52,51,50,49,48
	RdADatB5	DQS5	47,46,45,44,43,42,41,40
	RdADatB4	DQS4	39,38,37,36,35,34,33,32
RdADatLo	RdADatB3	DQS3	31,30,29,28,27,26,25,24
	RdADatB2	DQS2	23,22,21,20,19,18,17,16
	RdADatB1	DQS1	15,14,13,12,11,10,9,8
	RdADatB0	DQS0	7,6,5,4,3,2,1,0
WrADatHi	WrADatB7	DQS7	63,62,61,60,59,58,57,56
	WrADatB6	DQS6	55,54,53,52,51,50,49,48
	WrADatB5	DQS5	47,46,45,44,43,42,41,40
	WrADatB4	DQS4	39,38,37,36,35,34,33,32
WrADatLo	WrADatB3	DQS3	31,30,29,28,27,26,25,24
	WrADatB2	DQS2	23,22,21,20,19,18,17,16
	WrADatB1	DQS1	15,14,13,12,11,10,9,8
	WrBDatB0	DQS0	7,6,5,4,3,2,1,0
RdBDatHi	RdBDatB7	DQS7	63,62,61,60,59,58,57,56
	RdBDatB6	DQS6	55,54,53,52,51,50,49,48
	RdBDatB5	DQS5	47,46,45,44,43,42,41,40
	RdBDatB4	DQS4	39,38,37,36,35,34,33,32
RdBDatLo	RdBDatB3	DQS3	31,30,29,28,27,26,25,24
	RdBDatB2	DQS2	23,22,21,20,19,18,17,16
	RdBDatB1	DQS1	15,14,13,12,11,10,9,8
	RdBDatB0	DQS0	7,6,5,4,3,2,1,0
WrBDatHi	WrBDatB7	DQS7	63,62,61,60,59,58,57,56
	WrBDatB6	DQS6	55,54,53,52,51,50,49,48
	WrBDatB5	DQS5	47,46,45,44,43,42,41,40
	WrBDatB4	DQS4	39,38,37,36,35,34,33,32
WrBDatLo	WrBDatB3	DQS3	31,30,29,28,27,26,25,24
	WrBDatB2	DQS2	23,22,21,20,19,18,17,16
	WrBDatB1	DQS1	15,14,13,12,11,10,9,8
	WrBDatB0	DQS0	7,6,5,4,3,2,1,0

MDDR2-3A Groups/Bytes/Strobes Cross Reference

APPENDIX G - References

JEDEC Double Data Rate (DDR) SDRAM Specification
JESD-79-R2 – February 2002

Micron DDR2 SDRAM, SNOOP™-DIMM
October 2003

Tektronix TLA700 System User's Manual

Tektronix TLA700 Logic Analyzer User's Manual

NEXUS Low Profile Distributed probe manual

APPENDIX H - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: http://**www.nexustechnology.com**

Support Contact Information

Technical Support	**techsupport@nexustechnology.com**
General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Please do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.