



NEX-PC104/+ PC104 / PC104+ Bus Adapter Users Manual

Including these Software Support packages:

102PC104

68PC104

PC104PCI

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1.0 OVERVIEW

1.1 General Information

PC104 and PC104+ support is provided using the same adapter card. The 8 or 16-bit PC104 (ISA) signals are brought out on one side of the adapter to 0.1" stake pin headers. The PC104+ (PCI) signals are brought out to the opposite side in a similar fashion. The NEX-PC104 product includes software support for the standard PC104 8 and 16-bit bus. The NEX-PC104+ product includes the PC104 support for ISA and adds support for PC104+/PCI.

This manual is broken up into two sections. The first describes the PC104 interface (ISA). The second describes PC104+ (PCI). All references to ISA refer to the 8 and 16-bit PC104 bus. All references to PCI refer to the high speed bus added to PC104 in the PC104+ specification.

The NEX-PC104 / PC104+ adapter has been designed to provide quick and easy connections to interface a 68, 102- or 136-channel TLA600/700 acquisition module to the PC104/PC104+ connectors.

The software included with the PC104 product permits the acquisition of ISA bus cycles and will display the data in easy-to-read symbolic form rather than raw hexadecimal or binary data. The PC104+ product adds software for the PCI bus.

Please note that this manual uses some terms generically. For instance, references to the TLA600/700 apply to a TLA704, TLA711, TLA714 or TLA720 chassis with one or more 7*2/3/4 acquisition card.

Appendix E is a silk-screen print of the NEX-PC104/+ Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the PC104/+, ISA and PCI Bus specification and the Tektronix TLA600/700. Also, in the case of the TLA600/700, it is expected that the user is familiar with Windows O.S.

2.0 SOFTWARE INSTALLATION

Two 3½" diskettes have been included with the NEX-PC104 Bus Adapter. One (68PC104) is for use with a 68 channel acquisition card. The other (102PC104) is for the 102 or 136 channel acquisition card. The NEX-PC104 includes software support for the 8 and 16-bit ISA bus. The NEX-PC104+ product includes the two diskettes previously mentioned and PCI support (PC104PCI) for a 68 channel acquisition card.

2.1 TLA600/700

The PC104 / PC104+ support software is loaded in the same method as other Windows programs. Place the Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose 68PC104, 102PC104 or PC104PCI and click on **Okay**.

3.0 CONFIGURING the NEX-PC104/PC104+ BUS ADAPTER

3.1 General Information

There is a jumper area on the NEX-PC104 adapter board – JMPR1 pins 0 and 1. When using the NEX-PC104 adapter in 8-bit mode, shorting blocks must be placed across these two jumpers for proper data acquisition by the logic analyzer. When using the adapter in 16-bit mode, the shorting blocks must be removed. If they are left on when using the NEX-PC104 board in 16-bit mode, improper operation of the target system may result.

Jumper areas are provided for use with a 68-channel acquisition card. When using a 102-channel acquisition card, all of the IRQ, DRQ and DAK signals are acquired. When using a 68-channel card, the user must jumper select the desired IRQ, DRQ and DAK signals that are required.

Certain PC104+ (PCI) signals are slot specific. On standard PC104+ boards, a rotary switch must be set to the appropriate slot. In order to maximize the electrical characteristics of these signals for monitoring, the NEX-PC104 adapter uses jumper blocks instead. These must be set to the appropriate slot prior to acquisition for proper slot monitoring. Please refer to the Module Slot jumper configuration on the adapter board for proper jumper selection. For example the following jumpers must be installed for acquisition of Slot 2 signals: REQ1, GNT1 CLK1 and IDSEL1.

4.0 CONNECTING to the NEX-PC104 ADAPTER

4.1 General

Although longer than a standard PC104 / PC104+ module, the NEX-PC104 / PC104+ adapter is designed to plug directly into a PC104/+ system. The board length should be checked to verify that it will fit in the PC104/+ system.

4.2 TLA600/700

When using NEX-PC104 (ISA) support with a TLA600/700 containing a 7*3/4 acquisition module (102 or 136 channel card), the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. When using NEX-PC104 (ISA) support with a TLA600/700 containing a 7*2 acquisition module (68 channel acquisition card), the necessary acquisition data sections are A0-A3, D0, D1, C2 and C3. When using NEX-PC104+ (PCI) support with a TLA600/700 containing a 7*2/3/4 acquisition module (68, 102 or 136 channel acquisition card), the necessary acquisition data sections are A0-A3, D0, D1, C2 and C3. These grouped channels (8 podlets to a group) should be connected to the locations denoted on the silkscreen.

Connect the clock leads to their specified locations. Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for PC104 with a 102-channel or larger acquisition module. Table 2 shows the 68-channel PC104 support. Table 3 shows the wiring and channel grouping for PC104+ with a 68-channel acquisition module.

Group Name	Signal Name	PC104 Pin #	TLA600/700 input	Group Name	Signal Name	PC104 Pin #	TLA600/700 input		
Address (Hex)	LA23	C2	A2:7	Data (Hex)	SD15	C18	D1:7		
	LA22	C3	A2:6		SD14	C17	D1:6		
	LA21	C4	A2:5		SD13	C16	D1:5		
	LA20	C5	A2:4		SD12	C15	D1:4		
	SA19	A12	A2:3		SD11	C14	D1:3		
	SA18	A13	A2:2		SD10	C13	D1:2		
	SA17	A14	A2:1		SD9	C12	D1:1		
	SA16	A15	A2:0		SD8	C11	D1:0		
	SA15	A16	A1:7		SD7	A2	D0:7		
	SA14	A17	A1:6		SD6	A3	D0:6		
	SA13	A18	A1:5		SD5	A4	D0:5		
	SA12	A19	A1:4		SD4	A5	D0:4		
	SA11	A20	A1:3		SD3	A6	D0:3		
	SA10	A21	A1:2		SD2	A7	D0:2		
	SA9	A22	A1:1		SD1	A8	D0:1		
	SA8	A23	A1:0		SD0	A9	D0:0		
	SA7	A24	A0:7						
	SA6	A25	A0:6						
	Misc (Off)	RESET	B2		A3:0	CycType (Sym)	-IOW	B13	C2:3
		AEN	A11		C3:5		-IOR	B14	C2:2
BALE		B28	C3:2	-SMEMW	B11		C2:5		
SBHE		C1	C3:1	-SMEMR	B12		C2:4		
				-MEMW	C10		C2:1		
				-MEMR	C9	C2:0			
				BusCtrl (Sym)	T/C	B27	C3:0		
					-IOCHK	A1	C3:6		
					-REFRSH	B19	A3:1		
					-MASTER	D17	C3:7		
			-OWS		B8	C3:4			
DMA_Req (Off)	DRQ7	D15	D2:6		IORDY	A10	C3:3		
	DRQ6	D13	D2:5		-MEM16	D1	C2:7		
	DRQ5	D11	D2:4	Intrpts (Off)	-IO16	D2	C2:6		
	DRQ3	B16	D2:3		IRQ15	D6	C1:2		
	DRQ2	B6	D2:2		IRQ14	D7	C1:1		
	DRQ1	B18	D2:1		IRQ12	D5	C1:0		
DRQ0	D09	D2:0	IRQ11		D4	C0:7			
			IRQ10		D3	C0:6			
DMA_Ack (Off)	-DAK7	D14	D3:6	IRQ9	B4	C0:5			
	-DAK6	D12	D3:5	IRQ7	B21	C0:4			
	-DAK5	D10	D3:4	IRQ6	B22	C0:3			
	-DAK3	B15	D3:3	IRQ5	B23	C0:2			
	-DAK2	B26	D3:2	IRQ4	B24	C0:1			
	-DAK1	B17	D3:1	IRQ3	B25	C0:0			
MiscAddr	-DAK0	D8	D3:0	Unused (Off)	-----	---	C1:7		
	LA19	C6	A3:7		-----	---	C1:6		
	LA18	C7	A3:6		-----	---	C1:5		
	LA17	C8	A3:5		-----	---	C1:4		
Clock:0	CLK	B20	CLK0		-----	---	C1:3		
Clock:1			-----		-----	---	D3:7		
Clock:2			-----		-----	---	D2:7		
Clock:3	ISAWR=	*	CLK3						

Table 1- PC104/ISA TLA700 Wiring 102-channel support

* Derived signal

Group Name	Signal Name	PC104 Pin #	TLA600/700 input	Group Name	Signal Name	PC104 Pin #	TLA600/700 input	
Address (Hex)	LA23	C2	A2:7	Data (Hex)	SD15	C18	D1:7	
	LA22	C3	A2:6		SD14	C17	D1:6	
	LA21	C4	A2:5		SD13	C16	D1:5	
	LA20	C5	A2:4		SD12	C15	D1:4	
	SA19	A12	A2:3		SD11	C14	D1:3	
	SA18	A13	A2:2		SD10	C13	D1:2	
	SA17	A14	A2:1		SD9	C12	D1:1	
	SA16	A15	A2:0		SD8	C11	D1:0	
	SA15	A16	A1:7		SD7	A2	D0:7	
	SA14	A17	A1:6		SD6	A3	D0:6	
	SA13	A18	A1:5		SD5	A4	D0:5	
	SA12	A19	A1:4		SD4	A5	D0:4	
	SA11	A20	A1:3		SD3	A6	D0:3	
	SA10	A21	A1:2		SD2	A7	D0:2	
	SA9	A22	A1:1		SD1	A8	D0:1	
	SA8	A23	A1:0		SD0	A9	D0:0	
	SA7	A24	A0:7		CycType (Sym)	-IOW	B13	C2:3
	SA6	A25	A0:6			-IOR	B14	C2:2
	SA5	A26	A0:5			-SMEMW	B11	C2:5
	SA4	A27	A0:4			-SMEMR	B12	C2:4
SA3	A28	A0:3	-MEMW	C10		C2:1		
SA2	A29	A0:2	-MEMR	C9		C2:0		
Misc (Off)	RESET	B2	A3:0	BusCtrl (Sym)	T/C	B27	C3:0	
	AEN	A11	C3:5		-IOCHK	A1	C3:6	
	BALE	B28	C3:2		-REFRSH	B19	A3:1	
	SBHE	C1	C3:1		-MASTER	D17	C3:7	
					-OWS	B8	C3:4	
					IORDY	A10	C3:3	
MiscAddr	LA19	C6	A3:7		-MEM16	D1	C2:7	
	LA18	C7	A3:6		-IO16	D2	C2:6	
	LA17	C8	A3:5					
Clock:0	CLK	B20	CLK0	Select	IRQ_SEL	*1	CLK1	
Clock:1	IRQ_SEL	*1	CLK1		DRQ_SEL	*3	A3:4	
Clock:2			----		DAK_SEL	*4	A3:3	
Clock:3	ISAWR	*2	CLK3					

Table 2- PC104/ISA TLA600/700 Wiring 68-channel support

*1: IRQ select signal, *2: Derived signal, *3: DRQ select signal, *4: DAK select signal

Group Name	Signal Name	PC104+ Pin #	TLA600/700 input	Group Name	Signal Name	PC104+ Pin #	TLA600/700 input
Addr_Dat (Hex)	AD[31]	D22	+ A3:7	Control (Sym)	RST#	D28	+ C3:5
	AD[30]	B22	+ A3:6		FRAME#	A13	+ C2:0
	AD[29]	A21	+ A3:5		DEVSEL#	D12	+ C3:0
	AD[28]	C21	+ A3:4		STOP#	A11	+ C2:3
	AD[27]	D21	+ A3:3		IRDY#	C13	+ C2:1
	AD[26]	B20	+ A3:2		TRDY#	B12	+ C2:2
	AD[25]	C20	+ A3:1		C/BE#[3]	B19	+ C2:7
	AD[24]	A19	+ A3:0	C/BE#[2]	D14	+ C2:6	
	AD[23]	B17	+ A2:7	C/BE#[1]	B8	+ C2:5	
	AD[22]	C17	+ A2:6	C/BE#[0]	A4	+ C2:4	
	AD[21]	A16	+ A2:5	Intrpt (Off)	INTD#	B28	D0:3
	AD[20]	B16	+ A2:4		INTC#	D29	D0:2
	AD[19]	D16	+ A2:3		INTB#	C29	D0:1
	AD[18]	A15	+ A2:2		INTA#	B29	D0:0
	AD[17]	C15	+ A2:1	Misc (Off)	REQ#	*1	D0:5
	AD[16]	B14	+ A2:0		GNT#	*2	D0:6
	AD[15]	C8	+ A1:7		LOCK#	C11	C3:4
	AD[14]	A7	+ A1:6		IDSEL	*3	D0:4
	AD[13]	B7	+ A1:5		PERR#	B10	C3:3
	AD[12]	D7	+ A1:4		PAR	D9	C3:2
AD[11]	A6	+ A1:3	SERR#	A9	C3:1		
AD[10]	C6	+ A1:2	Ungrouped	SDONE	D10	C3:6	
AD[9]	B5	+ A1:1		SBO#	C9	D1:3	
AD[8]	C5	+ A1:0		M66EN	D6	D0:7	
AD[7]	B4	+ A0:7		Clock:0	unused	-----	
AD[6]	D4	+ A0:6	Clock:1	DEVSEL#	D12	+ CLK1	
AD[5]	A3	+ A0:5	Clock:2	unused	-----		
AD[4]	C3	+ A0:4	Clock:3	CLK	*4	+ CLK3	
AD[3]	D3	+ A0:3					
AD[2]	B2	+ A0:2					
AD[1]	C2	+ A0:1					
AD[0]	D1	+ A0:0					

Table 3- PC104+/PCI TLA600/700 Wiring

*1: REQ select signal, *2: GNT select signal, *3: IDSEL select signal, *4: CLK select signal, +: Required signals for clocking

5.0 CLOCK SELECTION

5.1 PC104: General Information

There are two clocking options available when using the NEX-PC104 support package. Each is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.2 PC104: Clocking Options - Explanation

Cycle Acquisition Only - This is the default clocking selection. In this mode every bus transaction is acquired. All Wait states are ignored. This clocking selection offers the best use of your acquisition memory by ignoring all Wait states, and also provides more easily understood data. For this acquisition mode to work properly, the PC104/ISA signals -MEMR, -MEMW, -IOR, -IOW, -SMEMR, -SMEMW, and CLK must be present.

Every CLK Edge - In this mode, data will be acquired on every edge of the PC104 / ISA CLK signal. This clocking mode shows *all* bus cycles, including Wait states. Since no clocking qualification is done only the CLK signal is required.

5.3 PC104+: General Information

There are three clocking options available when using the NEX-PC104+ support package. Each is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.4 PC104+: Clocking Options – Explanation

Bus Cycle Acquisition – This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as well all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable – In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge – In this mode, data will be acquired on every rising edge of PC104+/PCI CLK signal. The disassembly will filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows all bus cycles, including Wait and Idle states. Since no clocking qualification is done, only the CLK signal is required.

6.0 VIEWING DATA

6.1 PC104: Viewing State Data on the TLA600/700

After making an initial acquisition, the TLA600/700 will display the data in the Listing (State) format. Address and Data information is displayed in hexadecimal format; Cycle Type (CycType) and Bus Control (BusCtrl) data is displayed using symbols; Miscellaneous, DMA Request and Acknowledge, Interrupts, and MiscAddr data groups default to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-PC104, a symbol table (68PC104_Cyc for 68-Channel support and 102PC104_Cyc for 102-channel support, Table 4) has been provided to show the type of bus cycle that occurred on the PC104 bus. This symbol table quickly shows whether the acquisition was a memory or I/O operation, a read or a write, etc.

Sample	Address	Data	CycType	BusCtrl	Timestamp
11	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
12	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
13	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
14	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
15	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
16	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
17	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
18	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
19	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
20	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
21	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
22	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
23	000043	5454	IOW	8-BIT	316.572,375,500 ms
24	FFFC00	FFFF	MEMR	REFRESH	842.000 ns
25	0FE3B0	C1C1	SMEMR	8-BIT	555.000 ns
26	0FE3B1	EAEA	SMEMR	8-BIT	418.500 ns
27	0FE3B2	1010	SMEMR	8-BIT	419.500 ns
28	0FE3B3	E9E9	SMEMR	8-BIT	419.000 ns
29	0FE3B4	CACA	SMEMR	8-BIT	978.000 ns
30	0FE3B5	0202	SMEMR	8-BIT	419.000 ns
31	0FE3B6	6666	SMEMR	8-BIT	419.000 ns
32	0FE3B7	C1C1	SMEMR	8-BIT	419.500 ns
33	0FE3B8	E3E3	SMEMR	8-BIT	977.500 ns
34	0FE3B9	1010	SMEMR	8-BIT	419.000 ns
35	0FE3BA	2222	SMEMR	8-BIT	419.000 ns

Figure 1- PC104 State Display on TLA600/700

A second symbol table (68PC104_Bus for 68-channel support and 102PC104_Bus for 102-channel support, Table 5) shows whether the bus transaction was Refresh cycle, or an 8- or 16-bit operation. It is important to note that changing the group, channel, or wiring of the CycType or BusCtrl groups can result in incorrect symbol information being displayed.

Pattern	TLA700 Symbol
0xxxxx	IOW
x0xxxx	IOR
xx0xxx	SMEMW
xxx0xx	SMEMR
xxxx0x	MEMW
xxxxx0	MEMR

Table 4- 68PC104_Cyc/102PC104_Cyc Cycle Type Symbol Table

Signals, from left to right: -IOW, -IOR, -SMEMW, -SMEMR, -MEMW, -MEMR

Pattern	TLA700 Symbol
xx0xxxxx	REFRESH
xx1xxx0x	MEM16
xx1xxxx0	IO16
xx1xxx11	8-BIT

Table 5- 68PC104_Bus/102PC104_Bus Bus Control Symbol Table

Signals, from left to right: T/C, -IOCHK, -REFRSH, -MASTER, -OWS, IORDY, -MEM16, -IO16

6.2 PC104 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: PC104 and PC104-MagniVu. The first (PC104) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Timing format. The second selection, PC104-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

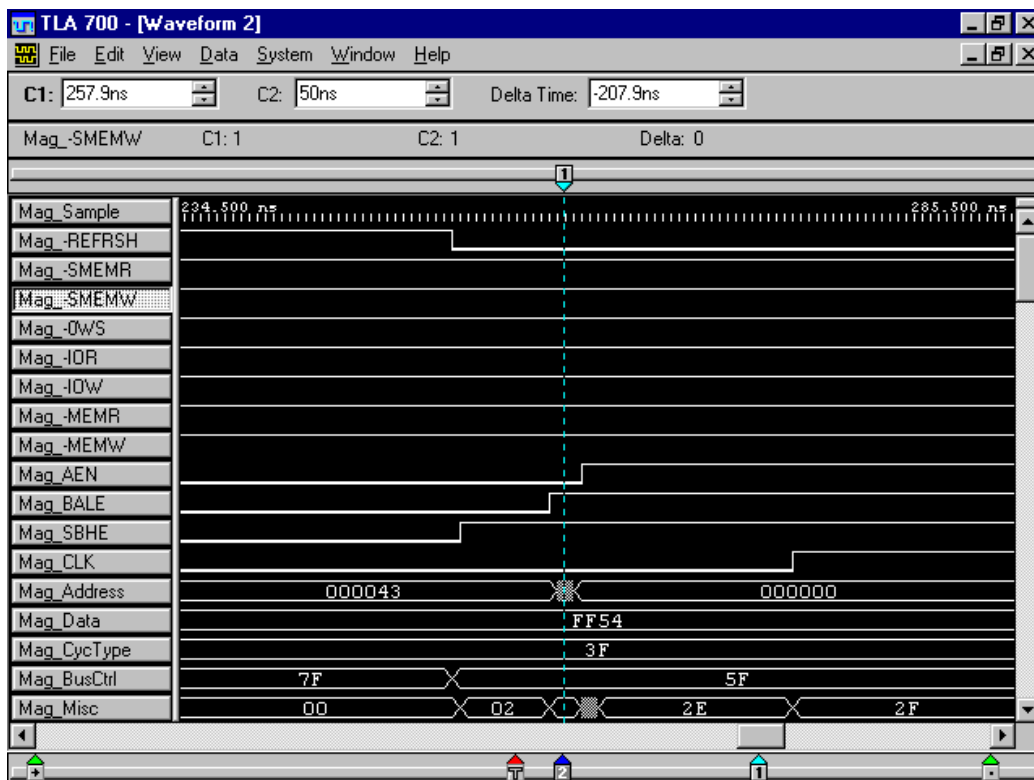


Figure 2- PC104 MagniVu Display on TLA600/700

6.3 PC104+ Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PC104PCI and PC104PCI-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PC104PCI-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

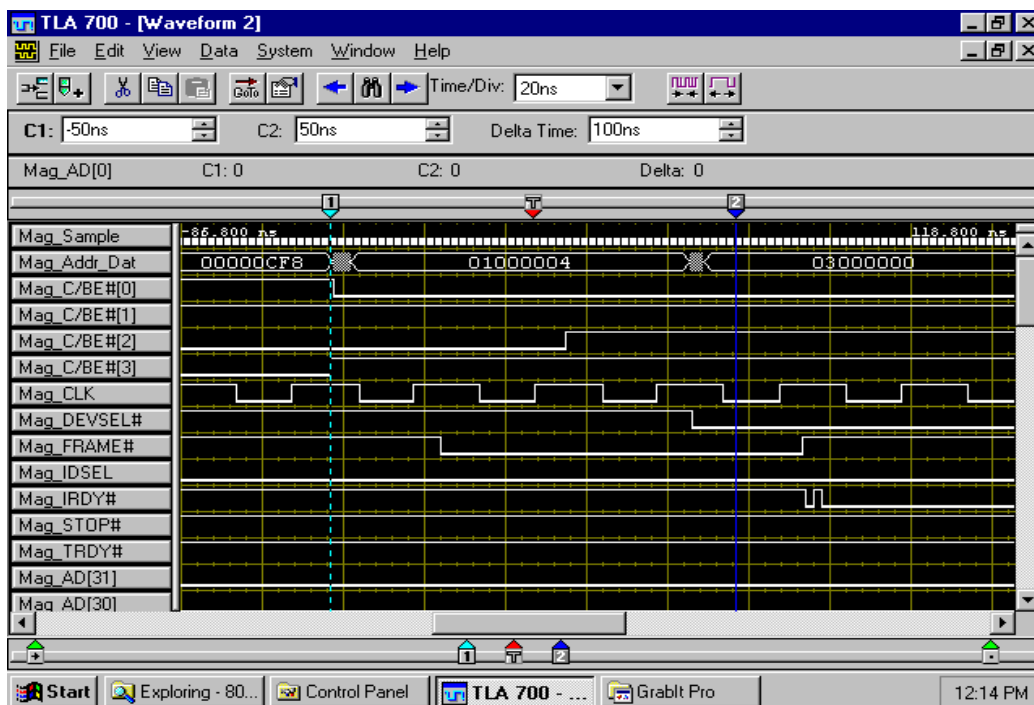


Figure 3- PC104PCI MagniVu Display on TLA700

Pattern	TLA700 Symbols	Meaning
0xxxxxxxxx	RESET	Reset
101110000	INTERRUPT ACK	Interrupt Acknowledge
101110001	SPECIAL CYCLE	Special Cycle
101110010	I/O READ ADDRESS	I/O Read
101110011	I/O WRITE ADDRESS	I/O Write
10111010x	RESERVED	Reserved
101110110	MEMORY READ ADDRESS	Memory Read
101110111	MEMORY WRITE ADDRESS	Memory Write
10111100x	RESERVED	Reserved
101111010	CONFIG READ ADDRESS	Configuration Read
101111011	CONFIG WRITE ADDRESS	Configuration Write
101111100	MEMORY READ MULTIPLE	Memory Read Multiple
101111101	DUAL ADDRESS	Dual Address Cycle
101111110	MEMORY READ LINE	Memory Read Line
101111111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
1x0x00110	DATA – BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA – BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA – BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA – BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA – BYTES 0 & 1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA – BYTES 2 & 3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA – BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo

Table 6- NEX-PC104+ Control Symbol Table

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#,
C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

7.0 USING the PC104+ DISASSEMBLY SOFTWARE

7.1 General

The NEX-PC104+ support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 4). All PC104+/PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest. The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the NEX-PC104+ software is its ability to intelligently acquire PC104+/PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers, the PC104+ software is able to acquire only the PC104+/PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PC104+/PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.4 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps in the TLA700 series, permits design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Using the TLA700

The TLA700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column – Adds a column to the display
- Add Mark – Adds a user mark to the display
- Cut – (may be grayed out) – Cuts the selection to the Clipboard
- Copy – (may be grayed out) – Copies the selection to the Clipboard
- Paste – (may be grayed out) – Inserts the contents of the Clipboard
- Go To – Moves the display to the item of interest
- Properties – Edits the current Listing Display properties
- Smaller Font – Decreases the displayed font size
- Larger Font – Increases the displayed font size
- Search Backward – Moves to a previous data match
- Define Search – Define data to be matched
- Search Forward – Moves to the next data match
- Mark Opcode – Permits placing an opcode mark (disabled in PC104+)

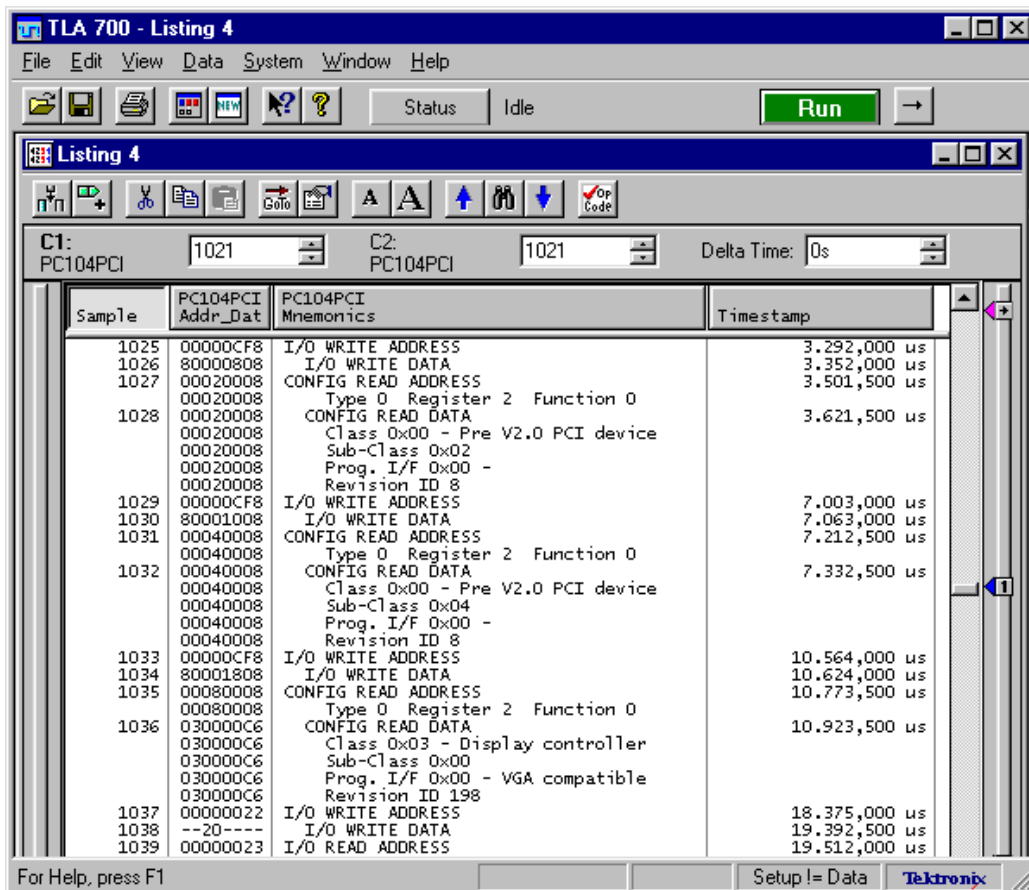


Figure 4- PC104+ Disassembly

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PC104+ disassembly information is displayed. As mentioned previously, it is possible to choose which PC104+/PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

APPENDIX A - Necessary Signals for Clocking

A.1 PC104/ISA

Because of the number of control signals defines in the PC104 specification, additional circuitry had to be provided to ensure proper clocking of data. A 74S30 8-input NAND gate is used to gate -IOW, -IOR, -SMEMW, -SMEMR, -MEMW, and -MEMR to provide a logic high output (ISAWR) whenever any one of these inputs goes low. This generated signal is what is used to acquire information when in the “Cycle Acquisition Only” mode.

When acquiring data in “Acquire Every CLK Edge” mode, the only signal necessary for clocking is CLK.

A.2 PC104+/PCI

To properly acquire PC104+/PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

APPENDIX B - Considerations

Loading

It must be noted that the NEX-PC104 Bus Adapter does not provide any buffering of the PC104/+ backplane signals. This was a conscious design decision that was made by balancing the tradeoffs of possible backplane loading versus signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-PC104/+ adapter, to see the exact timing relationships and signal waveforms from the backplane. It is also much easier to connect pattern generators to the backplane since buffer direction is not a concern. It is believed that the signal loading of the TLA600/700 acquisition cards is low enough so that PC104 signal degradation will not occur.

The NEX-PC104 Adapter Board was designed so that the run lengths for critical signals (and those with the highest activity levels, such as the address / data bus) are as short as possible. This should help greatly in retaining signal integrity.

APPENDIX C – PC104 Bus Pinout

Pin #	Side B	Side A
1	GND	-IOCHK
2	RESET	SD7
3	+5V	SD6
4	IRQ9	SD5
5	-5V	SD4
6	DRQ2	SD3
7	-12V	SD2
8	-OWS/ENDXFR*	SD1
9	+12V	SD0
10	GND/KEY	IORDY
11	-SMEMW	AEN
12	-SMEMR	SA19
13	-IOW	SA18
14	-IOR	SA17
15	-DAK3	SA16
16	DRQ3	SA15
17	-DAK1	SA14
18	DRQ1	SA13
19	REFRSH*	SA12
20	CLK	SA11
21	IRQ7	SA10
22	IRQ6	SA9
23	IRQ5	SA8
24	IRQ4	SA7
25	IRQ3	SA6
26	-DAK2	SA5
27	T/C	SA4
28	BALE	SA3
29	+5V	SA2
30	OSC	SA1
31	GND	SA0
32	GND	GND

J1 / P1 Connector

Pin #	Side D - Solder Side	Side C - Component Side
0	GND	GND
1	MEMCS16*	SBHE*
2	-IO16	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15	LA19
7	IRQ14	LA18
8	-DAK0	LA17
9	DRQ0	-MEMR
10	-DAK5	-MEMW
11	DRQ5	SD8
12	-DAK6	SD9
13	DRQ6	SD10
14	-DAK7	SD11
15	DRQ7	SD12
16	+5V	SD13
17	MASTER*	SD14
18	GND	SD15
19	GND	GND/KEY

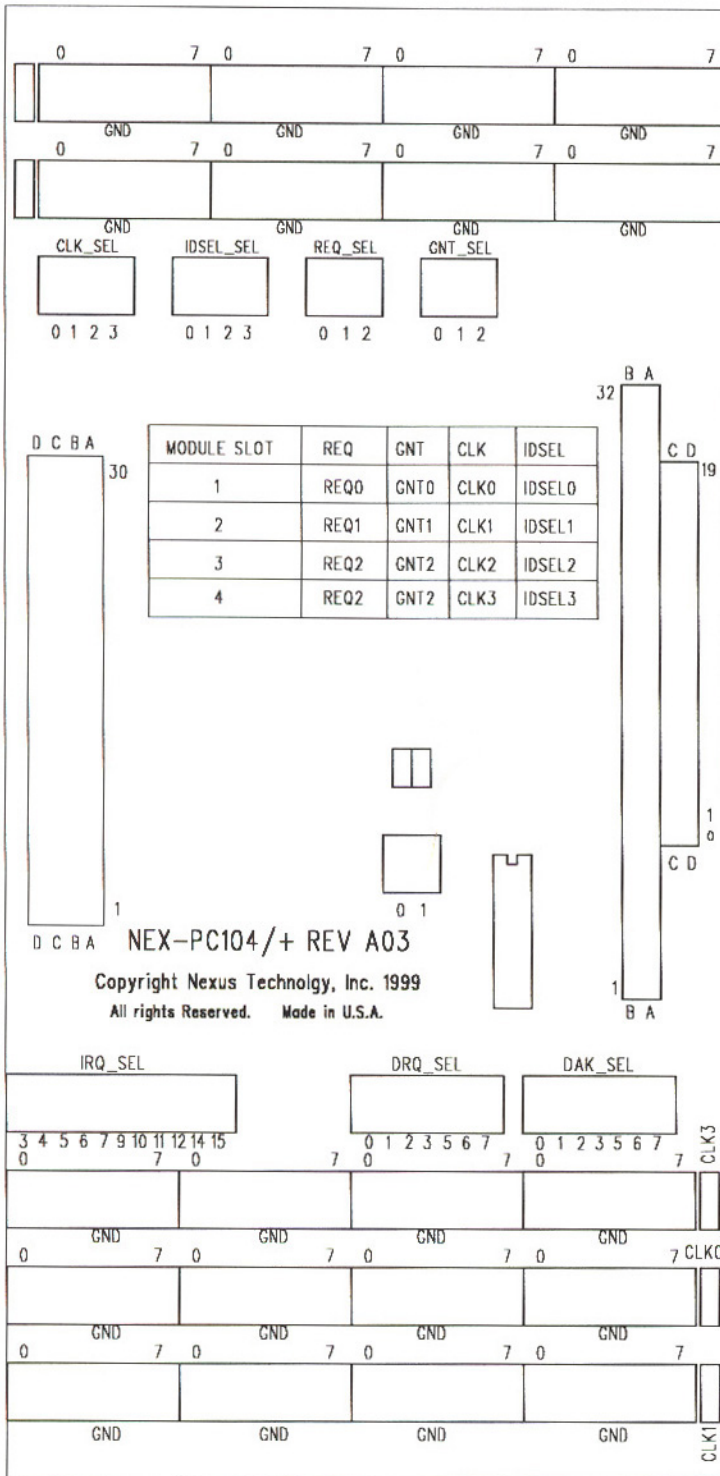
J2 / P2 Connector

APPENDIX D – PC104+ Bus Pinout

Pin #	A	B	C	D
1	GND/5.0V KEY	RESERVED	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BEO*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR	GND	SBO*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD20	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	RESERVED	RESERVED	GND/3.3V KEY

J3 / P3 Connector

APPENDIX E - NEX-PC104 Silk Screen



APPENDIX F - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Web site: <http://www.nexustechnology.com>

Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX G - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Logic Analyzer User's Manual

“AT Bus Design” by Edward Solari
Published by Annabooks, San Diego, CA

“Intel ISA Bus Specification and Application Notes”
Rev. 3.00, January 30, 1990

PC/104-Plus Specification Version 1.1

“Personal Computer Bus Standard”
IEEE document P996
Draft D2.02, 13 July 1990

Tektronix TLA600/700 Module User's Manual

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800-433-5177 (U.S.)
503-797-4207 (International)
503-234-6762 (Fax)

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