



NEX-PCI

PCI Bus Adapter Users Manual

Including these Software Support packages:
PCI64 PCI32SW_68 PCI32SW_102

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1.0 OVERVIEW

1.1 General Information

The NEX-PCI adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA600/700, a 92A96, or a 92C96 acquisition module to a 32-bit or 64-bit PCI backplane. (The PCI designation refers to the Peripheral Component Interconnect Local Bus specification.) In addition, the method of connection permits the use of other acquisition cards, pattern generation cards or other measurement devices such as oscilloscopes.

Two software support packages have been provided. The first, NEX-PCI32SW, permits the acquisition of all 32-bit PCI bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form. The second support package, NEX-PCI64, offers the same option for storing or not storing Wait and Idle cycles, but does not support transaction disassembly and instead displays bus data in symbolic form.

Please note that this manual uses some terms generically. For instance, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA700 apply to TLA600 or a TLA700 with a TLA704, TLA711, TLA714, TLA715, TLA720 or TLA721 chassis with one or more 7*3/4 acquisition cards.

Appendix E is a silk-screen print of the NEX-PCI Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the PCI Local Bus specification and the Tektronix TLA600/700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA600/700, it is expected that the user is familiar with M.S. Windows.

For information on using a Prism 32GPX/GPD module with this support, or if 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix F for contact information.

2.0 SOFTWARE INSTALLATION

Two 3½” diskettes have been included with the NEX-PCI Bus Adapter. They are for use with the TLA600/700 series. One is for 32-bit support (NEX-PCI32SW) and the other for 64-bit support (NEX-PCI64). Diskettes for the DAS9200 or TLA500 are available upon request. See Appendix F for contact information.

2.1 TLA600/700

The PCI support software is loaded in the same method as other Windows programs. Place the NEX-PCI32SW or NEX-PCI64 Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install, Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose either PCI32 or PCI64 and click on **Okay**. Note that for either support the Logic Analyzer card must be at least 102-channels in width.

2.2 DAS9200

The included diskettes should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing either "PCI32 Support" or "PCI64 Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

3.0 CONFIGURING the NEX-PCI BUS ADAPTER

3.1 General Information

Not all PCI signals are monitored by either the DAS9200 or the TLA600/700. Refer to Table 1 for a list of acquired signals using 32-bit support. Table 2 lists the signals acquired using 64-bit support. For information on physically modifying the NEX-PCI adapter to monitor signals not provided with the standard implementation, refer to Appendix C.

3.2 Configuring for Slot Specific Signals

A jumper block (JP1) has been provided to enable monitoring the slot specific signals REQ# and GNT#. To acquire these signals, connect the included flying leads to the appropriate signal pin, attach a grabber tip to the other end of the wire, then connect the grabber tip to a point on the backplane or target circuitry to acquire these signals. It may be necessary to refer to schematics of the target board to determine where the signals can be probed. For reference, the signals may be acquired on the PCI Bus at the following pins:

GNT#	A17
REQ#	B18

4.0 CONNECTING to the NEX-PCI ADAPTER

4.1 General

Although taller than a standard PCI module, the NEX-PCI adapter is designed to plug directly into any full-size PCI backplane slot. The board length and connector spacing conforms to PCI Revision 2.1 specifications.

4.2 TLA600/700

When using 32-bit support with a TLA600/700 containing a 7*3/4 acquisition module, the necessary acquisition data sections are A0-A3 and C0-C3. For 64-bit support data sections A0-A3, D0-D3, and C0-C3 are required. These grouped channels (8 podlets to a group) should be connected to the locations denoted for the A96. Follow the silk-screened information on the board that shows the proper relationship between the signal and reference inputs. When properly connected, the sides of the podlets that have writing on them should be visible.

Connect the four clock leads to their specified locations at J8 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the TLA600/700 when used with the NEX-PCI adapter in 32-bit mode. Table 2 shows the wiring and Channel Grouping for 64-bit support.

4.3 92A96

When using a 92A96 or 92C96, connect the grouped pods to their appropriate locations by following the silk-screen information printed on the adapter board. The 92A/C96 pods are labeled A0-A3, D0-D3, and C0-C3. Each pod has its proper location denoted on the silk-screen of the adapter board. When attaching the pods, follow the silk-screen information on the board showing the ground and signal pin locations. When properly connected, the colored sides of the podlets should be visible.

Connect the four clock leads (one per A96 cable) to their specified locations at J8 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the 92A96 when used with the NEX-PCI adapter in 32-bit mode. Table 2 shows the wiring and Channel Grouping for 64-bit support.

Group Name	Signal Name	PCI Pin #	TLA / 92A96 input	Group Name	Signal Name	PCI Pin #	TLA / 92A96 input	
Addr_Dat (Hex)	AD[31]	B20	A3:7	Control (Sym)	RST#	A15	C3:5	
	AD[30]	A20	A3:6		FRAME#	A34	C2:0	
	AD[29]	B21	A3:5		DEVSEL#	B37	C3:0	
	AD[28]	A22	A3:4		STOP#	A38	C2:3	
	AD[27]	B23	A3:3		IRDY#	B35	C2:1	
	AD[26]	A23	A3:2		TRDY#	A36	C2:2	
	AD[25]	B24	A3:1		C/BE#[3]	B26	C2:7	
	AD[24]	A25	A3:0		C/BE#[2]	B33	C2:6	
	AD[23]	B27	A2:7		C/BE#[1]	B44	C2:5	
	AD[22]	A28	A2:6		C/BE#[0]	A52	C2:4	
	AD[21]	B29	A2:5	Intrpt (Off)	INTD#	B08	C0:3	
	AD[20]	A29	A2:4		INTC#	A07	C0:2	
	AD[19]	B30	A2:3		INTB#	B07	C0:1	
	AD[18]	A31	A2:2		INTA#	A06	C0:0	
	AD[17]	B32	A2:1	Misc (Off)	REQ#	-----	C0:5	
	AD[16]	A32	A2:0		GNT#	-----	C0:6	
	AD[15]	A44	A1:7		LOCK#	B39	C3:4	
	AD[14]	B45	A1:6		IDSEL	A26	C0:4	
	AD[13]	A46	A1:5		PERR#	B40	C3:3	
	AD[12]	B47	A1:4		PAR	A43	C3:2	
	AD[11]	A47	A1:3		SERR#	B42	C3:1	
	AD[10]	B48	A1:2	CLK	B16	C3:6		
	AD[9]	A49	A1:1	Aux_0	Aux_0:[7-0]	-----	D2	
	AD[8]	B52	A1:0	Aux_1	Aux_1:[7-0]	-----	D3	
	AD[7]	B53	A0:7	Clock:0	CLK=	B16		
	AD[6]	A54	A0:6		Clock:1	unused	-----	
	AD[5]	B55	A0:5		Clock:2	DEVSEL#=	B37	
	AD[4]	A55	A0:4		Clock:3	unused	-----	
	AD[3]	B56	A0:3					
	AD[2]	A57	A0:2					
	AD[1]	B58	A0:1					
	AD[0]	A58	A0:0					

Table 1- 32-bit TLA600/700/92A96 Wiring

Group Name	Signal Name	PCI Pin #	TLA / 92A96 Input	Group Name	Signal Name	PCI Pin #	TLA / 92A96 input
AD-Hi (Hex)	AD[63]	B68	D3:7	AD-Lo (Hex)	AD[31]	B20	A3:7
	AD[62]	A68	D3:6		AD[30]	A20	A3:6
	AD[61]	B69	D3:5		AD[29]	B21	A3:5
	AD[60]	A70	D3:4		AD[28]	A22	A3:4
	AD[59]	B71	D3:3		AD[27]	B23	A3:3
	AD[58]	A71	D3:2		AD[26]	A23	A3:2
	AD[57]	B72	D3:1		AD[25]	B24	A3:1
	AD[56]	A73	D3:0		AD[24]	A25	A3:0
	AD[55]	B74	D2:7		AD[23]	B27	A2:7
	AD[54]	A74	D2:6		AD[22]	A28	A2:6
	AD[53]	B75	D2:5		AD[21]	B29	A2:5
	AD[52]	A76	D2:4		AD[20]	A29	A2:4
	AD[51]	B77	D2:3		AD[19]	B30	A2:3
	AD[50]	A77	D2:2		AD[18]	A31	A2:2
	AD[49]	B78	D2:1		AD[17]	B32	A2:1
	AD[48]	A79	D2:0		AD[16]	A32	A2:0
	AD[47]	B80	D1:7		AD[15]	A44	A1:7
	AD[46]	A80	D1:6		AD[14]	B45	A1:6
	AD[45]	B81	D1:5		AD[13]	A46	A1:5
	AD[44]	A82	D1:4		AD[12]	B47	A1:4
	AD[43]	B83	D1:3		AD[11]	A47	A1:3
	AD[42]	A83	D1:2		AD[10]	B48	A1:2
	AD[41]	B84	D1:1		AD[9]	A49	A1:1
	AD[40]	A85	D1:0		AD[8]	B52	A1:0
	AD[39]	B86	D0:7		AD[7]	B53	A0:7
	AD[38]	A86	D0:6		AD[6]	A54	A0:6
	AD[37]	B87	D0:5		AD[5]	B55	A0:5
	AD[36]	A88	D0:4		AD[4]	A55	A0:4
	AD[35]	B89	D0:3		AD[3]	B56	A0:3
	AD[34]	A89	D0:2		AD[2]	A57	A0:2
	AD[33]	B90	D0:1		AD[1]	B58	A0:1
	AD[32]	A91	D0:0		AD[0]	A58	A0:0
Cmd/Size (Sym)	DEVSEL#	B37	C3:0	Control (Sym)	RST#	A15	C3:5
	IRDY#	B35	C2:1		GNT#	A17	C0:6
	TRDY#	A36	C2:2		STOP#	A38	C2:3
	ACK64#	B60	C1:6		LOCK#	B39	C3:4
	REQ64#	A60	C1:5	FRAME#	A34	C2:0	
	C/BE#[7]	A64	C1:3	IDSEL	A26	C0:4	
	C/BE#[6]	A65	C1:2	Intrpt (Off)	INTD#	B08	C0:3
	C/BE#[5]	B65	C1:1		INTC#	A07	C0:2
	C/BE#[4]	B66	C1:0		INTB#	B07	C0:1
	C/BE#[3]	B26	C2:7	INTA#	A06	C0:0	
C/BE#[2]	B33	C2:6	Misc (Off)	REQ#	-----	C0:5	
C/BE#[1]	B44	C2:5		PERR#	B40	C3:3	
C/BE#[0]	A52	C2:4		PAR	A43	C3:2	
				SERR#	B42	C3:1	
Clock:0	CLK=	B16		CLK	B16	C3:6	
Clock:1	unused	-----					
Clock:2	DEVSEL#=	B37					
Clock:3	unused	-----					

Table 2- 64-bit TLA600/700/92A96 Wiring

5.0 CLOCK SELECTION

5.1 General Information

There are three clocking options available when using the NEX-PCI32SW support package, and two options available in the NEX-PCI64 support. Each is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

When using a DAS9200 or TLA500, the clocking selection is made in the Clock menu.

5.2 Clocking Options - Explanation

Bus Cycle Acquisition - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable (32-bit support only) - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge - In this mode, data will be acquired on every rising edge of the PCI CLK signal. When using 32-bit support the software will filter and display these cycles accordingly, although incorrect decoding may occur occasionally because of the numerous duplicated cycles. In 64-bit mode the data will be displayed symbolically. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

6.0 VIEWING DATA

6.1 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PCI32 (or PCI64), and PCI32-MagniVu (or PCI64-MagniVu). The first (PCI32 or PCI64) will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PCI32-MagniVu or PCI64-MagniVu, will show all of the channels in 2GHz/8GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

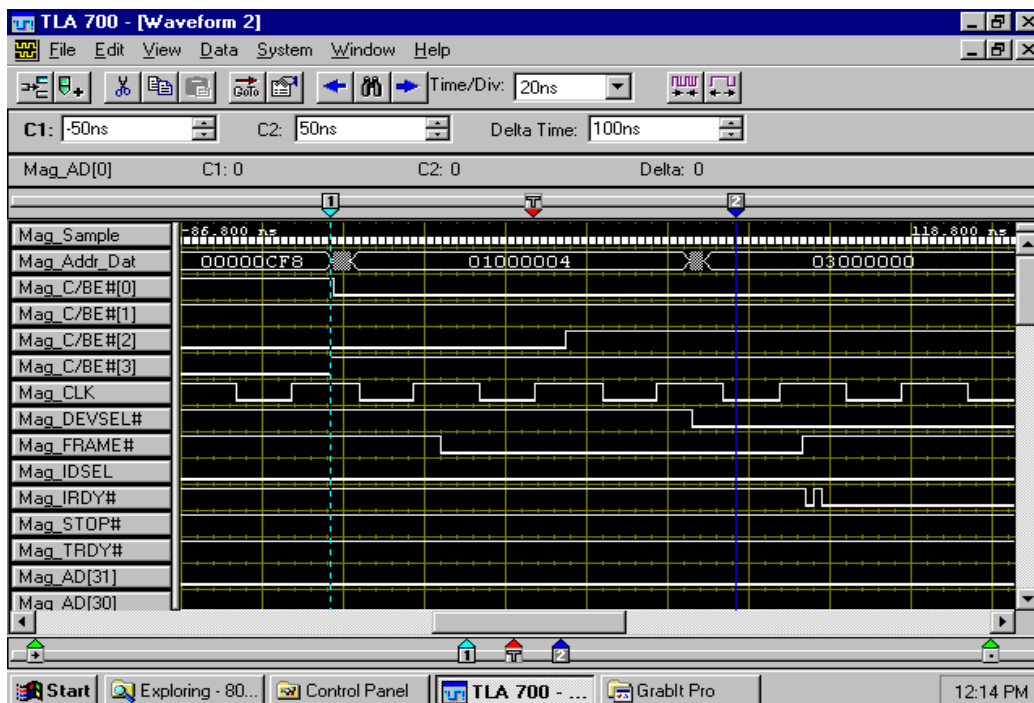


Figure 1- PCI32 MagniVu Display on TLA600/700

6.2 Viewing State Data on the DAS9200/TLA500

After an acquisition is made the DAS9200 Logic Analyzer will display the data in State Display mode (as a default only). Address / Data information is displayed in hexadecimal format; Control data is displayed using symbols; Interrupt, Miscellaneous, and both Auxiliary data groups default to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-PCI32SW, a symbol table (PCI32_Ctrl, Table 3) has been provided to show the type of transaction that occurred on the PCI bus. This symbol table quickly shows whether the acquisition was a memory or I/O operation, a read or a write, etc.

When using the NEX-PCI64 support, two symbol tables are available to help decode the bus transactions. The first, PCI64_Ctrl (Table 4), shows the state of some of the bus control lines. The second symbol table, PCI64_Cmd (Table 5), shows the type of transaction that occurred.

It is important to note that changing the group, channel, or wiring of the Cmd/Size or Control groups can result in incorrect symbol information being displayed.

6.3 Viewing Timing Data on the DAS9200/TLA500

It may be useful to display acquired information using the Timing Diagram display of the DAS9200. (Note that, unlike some other logic analyzers, with the DAS9200 there is no need to re-acquire PCI data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the DAS9200 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

Pattern	TLA600/700 / 92A96 Symbol	Meaning
0xxxxxxxxx	RESET	Reset
1011110000	INTERRUPT ACK	Interrupt Acknowledge
1011110001	SPECIAL CYCLE	Special Cycle
1011110010	I/O READ ADDRESS	I/O Read
1011110011	I/O WRITE ADDRESS	I/O Write
101111010x	RESERVED	Reserved
1011110110	MEMORY READ ADDRESS	Memory Read
1011110111	MEMORY WRITE ADDRESS	Memory Write
101111100x	RESERVED	Reserved
1011111010	CONFIG READ ADDRESS	Configuration Read
1011111011	CONFIG WRITE ADDRESS	Configuration Write
1011111100	MEMORY READ MULTIPLE	Memory Read Multiple
1011111101	DUAL ADDRESS	Dual Address Cycle
1011111110	MEMORY READ LINE	Memory Read Line
1011111111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
1x0x001110	DATA - BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA - BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA - BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA - BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA - BYTES 0 & 1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA - BYTES 2 & 3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA - BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo

Table 3- PCI32_Ctrl Control Symbol Table

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

Pattern	TLA600/700 / 92A96 Symbol	32GPX Symbol	Meaning
0xxxx0	RESET	RESET	Reset
1x0xx0	STOP	STOP	Stop current transaction
1x10x0	LOCK	LOCK	LOCK# asserted
1xxx00	FRAME	FRAME	Beginning/duration of access
1xxx1	IDEV SEL	IDEVSEL	Initialization Device Select

Table 4- PCI64_Ctrl Control Symbol Table

Signals, from left to right: RST#, GNT#, STOP#, LOCK#, FRAME#, IDSEL

Pattern	TLA600/700 / 92A96 Symbol	Meaning
111xxxxx0000	INTERRUPT ACK	Interrupt Acknowledge
111xxxxx0001	SPECIAL CYCLE	Special Cycle
111xxxxx0010	I/O READ	I/O Read
111xxxxx0011	I/O WRITE	I/O Write
111xxxxx010x	RESERVED	Reserved
111xxxxx0110	MEMORY READ	Memory Read
111xxxxx0111	MEMORY WRITE	Memory Write
111xxxxx100x	RESERVED	Reserved
111xxxxx1010	CONFIG READ	Configuration Read
111xxxxx1011	CONFIG WRITE	Configuration Write
111xxxxx1100	MEM READ MULT	Memory Read Multiple
111xxxxx1101	DUAL ADDR	Dual Address Cycle
111xxxxx1110	MEM READ LINE	Memory Read Line
111xxxxx1111	MEM WRT & INV	Memory Write & Invalidate
x00111111110	BYTE 0	Byte 0 valid (D0-7)
x00111111101	BYTE 1	Byte 1 valid (D8-15)
x00111111011	BYTE 2	Byte 2 valid (D16-23)
x00111110111	BYTE 3	Byte 3 valid (D24-31)
x00111110111	BYTE 4	Byte 4 valid (D32-39)
x00111101111	BYTE 5	Byte 5 valid (D40-47)
x00111011111	BYTE 6	Byte 6 valid (D48-55)
x00110111111	BYTE 7	Byte 7 valid (D56-63)
x00111111100	BYTES 0,1	Bytes 0 & 1 valid (D0-15)
x00111110011	BYTES 2,3	Bytes 2 & 3 valid (D16-31)
x00111100111	BYTES 4,5	Bytes 4 & 5 valid (D32-47)
x00110011111	BYTES 6,7	Bytes 6 & 7 valid (D48-63)
x00111110000	BYTES 0-3	Bytes 0-3 valid (D0-31)
x00110000111	BYTES 4-7	Bytes 4-7 valid (D32-63)
x00000000000	BYTES 0-7	Bytes 0-7 valid (D0-63)

Table 5- PCI64_Cmd Command/Size Symbol Table

Signals, from left to right: DEVSEL#, IRDY#, TRDY#, ACK64#, REQ64#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

7.0 USING the DISASSEMBLY SOFTWARE (NEX-PCI32SW)

7.1 General

The NEX-PCI32SW support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the NEX-PCI32SW software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the PCI32 software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.3 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 125ps/500ps in the TLA600/700 series, and to 10ns in the DAS9200 / TLA500, permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Using the TLA600/700

The TLA600/700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window

Sample	PCI32 Addr_Dat	PCI32 Mnemonics	Timestamp
812	01000008	CONFIG READ ADDRESS	2.526,500 us
	01000008	Type 0 Register 2 Function 0	
813	03000043	CONFIG READ DATA	150.500 ns
	03000043	Class 0x03 - Display controller	
	03000043	Sub-Class 0x00	
	03000043	Prog. I/F 0x00 - VGA compatible	
	03000043	Revision ID 67	
814	000C0000	MEMORY READ ADDRESS	23.317,000 us
815	----FFFF	MEMORY READ DATA	2.074,500 us
816	00000CF8	I/O WRITE ADDRESS	14.943,329,000 ns
817	80006804	I/O WRITE DATA	90.500 ns
818	01000004	CONFIG READ ADDRESS	1.955,000 us
	01000004	Type 0 Register 1 Function 0	
819	-----00	CONFIG READ DATA	150.500 ns
	-----00	Wait Cycle disabled	
	-----00	Parity Errors disabled	
	-----00	VGA Palette Snoop disabled	
	-----00	Mem Write & Inv. disabled	
	-----00	Special Cycle Recog. disabled	
	-----00	Master disabled	
	-----00	Memory Access disabled	
	-----00	I/O Access disabled	
820	00000CF8	I/O WRITE ADDRESS	13.510,500 us
821	80006804	I/O WRITE DATA	90.000 ns

Figure 2- PCI32 Disassembly

Sample	PCI32 Addr_Dat	PCI32 Mnemonics	Timestamp
	03000043	Revision ID 67	
818	01000004	CONFIG READ ADDRESS	14.970,766,000 ns
	01000004	Type 0 Register 1 Function 0	
819	-----00	CONFIG READ DATA	150.500 ns
	-----00	Wait Cycle disabled	
	-----00	Parity Errors disabled	
	-----00	VGA Palette Snoop disabled	
	-----00	Mem Write & Inv. disabled	
	-----00	Special Cycle Recog. disabled	
	-----00	Master disabled	
	-----00	Memory Access disabled	
	-----00	I/O Access disabled	
822	01000004	CONFIG WRITE ADDRESS	15.616,500 us
	01000004	Type 0 Register 1 Function 0	
823	-----02	CONFIG WRITE DATA	150.500 ns
	-----02	Wait Cycle disabled	
	-----02	Parity Errors disabled	
	-----02	VGA Palette Snoop disabled	
	-----02	Mem Write & Inv. disabled	
	-----02	Special Cycle Recog. disabled	
	-----02	Master disabled	
	-----02	Memory Access enabled	
	-----02	I/O Access disabled	
826	01000008	CONFIG READ ADDRESS	63.637,500 us

Figure 3- PCI32 Disassembly with suppressed Memory and I/O Cycles

contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark (disabled in PCI32SW)

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PCI32 disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

7.3 Disassembly Using the DAS9200 / TLA500

To view PCI32 data in Disassembly form, simply click on the DISASM button in the lower part of the DAS/TLA display, or select Disasm in the Display column of the Main Menu. All PCI transactions will be displayed and disassembled, and the Timestamp between each acquisition is displayed (Relative mode). To change the Timestamp format, press (or click) **F5** (Display Format) and open the Timestamp select field. The options available are: Relative (time from the previous sample), Delta (time from a user definable Delta mark), Absolute (time from when the acquisition card was started), and Off. Making a choice, closing the field, then pressing (or clicking) **F8** to Exit and Save will modify the Disassembly display appropriately.

To filter the displayed data, again move to the Display Format screen (press or click **F5**). The Hardware Display Mode (default) will display all PCI cycles by default.

By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Display Mode select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Display Mode select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Relative form) will be updated to show the time between displayed cycles.

APPENDIX A - Necessary Signals for Clocking

To properly acquire PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

APPENDIX B - Considerations

B.1 PCI Loading

It must be noted that the NEX-PCI Bus Adapter does not provide any buffering of the PCI backplane signals. This was a conscious design decision that was made by balancing the tradeoffs of possible backplane loading versus signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-PCI adapter, to see the exact timing relationships and signal waveforms from the backplane. It is also much easier to connect pattern generators to the backplane since buffer direction is not a concern. It is believed that the signal loading of the TLA600/700 or 92A96 acquisition cards is low enough so that PCI signal degradation will not occur.

The NEX-PCI Adapter Board was designed so that the run lengths for critical signals (and those with the highest activity levels, such as the address / data bus) are as short as possible. This should help greatly in retaining signal integrity

B.2 "Patch" Areas

If signal loading or reflection does become a concern, the capability exists to add series resistors to any PCI signal. Patch areas have been provided next to each TLA600/700/A96 connector, consisting of two rows of plated through holes. These areas (outlined on the silk-screen and labeled as Nxx) are suitable for individual resistors or resistor networks. To add a series resistor, simply cut the trace of the desired signal on the component side of the board, and solder the resistor between the two feed-throughs.

B.3 Pattern Generation

Because there is no buffer circuitry on the NEX-PCI Adapter, it is well suited for use with the 92S16 and 92S32 Pattern Generator modules available for the DAS9200. By connecting pattern generator probes to the A96 signal connectors on the Adapter, desired bus activity can be simulated. This can be particularly effective when trying to debug interrupt or DMA conflicts.

It should be noted that, because of the pin spacing of the A96 connectors, it is not recommended that the Tektronix P6464 or P6465 pattern generator probes be used without providing adequate cooling for their podlets. These probes use active podlets that can get very warm in use. A better choice would be the P6463 pods which are passive and do not have such cooling requirements.

APPENDIX C - Modifying the NEX-PCI Adapter

As previously mentioned, not all PCI signals are acquired by a 92A96 or TLA600/700. Assumptions have been made as to what signals are of interest, but these assumptions may not be appropriate for every instance. For these occasions, the NEX-PCI adapter may be easily modified to monitor any desired signals.

To monitor additional signals, the method is fairly simple. All PCI signals have been brought out to feed-throughs on the board, and there are two unused TLA/A96 connectors. These connectors have a patch area beneath them (towards the edge connector) to provide easy solder points. Use wire wrap wire to connect the PCI signals to these connectors.

APPENDIX D - PCI Local Bus Pinout

Pin #	Side B - Component Side	Side A - Solder Side	Comments
1	-12V	TRST#	32-bit start
2	TCK	+12V	
3	Ground	TMS	
4	TDO	TDI	
5	+5V	+5V	
6	+5V	INTA#	
7	INTB#	INTC#	
8	INTD#	+5V	
9	PRSNT1#	Reserved	
10	Reserved	+V I/O	
11	PRSNT2#	Reserved	
12	KEYWAY	KEYWAY	3.3V key
13	KEYWAY	KEYWAY	3.3V key
14	Reserved	Reserved	
15	Ground	RST#	
16	CLK	+V I/O	
17	Ground	GNT#	
18	REQ#	Ground	
19	+V I/O	Reserved	
20	AD[31]	AD[30]	
21	AD[29]	+3.3V	
22	Ground	AD[28]	
23	AD[27]	AD[26]	
24	AD[25]	Ground	
25	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	
28	Ground	AD[22]	
29	AD[21]	AD[20]	
30	AD[19]	Ground	
31	+3.3V	AD[18]	
32	AD[17]	AD[16]	
33	C/BE[2]#	+3.3V	
34	Ground	FRAME#	
35	IRDY#	Ground	
36	+3.3V	TRDY#	
37	DEVSEL#	Ground	
38	Ground	STOP#	
39	LOCK#	+3.3V	
40	PERR#	SDONE	
41	+3.3V	SBO#	
42	SERR#	GROUND	
43	+3.3V	PAR	
44	C/BE[1]#	AD[15]	
45	AD[14]	+3.3V	
46	Ground	AD[13]	
47	AD[12]	AD[11]	

Information given here is for the 64-bit Universal Board definitions:

Pin #	Side B - Component Side	Side A - Solder Side	Comments
48	AD[10]	Ground	
49	M66EN	AD[9]	
50	KEYWAY	KEYWAY	5V key
51	KEYWAY	KEYWAY	5V key
52	AD[8]	C/BE[0]#	
53	AD[7]	+3.3V	
54	+3.3V	AD[6]	
55	AD[5]	AD[4]	
56	AD[3]	Ground	
57	Ground	AD[2]	
58	AD[1]	AD[0]	
59	+V I/O	+V I/O	
60	ACK64#	REQ64#	
61	+5V	+5V	
62	+5V	+5V	32-bit end
	KEYWAY	KEYWAY	64-bit spacer
	KEYWAY	KEYWAY	64-bit spacer
63	Reserved	Ground	64-bit start
64	Ground	C/BE[7]#	
65	C/BE[6]#	C/BE[5]#	
66	C/BE[4]#	+V I/O	
67	Ground	PAR64	
68	AD[63]	AD[62]	
69	AD[61]	Ground	
70	+V I/O	AD[60]	
71	AD[59]	AD[58]	
72	AD[57]	Ground	
73	Ground	AD[56]	
74	AD[55]	AD[54]	
75	AD[53]	+V I/O	
76	Ground	AD[52]	
77	AD[51]	AD[50]	
78	AD[49]	Ground	
79	+V I/O	AD[48]	
80	AD[47]	AD[46]	
81	AD[45]	Ground	
82	Ground	AD[44]	
83	AD[43]	AD[42]	
84	AD[41]	+V I/O	
85	Ground	AD[40]	
86	AD[39]	AD[38]	
87	AD[37]	Ground	
88	+V I/O	AD[36]	
89	AD[35]	AD[34]	
90	AD[33]	Ground	
91	Ground	AD[32]	
92	Reserved	Reserved	
93	Reserved	Ground	
94	Ground	Reserved	

APPENDIX F - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX G - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Logic Analyzer User's Manual

Tektronix DAS9200 / TLA500 System User's Manual

Tektronix 92A96 / 92C96 Module User's Manual

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