



# NEX-PCI64EXHD

## PCI Bus Adapter Users Manual

Including these Software Support packages:  
PCI64X                      PCI64X32

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## **1.0 OVERVIEW**

### **1.1 General Information**

The NEX-PCI64EXHD adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA600/700, a 92A96, or a 92C96 acquisition module to a 64-bit PCI backplane. (The PCI designation refers to the Peripheral Component Interconnect Local Bus specification.) Connections are made through P6434/P6860 Mass Termination probes when using a TLA600/700, and through a DASMTIF interface when using a 92A/C96 card. Both the P6434/P6860 probes and the DASMTIF are available from Tektronix.

Two different NEX-PCI64EXHD cards are available. One supports a +5V target; the other supports a +3.3V target. Each card has its edge connector keyed for the specific voltage support, and cannot be plugged into a wrong slot. Two different boards were necessary to prevent damage that might be caused by accidentally plugging a +3.3V target into a +5V slot.

The included NEX-PCI64X and NEX-PCI32X software permits the acquisition of all PCI bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. For instance, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA600/700 apply to a TLA704 or TLA711 chassis with one or more 7X3/4 acquisition card.

Appendix D is a silk-screen print of the NEX-PCI64EXHD Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the PCI Local Bus specification and the Tektronix TLA600/700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA600/700, it is expected that the user is familiar with Windows O.S.

If 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix F for contact information.

## **2.0 SOFTWARE INSTALLATION**

Two 3½” diskettes have been included with the NEX-PCI64EXHD Bus Adapter. They are for use with the TLA600/700 series. One disk is for 64-bit PCI (PCI64X) and the other is for 32-bit PCI (PCI32X). Diskettes for the DAS9200 or TLA500 are available upon request. See Appendix F for contact information.

### **2.1 TLA600/700**

The NEX-PCI64X / NEX-PCI32X software is loaded in the same method as other Win95 programs. Place the appropriate Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the PCI64X or PCI32X support in its proper place on the hard disk.

To load PCI64X or PCI32X support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose PCI64X or PCI32X and click on **Okay**.

### **2.2 DAS9200**

The included diskettes should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing "PCI64X Support" or "PCI32X Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

## **3.0 CONFIGURING the NEX-PCI64EXHD BUS ADAPTER**

### **3.1 General Information**

Not all 64-bit PCI signals are monitored by either the DAS9200 or the TLA600/700. (Refer to Table 1 or Table 2 for a list of acquired signals.) The remaining signals have been brought to a 2x14 header so that they can be monitored, if desired, simply by connecting unused data channels to them. The signals are on the pins nearest the signal names. The leftmost row of pins (opposite the signal names) are all connected to signal ground.

Use the supplied jumper to short or break the connection between TDI and TDO (JP1). If the target card does not support JTAG Boundary Scan then the two pins should be shorted together.

## **4.0 CONNECTING to the NEX-PCI64EXHD ADAPTER**

### **4.1 General**

The NEX-PCI64EXHD is an extender card that is also designed to permit monitoring the PCI bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will violate the PCI specification for stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, Schottky diode bus terminators have been added to each signal to reduce any signal reflections or voltage spikes. It is entirely possible, however, that placing a target card onto the NEX-PCI64EXHD extender will result in improper operation of the target card or the target system.

### **4.2 TLA600/700 - 64-bit Operation**

To use a TLA600/700 with the NEX-PCI64EXHD adapter board it is necessary to use the P6434 high-density probes for connecting to the board. Each P6434 probe consists of one high-density probe tip (which connects to the adapter board) and two module ends (which connect to the acquisition card). It is important to note that where the module ends connect to the acquisition card will depend on how many channels the acquisition card has. Be very careful in noting where Pin 1 is on each probe tip, and follow the P6434/P6860 Mass Termination Probe manual for instructions on applying the labels.

When using a 7X3/4 102/136-channel acquisition module for 64-bit support, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. One P6434/P6860 plugs onto the Group A connector on the 64EXHD and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434/P6860 plugs onto the Group C connector on the 64EXHD and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. The third P6434/P6860 plugs onto the Group D connector on the 64EXHD and then connects to the Yellow (D0 and D1) and Blue (D2 and D3) locations on the acquisition card. Table 1 shows the wiring and Channel Grouping for the 102/136-channel TLA600/700 NEX-PCI64EXHD connection.

### **4.3 TLA600/700 - 32-bit Operation**

For 32-bit support with the NEX-PCI64EXHD the necessary acquisition data sections are A0-A3 and C0-C3. One P6434/P6860 plugs onto the Group A connector on the 64EXHD and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434/P6860 plugs onto the Group C connector on the 64EXHD and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. Table 2 shows the

32-bit wiring and Channel Grouping for the 102/136-channel TLA600/700 NEX-PCI64EXHD connection.

#### **4.4 92A96 - 64-bit Operation**

When using a 92A96 or 92C96 acquisition card, connection to the 64EXHD is made through the DASMTIF interface adapter. For 64-bit operation, connect the A Probe from the adapter to the Group A connector, the D Probe to the Group D connector, and the C Probe to the Group C connector. Table 1 shows the wiring and Channel Grouping for the 92A96 when used with the NEX-PCI64EXHD adapter.

#### **4.5 92A96 - 32-bit Operation**

For 32-bit support using the NEX-PCI64EXHD, connect the A Probe from the DASMTIF adapter to the Group A connector. Connect the C Probe to the Group C connector. Table 2 shows the wiring and Channel Grouping for the 92A96 when used with the NEX-PCI64EXHD adapter.

Group	Signal	PCI	TLA600/700/ 92A96	Group	Signal	PCI	TLA600/700 / 92A96
Name	Name	Pin #	input	Name	Name	Pin #	input
AD_Hi (Hex)	AD[63]	B68	D3:7	AD_Lo (Hex)	AD[31]	B20	A3:7
	AD[62]	A68	D3:6		AD[30]	A20	A3:6
	AD[61]	B69	D3:5		AD[29]	B21	A3:5
	AD[60]	A70	D3:4		AD[28]	A22	A3:4
	AD[59]	B71	D3:3		AD[27]	B23	A3:3
	AD[58]	A71	D3:2		AD[26]	A23	A3:2
	AD[57]	B72	D3:1		AD[25]	B24	A3:1
	AD[56]	A73	D3:0		AD[24]	A25	A3:0
	AD[55]	B74	D2:7		AD[23]	B27	A2:7
	AD[54]	A74	D2:6		AD[22]	A28	A2:6
	AD[53]	B75	D2:5		AD[21]	B29	A2:5
	AD[52]	A76	D2:4		AD[20]	A29	A2:4
	AD[51]	B77	D2:3		AD[19]	B30	A2:3
	AD[50]	A77	D2:2		AD[18]	A31	A2:2
	AD[49]	B78	D2:1		AD[17]	B32	A2:1
	AD[48]	A79	D2:0		AD[16]	A32	A2:0
	AD[47]	B80	D1:7		AD[15]	A44	A1:7
	AD[46]	A80	D1:6		AD[14]	B45	A1:6
	AD[45]	B81	D1:5		AD[13]	A46	A1:5
	AD[44]	A82	D1:4		AD[12]	B47	A1:4
	AD[43]	B83	D1:3		AD[11]	A47	A1:3
	AD[42]	A83	D1:2		AD[10]	B48	A1:2
	AD[41]	B84	D1:1		AD[9]	A49	A1:1
	AD[40]	A85	D1:0		AD[8]	B52	A1:0
	AD[39]	B86	D0:7		AD[7]	B53	A0:7
	AD[38]	A86	D0:6		AD[6]	A54	A0:6
	AD[37]	B87	D0:5		AD[5]	B55	A0:5
	AD[36]	A88	D0:4		AD[4]	A55	A0:4
	AD[35]	B89	D0:3		AD[3]	B56	A0:3
	AD[34]	A89	D0:2		AD[2]	A57	A0:2
	AD[33]	B90	D0:1		AD[1]	B58	A0:0
	AD[32]	A91	D0:0		AD[0]	A58	A0:1

**Table 1- NEX-PCI64EXHD 92A96/TLA600/700 (102/136-channel) Wiring**

Note: All signals listed above are required for proper disassembly

Group Name	Signal Name	PCI Pin #	TLA700 / 92A96 input	Group Name	Signal Name	PCI Pin #	TLA700 / 92A96 input
Control (Sym)	RST#	A15	+ C3:5	Intrpt (Off)	INTD#	B08	C0:3
	REQ64#	A60	+ C1:0		INTC#	A07	C0:2
	ACK64#	B60	+ C1:1		INTB#	B07	C0:1
	FRAME#	A34	+ C2:0		INTA#	A06	C0:0
	DEVSEL#	B37	+ C3:0	Misc (Off)	REQ#	B18	C0:5
	STOP#	A38	+ C2:3		GNT#	A17	C0:6
	IRDY#	B35	+ C2:1		LOCK#	B39	C3:4
	TRDY#	A36	+ C2:2		IDSEL	A26	C0:4
	C/BE#[7]	A64	+ C1:7		PERR#	B40	C3:3
	C/BE#[6]	B65	+ C1:6		PAR	A43	C3:2
	C/BE#[5]	A65	+ C1:5		SERR#	B42	C3:1
	C/BE#[4]	B66	+ C1:4		CLK	B16	C3:7
	C/BE#[3]	B26	+ C2:7	Ungrouped	SDONE	A40	C3:6
	C/BE#[2]	B33	+ C2:6		SBO#	A41	C1:3
	C/BE#[1]	B44	+ C2:5		M66EN	B49	C0:7
	C/BE#[0]	A52	+ C2:4	Clock:0	unused	-----	
				Clock:1	DEVSEL#	B37	+
			Clock:2	unused	-----		
			Clock:3	CLK	B16	+	

**Table 1 - NEX-PCI64EXHD 92A96/TLA600/700 (102/136-channel) Wiring (cont'd.)**

Note: Signals with a '+' are required for proper clocking / disassembly

Group	Signal	PCI	TLA600/700 / 92A96	Group	Signal	PCI	TLA600/700 / 92A96
Name	Name	Pin #	input	Name	Name	Pin #	input
Addr_Dat (Hex)	AD[31]	B20	+ A3:7	Control (Sym)	RST#	A15	+ C3:5
	AD[30]	A20	+ A3:6		FRAME#	A34	+ C2:0
	AD[29]	B21	+ A3:5		DEVSEL#	B37	+ C3:0
	AD[28]	A22	+ A3:4		STOP#	A38	+ C2:3
	AD[27]	B23	+ A3:3		IRDY#	B35	+ C2:1
	AD[26]	A23	+ A3:2		TRDY#	A36	+ C2:2
	AD[25]	B24	+ A3:1		C/BE#[3]	B26	+ C2:7
	AD[24]	A25	+ A3:0		C/BE#[2]	B33	+ C2:6
	AD[23]	B27	+ A2:7		C/BE#[1]	B44	+ C2:5
	AD[22]	A28	+ A2:6		C/BE#[0]	A52	+ C2:4
	AD[21]	B29	+ A2:5	Intrpt (Off)	INTD#	B08	C0:3
	AD[20]	A29	+ A2:4		INTC#	A07	C0:2
	AD[19]	B30	+ A2:3		INTB#	B07	C0:1
	AD[18]	A31	+ A2:2		INTA#	A06	C0:0
	AD[17]	B32	+ A2:1	Misc (Off)	REQ#	B18	C0:5
	AD[16]	A32	+ A2:0		GNT#	A17	C0:6
	AD[15]	A44	+ A1:7		LOCK#	B39	C3:4
	AD[14]	B45	+ A1:6		IDSEL	A26	C0:4
	AD[13]	A46	+ A1:5		PERR#	B40	C3:3
	AD[12]	B47	+ A1:4		PAR	A43	C3:2
	AD[11]	A47	+ A1:3		SERR#	B42	C3:1
	AD[10]	B48	+ A1:2	CLK	B16	C3:7	
	AD[9]	A49	+ A1:1	Ungrouped	SDONE	A40	C3:6
	AD[8]	B52	+ A1:0		SBO#	A41	C1:3
AD[7]	B53	+ A0:7	ACQ64#		B60	C1:1	
AD[6]	A54	+ A0:6	REQ64#		A60	C1:0	
AD[5]	B55	+ A0:5	M66EN		B49	C0:7	
AD[4]	A55	+ A0:4	Aux_1	Aux_1:[7-0]	-----	D3	
AD[3]	B56	+ A0:3	Clock:0	unused	-----		
AD[2]	A57	+ A0:2		Clock:1	DEVSEL#=	B37	+
AD[1]	B58	+ A0:0		Clock:2	unused	-----	
AD[0]	A58	+ A0:1		Clock:3	CLK=	B16	+
Aux_0	Aux_0:[7-0]	-----	D2				

**Table 2- NEX-PCI64EXHD 32 bit 92A96/TLA600/700 (102/136-channel) Wiring**

Note: Signals with a '+' are required for proper clocking / disassembly

## **5.0 CLOCK SELECTION**

### **5.1 General Information**

There are three clocking options available when using either the NEX-PCI64X or NEX-PCI32X support package. Each selection is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

When using a DAS9200 or TLA500, the clocking selection is made in the Clock menu. Choose the desired mode in the Clocking Select field, then press <RETURN>.

### **5.2 Clocking Options - Explanation**

**Bus Cycle Acquisition** - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

**Dual Address Capable (32-bit only)** - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

**Every CLK Rising Edge** - In this mode, data will be acquired on every rising edge of the PCI CLK signal. The disassembly will filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

## 6.0 VIEWING DATA

### 6.1 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PCI64X and PCI64X-MagniVu (or PCI32X and PCI32X-MagniVu when using 32-bit support). The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PCI64X-MagniVu (or PCI32X-MagniVu), will show all of the channels in 8GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

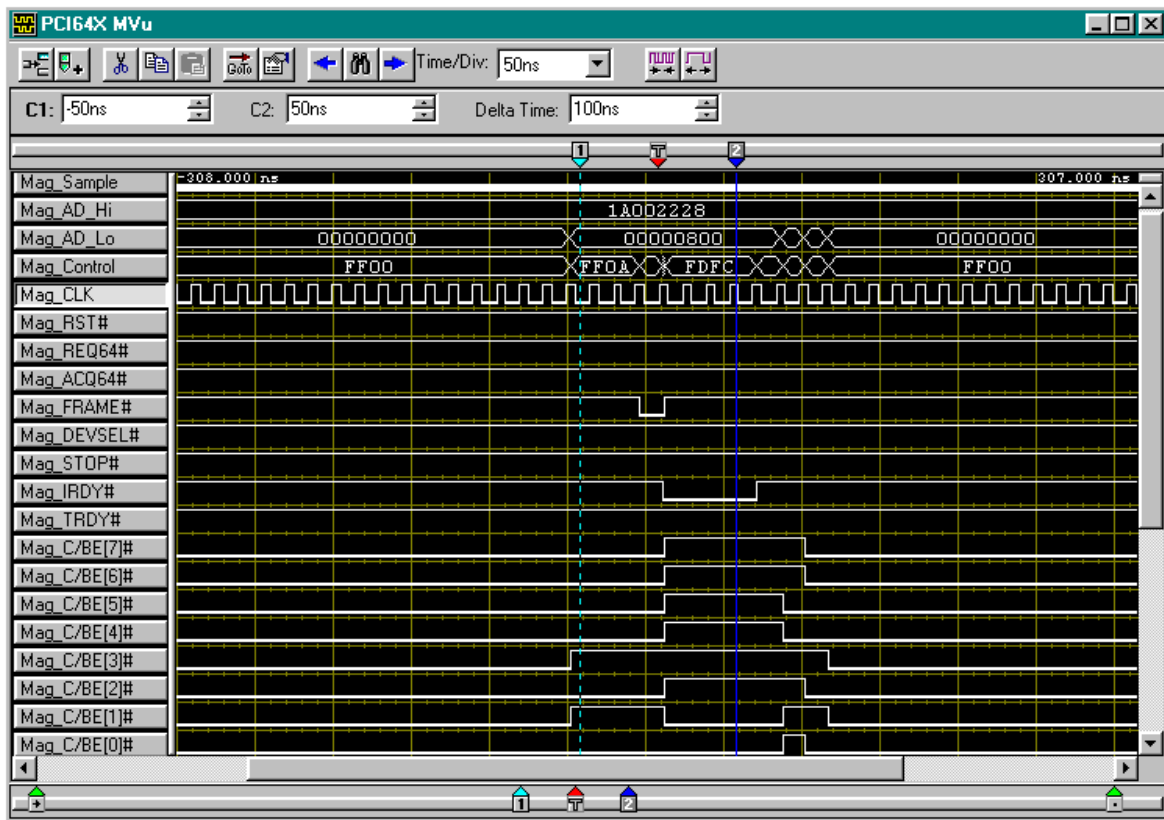


Figure 1- PCI64X MagniVu Display on TLA600/700

## 6.2 Viewing State Data on the DAS9200/TLA500

After an acquisition is made the DAS9200 Logic Analyzer will display the data in State Display mode (as a default only). Address / Data information is displayed in hexadecimal format; Control data is displayed using symbols; Interrupt, Miscellaneous, and both Auxiliary data groups default to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. A symbol table (PCI64X\_Ctrl, Table 3 for 64-bit support; PCI32X\_Ctrl, Table 4 for 32-bit support) has been provided to show the type of transaction that occurred on the PCI bus. This symbol table quickly shows whether the acquisition was a memory or I/O operation, a read or a write, etc.

It is important to note that changing the group, channel, or wiring of the Control group can result in incorrect symbol information being displayed.

## 6.3 Viewing Timing Data on the DAS9200/TLA500

It may be useful to display acquired information using the Timing Diagram display of the DAS9200. (Note that, unlike some other logic analyzers, with the DAS9200 there is no need to re-acquire PCI data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the DAS9200 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

Pattern	TLA600/700 / 92A96 Symbols	Meaning
0xxxxxxxxxxxx	RESET	Reset
101111xxxx0000	INTERRUPT ACK	Interrupt Acknowledge
101111xxxx0001	SPECIAL CYCLE	Special Cycle
101111xxxx0010	I/O READ ADDRESS	I/O Read
101111xxxx0011	I/O WRITE ADDRESS	I/O Write
101111xxxx010x	RESERVED	Reserved
101111xxxx0110	MEMORY READ ADDRESS	Memory Read
101111xxxx0111	MEMORY WRITE ADDRESS	Memory Write
101111xxxx100x	RESERVED	Reserved
101111xxxx1010	CONFIG READ ADDRESS	Configuration Read
101111xxxx1011	CONFIG WRITE ADDRESS	Configuration Write
101111xxxx1100	MEMORY READ MULTIPLE	Memory Read Multiple
101111xxxx1101	DUAL ADDRESS	Dual Address Cycle
101111xxxx1110	MEMORY READ LINE	Memory Read Line
101111xxxx1111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
111101xxxxxxxx	WAIT/MASTER ABORT	Wait or Master Abort
111001xxxxxxxx	TARGET ABORT	Target Abort
110001xxxxxxxx	RETRY	Retry Cycle
1x0x0011111110	BYTE 0	Byte 0 valid (D0-7)
1x0x0011111101	BYTE 1	Byte 1 valid (D8-15)
1x0x0011111011	BYTE 2	Byte 2 valid (D16-23)
1x0x0011110111	BYTE 3	Byte 3 valid (D24-31)
1x0x0011101111	BYTE 4	Byte 4 valid (D32-39)
1x0x0011011111	BYTE 5	Byte 5 valid (D40-47)
1x0x0010111111	BYTE 6	Byte 6 valid (D48-55)
1x0x0001111111	BYTE 7	Byte 7 valid (D56-63)
1x0x0011111100	BYTES 0,1	Bytes 0 & 1 valid (D0-15)
1x0x0011110011	BYTES 2,3	Bytes 2 & 3 valid (D16-31)
1x0x0011001111	BYTES 4,5	Bytes 4 & 5 valid (D32-47)
1x0x0000111111	BYTES 6,7	Bytes 6 & 7 valid (D48-63)
1x0x0011110000	BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x0000001111	BYTES 4-7	Bytes 4-7 valid (D32-63)
1x0x0000000000	BYTES 0-7	Bytes 0-3 valid (D0-63)
1x0x0011111111	INVALID DATA	Invalid Data
1xxxxxxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxxxxxx	FRAME LO	Frame Lo

**Table 3- PCI64X\_Ctrl Control Symbol Table**

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

Pattern	TLA600/700 / 92A96 Symbols	Meaning
0xxxxxxxxx	RESET	Reset
1011110000	INTERRUPT ACK	Interrupt Acknowledge
1011110001	SPECIAL CYCLE	Special Cycle
1011110010	I/O READ ADDRESS	I/O Read
1011110011	I/O WRITE ADDRESS	I/O Write
101111010x	RESERVED	Reserved
1011110110	MEMORY READ ADDRESS	Memory Read
1011110111	MEMORY WRITE ADDRESS	Memory Write
101111100x	RESERVED	Reserved
1011111010	CONFIG READ ADDRESS	Configuration Read
1011111011	CONFIG WRITE ADDRESS	Configuration Write
1011111100	MEMORY READ MULTIPLE	Memory Read Multiple
1011111101	DUAL ADDRESS	Dual Address Cycle
1011111110	MEMORY READ LINE	Memory Read Line
1011111111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
111101xxxx	WAIT/MASTER ABORT	Wait or Master Abort
111001xxxx	TARGET ABORT	Target Abort
110001xxxx	RETRY	Retry Cycle
1x0x001110	DATA - BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA - BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA - BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA - BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA - BYTES 0 & 1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA - BYTES 2 & 3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA - BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo

**Table 4- PCI32X\_Ctrl Control Symbol Table**

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

## **7.0 USING the DISASSEMBLY SOFTWARE**

### **7.1 General**

The PCI64X and PCI32X support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the PCI64X and PCI32X software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the PCI64X / PCI32X software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 125ps in the TLA600/700 series, and to 10ns in the DAS9200 / TLA500, permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

### **7.2 Disassembly Using the TLA600/700**

The TLA600/700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window

Sample	PCI64X AD_Hi	PCI64X AD_Lo	PCI64X Mnemonics	Timestamp
	-----	FFFE0000	Memory Not Prefetchable	
	-----	FFFE0000	Decoder for 128KB Memory Space	
438	-----	04000010	CONFIG WRITE ADDRESS	6.904,570,000 ms
	-----	04000010	Type 0 Register 4 Function 0	
439	-----	00000000	CONFIG WRITE DATA	6.904,600,000 ms
	-----	00000000	Write to Base Address Register 0	
440	-----	04000008	CONFIG READ ADDRESS	6.908,491,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
441	-----	03000002	CONFIG READ DATA	6.908,536,500 ms
	-----	03000002	Class 0x03 - Display controller	
	-----	03000002	Sub-Class 0x00	
	-----	03000002	Prog. I/F 0x00 - VGA compatible	
	-----	03000002	Revision ID 2	
442	-----	04000010	CONFIG READ ADDRESS	6.937,764,500 ms
	-----	04000010	Type 0 Register 4 Function 0	
443	-----	-----00	CONFIG READ DATA	6.937,809,000 ms
	-----	-----00	Invalid Base Address data	
	-----	-----00	Base Address Register 0	
	-----	-----00	Memory Address Register	
	-----	-----00	Locate anywhere in 32-bit space	
	-----	-----00	Memory Not Prefetchable	
	-----	-----00	Decoder for 16 bytes Memory Space	
444	-----	04000008	CONFIG READ ADDRESS	6.941,296,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
445	-----	03000002	CONFIG READ DATA	6.941,341,500 ms

Figure 2- PCI64X Disassembly

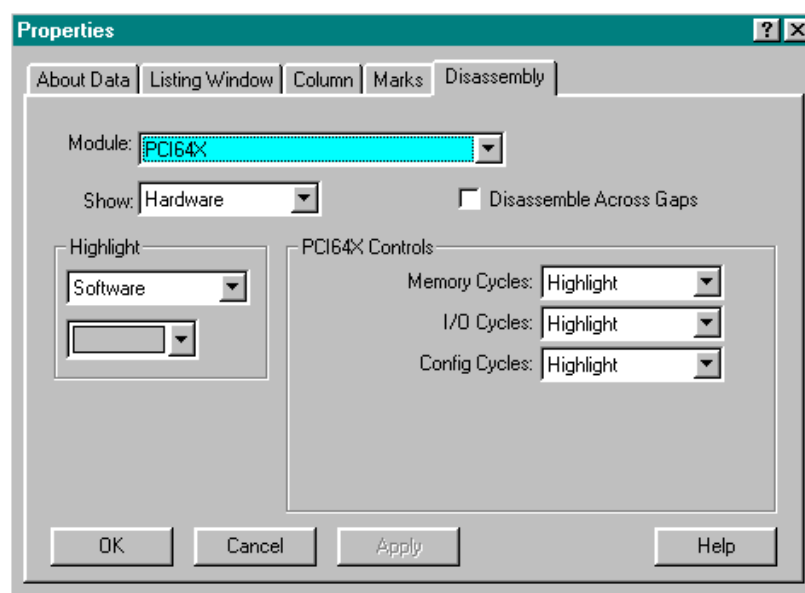


Figure 3- PCI64X Cycle Filtering Window

contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark (disabled in PCI64SW)

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PCI64X / PCI32X disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

### 7.3 Disassembly Using the DAS9200 / TLA500

To view PCI64X or PCI32X data in Disassembly form, simply click on the DISASM button in the lower part of the DAS/TLA display, or select Disasm in the Display column of the Main Menu. All PCI transactions will be displayed and disassembled, and the Timestamp between each acquisition is displayed (Relative mode). To change the Timestamp format, press (or click) **F5** (Display Format) and open the Timestamp select field. The options available are: Relative (time from the previous sample), Delta (time from a user definable Delta mark), Absolute (time from when the acquisition card was started), and Off. Making a choice, closing the field, then pressing (or clicking) **F8** to Exit and Save will modify the Disassembly display appropriately.

To filter the displayed data, again move to the Display Format screen (press or click **F5**). The Hardware Display Mode (default) will display all PCI cycles by default.

By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Display Mode select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Display Mode select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Relative form) will be updated to show the time between displayed cycles.

## **APPENDIX A - Necessary Signals for Clocking**

To properly acquire PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

## **APPENDIX B - Considerations**

The NEX-PCI64EXHD is an extender card that is also designed to permit monitoring the PCI bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will violate the PCI specification for stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, Schottky diode bus terminators have been added to each signal to reduce any signal reflections or voltage spikes. It is entirely possible, however, that placing a target card onto the NEX-PCI64EXHD extender will result in improper operation of the target card.

## **APPENDIX C - PCI Local Bus Pinout**

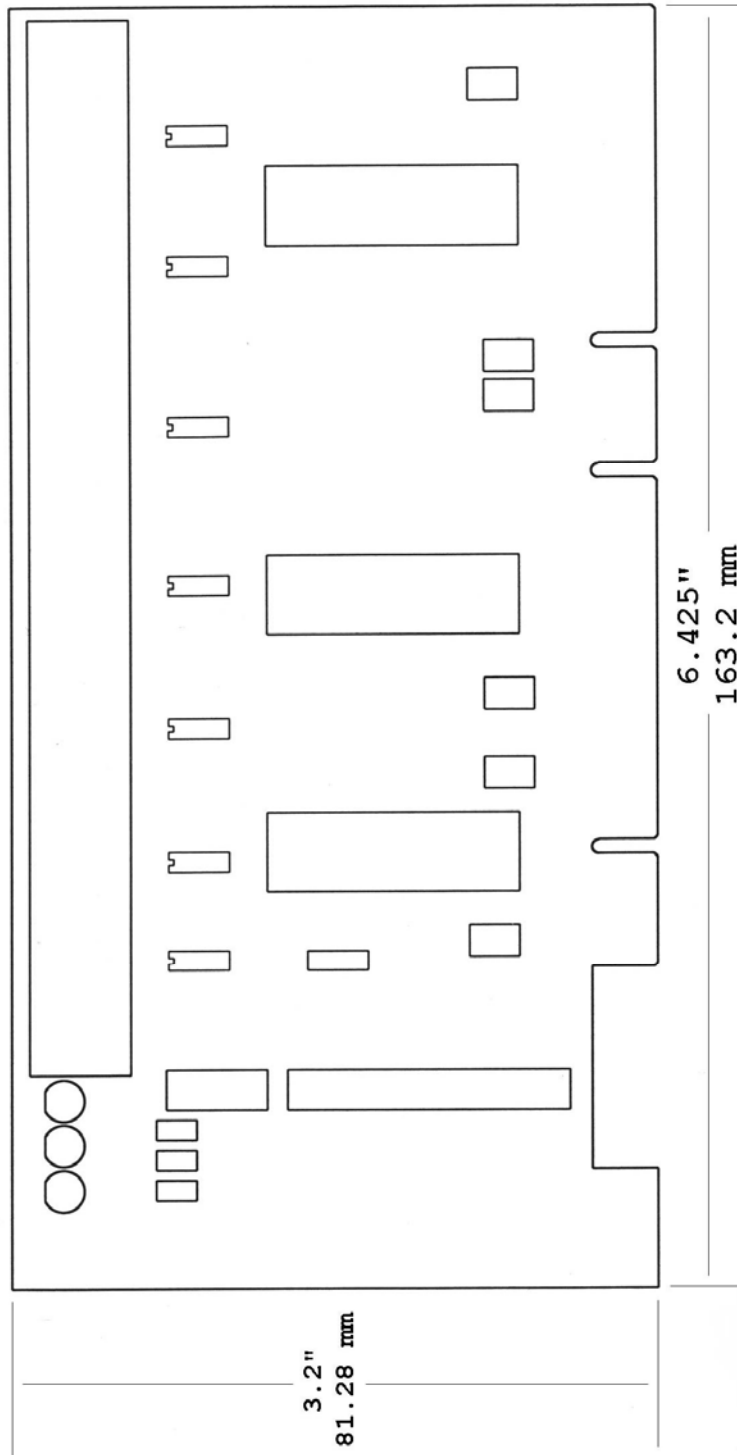
Information given here is for the +5V and +3.3V PCI Board definitions:

<b>Pin #</b>	<b>+5V Side B Component Side</b>	<b>+5V Side A Solder Side</b>	<b>+3.3V Side B Component Side</b>	<b>+3.3V Side A Solder Side</b>	<b>Comments</b>
1	-12V	TRST#	-12V	TRST#	32-bit start
2	TCK	+12V	TCK	+12V	
3	Ground	TMS	Ground	TMS	
4	TDO	TDI	TDO	TDI	
5	+5V	+5V	+5V	+5V	
6	+5V	INTA#	+5V	INTA#	
7	INTB#	INTC#	INTB#	INTC#	
8	INTD#	+5V	INTD#	+5V	
9	PRSENT1#	Reserved	PRSENT1#	Reserved	
10	Reserved	+5V	Reserved	+3.3V	
11	PRSENT2#	Reserved	PRSENT2#	Reserved	
12	Ground	Ground	KEYWAY	KEYWAY	3.3V key
13	Ground	Ground	KEYWAY	KEYWAY	
14	Reserved	Reserved	Reserved	Reserved	
15	Ground	RST#	Ground	RST#	
16	CLK	+5V	CLK	+3.3V	
17	Ground	GNT#	Ground	GNT#	
18	REQ#	Ground	REQ#	Ground	
19	+V I/O	Reserved	+V I/O	Reserved	
20	AD[31]	AD[30]	AD[31]	AD[30]	
21	AD[29]	+3.3V	AD[29]	+3.3V	
22	Ground	AD[28]	Ground	AD[28]	
23	AD[27]	AD[26]	AD[27]	AD[26]	
24	AD[25]	Ground	AD[25]	Ground	
25	+3.3V	AD[24]	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	AD[23]	+3.3V	
28	Ground	AD[22]	Ground	AD[22]	
29	AD[21]	AD[20]	AD[21]	AD[20]	
30	AD[19]	Ground	AD[19]	Ground	
31	+3.3V	AD[18]	+3.3V	AD[18]	
32	AD[17]	AD[16]	AD[17]	AD[16]	

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
33	C/BE[2]#	+3.3V	C/BE[2]#	+3.3V	
34	Ground	FRAME#	Ground	FRAME#	
35	IRDY#	Ground	IRDY#	Ground	
36	+3.3V	TRDY#	+3.3V	TRDY#	
37	DEVSEL#	Ground	DEVSEL#	Ground	
38	Ground	STOP#	Ground	STOP#	
39	LOCK#	+3.3V	LOCK#	+3.3V	
40	PERR#	SDONE	PERR#	SDONE	
41	+3.3V	SBO#	+3.3V	SBO#	
42	SERR#	Ground	SERR#	Ground	
43	+3.3V	PAR	+3.3V	PAR	
44	C/BE[1]#	AD[15]	C/BE[1]#	AD[15]	
45	AD[14]	+3.3V	AD[14]	+3.3V	
46	Ground	AD[13]	Ground	AD[13]	
47	AD[12]	AD[11]	AD[12]	AD[11]	
48	AD[10]	Ground	AD[10]	Ground	
49	Ground	AD[9]	M66EN	AD[9]	
50	KEYWAY	KEYWAY	Ground	Ground	5V key
51	KEYWAY	KEYWAY	Ground	Ground	5V key
52	AD[8]	C/BE[0]#	AD[8]	C/BE[0]#	
53	AD[7]	+3.3V	AD[7]	+3.3V	
54	+3.3V	AD[6]	+3.3V	AD[6]	
55	AD[5]	AD[4]	AD[5]	AD[4]	
56	AD[3]	Ground	AD[3]	Ground	
57	Ground	AD[2]	Ground	AD[2]	
58	AD[1]	AD[0]	AD[1]	AD[0]	
59	+5V	+5V	+3.3V	+3.3V	
60	ACK64#	REQ64#	ACK64#	REQ64#	
61	+5V	+5V	+5V	+5V	
62	+5V	+5V	+5V	+5V	32-bit end

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
	KEYWAY	KEYWAY	KEYWAY	KEYWAY	64-bit spacer
	KEYWAY	KEYWAY	KEYWAY	KEYWAY	64-bit spacer
63	Reserved	Ground	Reserved	Ground	
64	Ground	C/BE[7]#	Ground	C/BE[7]#	
65	C/BE[6]#	C/BE[5]#	C/BE[6]#	C/BE[5]#	
66	C/BE[4]#	+5V	C/BE[4]#	+3.3V	
67	Ground	PAR64	Ground	PAR64	
68	AD[63]	AD[62]	AD[63]	AD[62]	
69	AD[61]	Ground	AD[61]	Ground	
70	+5V	AD[60]	+3.3V	AD[60]	
71	AD[59]	AD[58]	AD[59]	AD[58]	
72	AD[57]	Ground	AD[57]	Ground	
73	Ground	AD[56]	Ground	AD[56]	
74	AD[55]	AD[54]	AD[55]	AD[54]	
75	AD[53]	+5V	AD[53]	+3.3V	
76	Ground	AD[52]	Ground	AD[52]	
77	AD[51]	AD[50]	AD[51]	AD[50]	
78	AD[49]	Ground	AD[49]	Ground	
79	+5V	AD[48]	+3.3V	AD[48]	
80	AD[47]	AD[46]	AD[47]	AD[46]	
81	AD[45]	Ground	AD[45]	Ground	
82	Ground	AD[44]	Ground	AD[44]	
83	AD[43]	AD[42]	AD[43]	AD[42]	
84	AD[41]	+5V	AD[41]	+3.3V	
85	Ground	AD[40]	Ground	AD[40]	
86	AD[39]	AD[38]	AD[39]	AD[38]	
87	AD[37]	Ground	AD[37]	Ground	
88	+5V	AD[36]	+3.3V	AD[36]	
89	AD[35]	AD[34]	AD[35]	AD[34]	
90	AD[33]	Ground	AD[33]	Ground	
91	Ground	AD[32]	Ground	AD[32]	
92	Reserved	Reserved	Reserved	Reserved	
93	Reserved	Ground	Reserved	Ground	
94	Ground	Reserved	Ground	Reserved	64-bit end

**APPENDIX D - NEX-PCI64EXHD Outline**



## APPENDIX E - NEX-PCI64EXHD Mictor Pinout

Tek Mictor Pin #	AMP Mictor Pin #	TLA600/700 Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/700 Channel	PCI Signal Name	PCI Pin #
3	5	CLK:0	unused	----	36	6	CLK:1 <sup>1</sup>	DEVSEL#	B37
4	7	A3:7	AD[31]	B20	35	8	A1:7	AD[15]	A44
5	9	A3:6	AD[30]	A20	34	10	A1:6	AD[14]	B45
6	11	A3:5	AD[29]	B21	33	12	A1:5	AD[13]	A46
7	13	A3:4	AD[28]	A22	32	14	A1:4	AD[12]	B47
8	15	A3:3	AD[27]	B23	31	16	A1:3	AD[11]	A47
9	17	A3:2	AD[26]	A23	30	18	A1:2	AD[10]	B48
10	19	A3:1	AD[25]	B24	29	20	A1:1	AD[9]	A49
11	21	A3:0	AD[24]	A25	28	22	A1:0	AD[8]	B52
12	23	A2:7	AD[23]	B27	27	24	A0:7	AD[7]	B53
13	25	A2:6	AD[22]	A28	26	26	A0:6	AD[6]	A54
14	27	A2:5	AD[21]	B29	25	28	A0:5	AD[5]	B55
15	29	A2:4	AD[20]	A29	24	30	A0:4	AD[4]	A55
16	31	A2:3	AD[19]	B30	23	32	A0:3	AD[3]	B56
17	33	A2:2	AD[18]	A31	22	34	A0:2	AD[2]	A57
18	35	A2:1	AD[17]	B32	21	36	A0:1	AD[0]	A58
19	37	A2:0	AD[16]	A32	20	38	A0:0	AD[1]	B58

### Group A Mictor Connector

Notes:

1. DEVSEL# is also connected to C3:0
2. All signals on this Mictor required for proper 32- or 64-bit disassembly

Tek Mictor Pin #	AMP Mictor Pin #	TLA600 /700 Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600/ 700 Channel	PCI Signal Name	PCI Pin #
3	5	CLK:3 <sup>1</sup>	CLK	B16	36	6	QUAL:1	unused	----
4	7	C3:7	CLK	B16	35	8	C1:7 <sup>3</sup>	C/BE[7]#	A64
5	9	C3:6	SDONE	A40	34	10	C1:6 <sup>3</sup>	C/BE[6]#	B65
6	11	C3:5 <sup>2</sup>	RST#	A15	33	12	C1:5 <sup>3</sup>	C/BE[5]#	A65
7	13	C3:4	LOCK#	B39	32	14	C1:4 <sup>3</sup>	C/BE[4]#	B66
8	15	C3:3	PERR#	B40	31	16	C1:3	SBO#	A41
9	17	C3:2	PAR	A43	30	18	C1:2	PAR64	A67
10	19	C3:1	SERR#	B42	29	20	C1:1 <sup>3</sup>	ACQ64#	B60
11	21	C3:0 <sup>2</sup>	DEVSEL#	B37	28	22	C1:0 <sup>3</sup>	REQ64#	A60
12	23	C2:7 <sup>2</sup>	C/BE[3]#	B26	27	24	C0:7	M66EN	B49
13	25	C2:6 <sup>2</sup>	C/BE[2]#	B33	26	26	C0:6	GNT#	A17
14	27	C2:5 <sup>2</sup>	C/BE[1]#	B44	25	28	C0:5	REQ#	B18
15	29	C2:4 <sup>2</sup>	C/BE[0]#	A52	24	30	C0:4	IDSEL	A26
16	31	C2:3 <sup>2</sup>	STOP#	A38	23	32	C0:3	INTD#	B08
17	33	C2:2 <sup>2</sup>	TRDY#	A36	22	34	C0:2	INTC#	A07
18	35	C2:1 <sup>2</sup>	IRDY#	B35	21	36	C0:1	INTB#	B07
19	37	C2:0 <sup>2</sup>	FRAME#	A34	20	38	C0:0	INTA#	A06

### Group C Mictor Connector

Notes:

1. CLK is also connected to C3:7
2. These signals are required for proper 32- or 64-bit disassembly
3. These signals are required for proper 64-bit disassembly

<b>Tek Mictor Pin #</b>	<b>AMP Mictor Pin #</b>	<b>TLA600 /700 Channel</b>	<b>PCI Signal Name</b>	<b>PCI Pin #</b>	<b>Tek Mictor Pin #</b>	<b>AMP Mictor Pin #</b>	<b>TLA600 /700 Channel</b>	<b>PCI Signal Name</b>	<b>PCI Pin #</b>
3	5	QUAL:0	unused	----	36	6	CLK:2	unused	----
4	7	D3:7	AD[63]	B68	35	8	D1:7	AD[47]	B80
5	9	D3:6	AD[62]	A68	34	10	D1:6	AD[46]	A80
6	11	D3:5	AD[61]	B69	33	12	D1:5	AD[45]	B81
7	13	D3:4	AD[60]	A70	32	14	D1:4	AD[44]	A82
8	15	D3:3	AD[59]	B71	31	16	D1:3	AD[43]	B83
9	17	D3:2	AD[58]	A71	30	18	D1:2	AD[42]	A83
10	19	D3:1	AD[57]	B72	29	20	D1:1	AD[41]	B84
11	21	D3:0	AD[56]	A73	28	22	D1:0	AD[40]	A85
12	23	D2:7	AD[55]	B74	27	24	D0:7	AD[39]	B86
13	25	D2:6	AD[54]	A74	26	26	D0:6	AD[38]	A86
14	27	D2:5	AD[53]	B75	25	28	D0:5	AD[37]	B87
15	29	D2:4	AD[52]	A76	24	30	D0:4	AD[36]	A88
16	31	D2:3	AD[51]	B77	23	32	D0:3	AD[35]	B89
17	33	D2:2	AD[50]	A77	22	34	D0:2	AD[34]	A89
18	35	D2:1	AD[49]	B78	21	36	D0:1	AD[33]	B90
19	37	D2:0	AD[48]	A79	20	38	D0:0	AD[32]	A91

### Group D Mictor Connector

Notes:

1. All signals on this Mictor required for proper 64-bit disassembly

## **APPENDIX F - Support**

### **About Nexus Technology, Inc.**



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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TEL: 877-595-8116  
FAX: 877-595-8118

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### **Support Contact Information**

Technical Support	<b><a href="mailto:techsupport@nexustechnology.com">techsupport@nexustechnology.com</a></b>
General Information	<b><a href="mailto:support@nexustechnology.com">support@nexustechnology.com</a></b>
Quote Requests	<b><a href="mailto:quotes@nexustechnology.com">quotes@nexustechnology.com</a></b>

We will try to respond within one business day.

### **If Problems Are Found**

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

## **APPENDIX G - References**

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

Tektronix DAS9200 / TLA500 System User's Manual

Tektronix 92A96 / 92C96 Module User's Manual

PCI Local Bus Specification

Production Version; Revision 2.1s - June 1, 1995

Published by:

PCI Special Interest Group

PO Box 14070

Portland OR 97214

800-433-5177 (U.S.)

503-797-4207 (International)

503-234-6762 (FAX)

PCI System Architecture

Third Edition

Mindshare, Inc. (Tom Shanley / Don Anderson)

Published by Addison Wesley

ISBN 0-201-40993-3