



NEX-PCI64HS User Manual

Including these Software Support packages:

PCI32HS PCI64HS
PCI32HSD PCI64HSD

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1.0 Overview

1.1 General Information

The NEX-PCI64HS adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel Tektronix TLA600/700/5200 Logic Analyzer to a 32 or 64-bit PCI backplane. (The PCI designation refers to the Peripheral Component Interconnect Local Bus specification.) Connections are made through P6434 Mass Termination (Mictor) probe points.

Two different NEX-PCI64HS cards are available. One supports a +5V target; the other supports a +3.3V target. Each card has its edge connector keyed for the specific voltage support, and cannot be plugged into a wrong slot. Two different boards were necessary to prevent damage that might be caused by accidentally plugging a +3.3V target into a +5V slot.

The included support software permits the acquisition of all PCI bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. For instance, references to the TLA apply to a suitably configured TLA600, TLA5200 or TLA700 logic analyzer.

Appendix D is a silk-screen print of the NEX-PCI64HS Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the PCI Local Bus specification and the Tektronix TLA Logic Analyzers. It is also expected that the user is familiar with the version of Windows installed on the TLA being used.

Please see Appendix I for Nexus Technology contact information.

2.0 Software Installation

2.1 General Support Software Information

Four 3½” diskettes have been included with the NEX-PCI64HS Bus Adapter. The particular support needed depends on the PCI bus and the Tektronix probing method used. Please note that hardware requirements differ depending on the probing method used. For more information on the hardware requirements and setup please see Section 4.0.

Support	PCI Bus	TLA Probes Required
PCI32HS	32-bit	P6434, P6419 or P6860
PCI64HS	64-bit	P6434, P6419 or P6860
PCI32HSD	32-bit	P6960
PCI64HSD	64-bit	P6960

2.2 Loading the Support into the TLA

The support software is loaded in the same method as other Windows programs. Place the appropriate Install disk in the floppy drive of the TLA. Select **Control Panel** and run **Add/Remove Programs**, choose **Install, Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose PCI64HS, PCI64HSD, PCI32HS or PCI64HSD and click on **Okay**.

3.0 Configuring the NEX-PCI64HS Bus Adapter

3.1 General Information

Use the supplied jumper to short or break the connection between TDI and TDO (JP1). If the target card does not support JTAG Boundary Scan then the two pins should be shorted together.

4.0 Connecting to the NEX-PCI64HS Adapter

4.1 General

The NEX-PCI64HS is an extender card that is also designed to permit monitoring the PCI bus signals. This permits the user to see exactly what is happening at the target. Every effort has been taken to keep trace length as short as possible. It is entirely possible, however, that placing a target card onto the NEX-PCI64HS extender will result in improper operation of the target card or the target system.

Although designed for use with P6434 High-Density probes it is possible, using adapters, to use other acquisition probes. The hardware and software requirements for the different analyzer and probe combinations can be found in the table below.

Tek. Probes Required		PCI Support	Probing Adapters Required		Tek. Module Requirement 102-ch minimum	Support Software Required
Type	Qty		Type	Qty		
P6434 Mictor	2	32-bit	None	0	TLA7Lx/Mx/Nx/Px/Qx TLA603/4	PCI32HS
P6434 Mictor	3	64-bit	None	0	TLA7Lx/Mx/Nx/Px/Qx TLA603/4	PCI64HS
P6860 or P6419 Compression	3	32-bit	Tektronix 020-2457-00 34-Ch. Mictor-on-PCB to P6860 Compression	2	TLA7AAx , TLA7ABx or TLA5203/4	PCI32HS
P6860 or P6419 Compression	3	64-bit	Tektronix 020-2457-00 34-Ch. Mictor-on-PCB to P6860 Compression	3	TLA7AAx, TLA7ABx or TLA5203/4	PCI64HS
P6960 D-Max™ Probing Technology	3	32-bit	Nexus NEX-M2P69X Mictor to P6960 Adapter	3	TLA7AAx or TLA7ABx	PCI32HSD
P6960 D-Max™ Probing Technology	3	64-bit	Nexus NEX-M2P69X Mictor to P6960 Adapter	3	TLA7AAx or TLA7ABx	PCI64HSD

Table 1 - PCI Support Cross Reference

4.2 32- / 64-bit Operation using P6434 Probes

The NEX-PCI64HS adapter board is designed to be used with P6434 high-density probes for the TLA logic analyzer connections. Each P6434 probe consists of one high-density probe tip (which connects to the adapter board) and two module ends (which connect to the acquisition card). Be very careful in noting where Pin 1 is on each probe tip, and follow the P6434 Mass Termination Probe manual for instructions on applying the labels.

When using a 102-/136-channel logic analyzer with P6434 probes for 64-bit support using the PCI64HS support package, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. One P6434 plugs onto the Group A connector on the NEX-PCI64HS

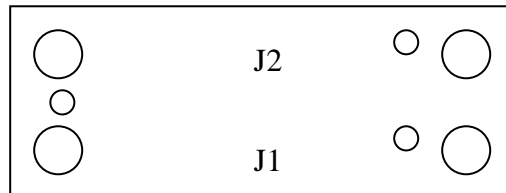
adapter and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434 plugs onto the Group C connector on the adapter and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. The third P6434 plugs onto the Group D connector and then connects to the Yellow (D0 and D1) and Blue (D2 and D3) locations on the acquisition card. Table 2 shows the wiring and Channel Grouping defined by the PCI64HS support software.

For 32-bit support using the PCI32HS support package the necessary acquisition data sections are A0-A3 and C0-C3. One P6434 plugs onto the Group A connector on the NEX-PCI64HS adapter and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434 plugs onto the Group C connector on the adapter and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. Table 3 shows the 32-bit wiring and Channel Grouping defined by the PCI32HS support software.

4.3 32- / 64-bit Operation using P6860 and P6419 Probes

By using Mictor-on-PCB-to-Compression adapters available from Tektronix (their P/N 020-2457-00) it is possible to use P6860 or P6419 compression probes with the Mictor connectors on the NEX-PCI64HS adapter. For 64-bit PCI support the PCI64HS support software should be used, and the channel grouping and wiring is shown in Table 2. For 32-bit support the PCI32HS support software should be used, and its channel grouping and wiring is shown in Table 3.

The top view of these adapters is as follows:



The J1 side of the adapter interfaces the odd-numbered Mictor pins to a P6860 or P6419 probe (hereafter referred to as Compression probe); the J2 side of the adapter interfaces the even-numbered Mictor to a Compression probe (based on the Amp pin numbering definition). When connecting the Compression probes to the adapter a single 17-channel Compression probe head will be connected to either J1 or J2. These connections are to be made as follows:

NEX-PCI64HS Group A Mictor			
J1	to	P6860/P6419	A3/A3
J2	to	P6860/P6419	A1/A0

NEX-PCI64HS Group C Mictor

J1 to P6860/P6419 C3/C2
J2 to P6860/P6419 C1/C0

NEX-PCI64HS Group D Mictor (64-bit support only)

J1 to P6860/P6419 D3/D2
J2 to P6860/P6419 D1/D0

4.4 32- / 64-bit Operation using P6960 Probes

By using Nexus Technology's NEX-M2P69X Mictor-to-P69XX probe adapters it is possible to use P6960 D-Max probes with the Mictor connectors on the NEX-PCI64HS adapter. For 64-bit PCI support the PCI64HSD support software should be used, and the channel grouping and wiring is shown in Table 4. For 32-bit support the PCI32HSD support software should be used, and its channel grouping and wiring is shown in Table 5.

The High A/D P6960 probe (containing TLA input sections A3, A2, D3 and D2) should be connected to the Group A Mictor on the PCI64HS adapter. The Low A/D probe (containing TLA input sections A1, A0, D1 and D0) should be connected to the Group D Mictor. The C probe should be connected to the Group C Mictor.

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
AD_Hi (Hex)	AD[63]	B68	D3:7	AD_Lo (Hex)	AD[31]	B20	A3:7
	AD[62]	A68	D3:6		AD[30]	A20	A3:6
	AD[61]	B69	D3:5		AD[29]	B21	A3:5
	AD[60]	A70	D3:4		AD[28]	A22	A3:4
	AD[59]	B71	D3:3		AD[27]	B23	A3:3
	AD[58]	A71	D3:2		AD[26]	A23	A3:2
	AD[57]	B72	D3:1		AD[25]	B24	A3:1
	AD[56]	A73	D3:0		AD[24]	A25	A3:0
	AD[55]	B74	D2:7		AD[23]	B27	A2:7
	AD[54]	A74	D2:6		AD[22]	A28	A2:6
	AD[53]	B75	D2:5		AD[21]	B29	A2:5
	AD[52]	A76	D2:4		AD[20]	A29	A2:4
	AD[51]	B77	D2:3		AD[19]	B30	A2:3
	AD[50]	A77	D2:2		AD[18]	A31	A2:2
	AD[49]	B78	D2:1		AD[17]	B32	A2:1
	AD[48]	A79	D2:0		AD[16]	A32	A2:0
	AD[47]	B80	D1:7		AD[15]	A44	A1:7
	AD[46]	A80	D1:6		AD[14]	B45	A1:6
	AD[45]	B81	D1:5		AD[13]	A46	A1:5
	AD[44]	A82	D1:4		AD[12]	B47	A1:4
	AD[43]	B83	D1:3		AD[11]	A47	A1:3
	AD[42]	A83	D1:2		AD[10]	B48	A1:2
	AD[41]	B84	D1:1		AD[9]	A49	A1:1
	AD[40]	A85	D1:0		AD[8]	B52	A1:0
	AD[39]	B86	D0:7		AD[7]	B53	A0:7
	AD[38]	A86	D0:6		AD[6]	A54	A0:6
	AD[37]	B87	D0:5		AD[5]	B55	A0:5
	AD[36]	A88	D0:4		AD[4]	A55	A0:4
	AD[35]	B89	D0:3		AD[3]	B56	A0:3
	AD[34]	A89	D0:2		AD[2]	A57	A0:2
	AD[33]	B90	D0:1		AD[1]	B58	A0:0
	AD[32]	A91	D0:0		AD[0]	A58	A0:1

Note: All signals listed above are required for proper disassembly

Table 2 - PCI64HS Channel Grouping and Wiring

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
Control (Sym)	RST#	A15	+ Clock:3	Intrpt (Off)	INTD#	B08	C0:3
	REQ64#	A60	+ C1:5		INTC#	A07	C0:2
	ACK64#	B60	+ C0:7		INTB#	B07	C0:1
	FRAME#	A34	+ C2:0		INTA#	A06	C0:0
	DEVSEL#	B37	+ Clock:1	Misc (Off)	REQ#	B18	C0:5
	STOP#	A38	+ C2:3		GNT#	A17	C0:6
	IRDY#	B35	+ C2:1		LOCK#	B39	C2:6
	TRDY#	A36	+ C2:2		IDSEL	A26	C0:4
	C/BE#[7]	A64	+ C3:7		PERR#	B40	C2:5
	C/BE#[6]	B65	+ C3:6		PAR	A43	C2:4
	C/BE#[5]	A65	+ C3:5		SERR	B42	Clock:2
	C/BE#[4]	B66	+ C3:4	CLK	B16	+ Clock:0	
	C/BE#[3]	B26	+ C3:3	Ungrouped	PAR64	A67	C1:4
	C/BE#[2]	B33	+ C3:2		SBO#	A41	C2:7
C/BE#[1]	B44	+ C3:1	M66EN		B49	C1:6	
C/BE#[0]	A52	+ C3:0	SERR#		B42	Clock:2	
			SDONE		A40	Qual:0	

Note: Signals with a '+' are required for proper clocking / disassembly

Table 2 - PCI64HS Channel Grouping and Wiring (cont'd.)

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
Addr_Dat (Hex)	AD[31]	B20	A3:7	Control (Sym)	RST#	A15	+ Clock:3
	AD[30]	A20	A3:6		FRAME#	A34	+ C2:0
	AD[29]	B21	A3:5		DEVSEL#	B37	+ Clock:1
	AD[28]	A22	A3:4		STOP#	A38	+ C2:3
	AD[27]	B23	A3:3		IRDY#	B35	+ C2:1
	AD[26]	A23	A3:2		TRDY#	A36	+ C2:2
	AD[25]	B24	A3:1		C/BE#[3]	B26	+ C3:3
	AD[24]	A25	A3:0		C/BE#[2]	B33	+ C3:2
	AD[23]	B27	A2:7		C/BE#[1]	B44	+ C3:1
	AD[22]	A28	A2:6		C/BE#[0]	A52	+ C3:0
	AD[21]	B29	A2:5	Intrpt (Off)	INTD#	B08	C0:3
	AD[20]	A29	A2:4		INTC#	A07	C0:2
	AD[19]	B30	A2:3		INTB#	B07	C0:1
	AD[18]	A31	A2:2		INTA#	A06	C0:0
	AD[17]	B32	A2:1	Misc (Off)	REQ#	B18	C0:5
	AD[16]	A32	A2:0		GNT#	A17	C0:6
	AD[15]	A44	A1:7		LOCK#	B39	C2:6
	AD[14]	B45	A1:6		IDSEL	A26	C0:4
	AD[13]	A46	A1:5		PERR#	B40	C2:5
	AD[12]	B47	A1:4		PAR	A43	C2:4
AD[11]	A47	A1:3	SERR		B42	Clock:2	
AD[10]	B48	A1:2	CLK	B16	+ Clock:0		
AD[9]	A49	A1:1	Ungrouped	SBO#	A41	C2:7	
AD[8]	B52	A1:0		M66EN	B49	C1:6	
AD[7]	B53	A0:7		SERR#	B42	Clock:2	
AD[6]	A54	A0:6		SDONE	A40	Qual:0	
AD[5]	B55	A0:5					
AD[4]	A55	A0:4					
AD[3]	B56	A0:3					
AD[2]	A57	A0:2					
AD[1]	B58	A0:0					
AD[0]	A58	A0:1					

Note: All signals listed above are required for proper disassembly

Table 3 - PCI32HS Channel Grouping and Wiring

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
AD_Hi (Hex)	AD[63]	B68	A1:7	AD_Lo (Hex)	AD[31]	B20	A3:7
	AD[62]	A68	A1:6		AD[30]	A20	A3:6
	AD[61]	B69	A1:5		AD[29]	B21	A3:5
	AD[60]	A70	A1:4		AD[28]	A22	A3:4
	AD[59]	B71	A1:3		AD[27]	B23	A3:3
	AD[58]	A71	A1:2		AD[26]	A23	A3:2
	AD[57]	B72	A1:1		AD[25]	B24	A3:1
	AD[56]	A73	A1:0		AD[24]	A25	A3:0
	AD[55]	B74	A0:7		AD[23]	B27	A2:7
	AD[54]	A74	A0:6		AD[22]	A28	A2:6
	AD[53]	B75	A0:5		AD[21]	B29	A2:5
	AD[52]	A76	A0:4		AD[20]	A29	A2:4
	AD[51]	B77	A0:3		AD[19]	B30	A2:3
	AD[50]	A77	A0:2		AD[18]	A31	A2:2
	AD[49]	B78	A0:1		AD[17]	B32	A2:1
	AD[48]	A79	A0:0		AD[16]	A32	A2:0
	AD[47]	B80	D1:7		AD[15]	A44	D3:7
	AD[46]	A80	D1:6		AD[14]	B45	D3:6
	AD[45]	B81	D1:5		AD[13]	A46	D3:5
	AD[44]	A82	D1:4		AD[12]	B47	D3:4
	AD[43]	B83	D1:3		AD[11]	A47	D3:3
	AD[42]	A83	D1:2		AD[10]	B48	D3:2
	AD[41]	B84	D1:1		AD[9]	A49	D3:1
	AD[40]	A85	D1:0		AD[8]	B52	D3:0
	AD[39]	B86	D0:7		AD[7]	B53	D2:7
	AD[38]	A86	D0:6		AD[6]	A54	D2:6
	AD[37]	B87	D0:5		AD[5]	B55	D2:5
	AD[36]	A88	D0:4		AD[4]	A55	D2:4
	AD[35]	B89	D0:3		AD[3]	B56	D2:3
	AD[34]	A89	D0:2		AD[2]	A57	D2:2
	AD[33]	B90	D0:1		AD[1]	B58	D2:0
	AD[32]	A91	D0:0		AD[0]	A58	D2:1

Note: All signals listed above are required for proper disassembly

Table 4 - PCI64HSD Channel Grouping and Wiring

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
Control (Sym)	RST#	A15	+ Clock:3	Intrpt (Off)	INTD#	B08	C0:3
	REQ64#	A60	+ C1:5		INTC#	A07	C0:2
	ACK64#	B60	+ C0:7		INTB#	B07	C0:1
	FRAME#	A34	+ C2:0		INTA#	A06	C0:0
	DEVSEL#	B37	+ Qual0	Misc (Off)	REQ#	B18	C0:5
	STOP#	A38	+ C2:3		GNT#	A17	C0:6
	IRDY#	B35	+ C2:1		LOCK#	B39	C2:6
	TRDY#	A36	+ C2:2		IDSEL	A26	C0:4
	C/BE#[7]	A64	+ C3:7		PERR#	B40	C2:5
	C/BE#[6]	B65	+ C3:6		PAR	A43	C2:4
	C/BE#[5]	A65	+ C3:5		SERR	B42	Clock:2
	C/BE#[4]	B66	+ C3:4	CLK	B16	+ Clock:0	
	C/BE#[3]	B26	+ C3:3	Ungrouped	PAR64	A67	C1:4
	C/BE#[2]	B33	+ C3:2		SBO#	A41	C2:7
C/BE#[1]	B44	+ C3:1	M66EN		B49	C1:6	
C/BE#[0]	A52	+ C3:0	SERR#		B42	Clock:2	
			SDONE		A40	Clock:1	

Note: Signals with a '+' are required for proper clocking / disassembly

Table 4 - PCI64HSD Channel Grouping and Wiring (cont'd.)

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
Addr_Dat (Hex)	AD[31]	B20	A3:7	Control (Sym)	RST#	A15	+ Clock:3
	AD[30]	A20	A3:6		FRAME#	A34	+ C2:0
	AD[29]	B21	A3:5		DEVSEL#	B37	+ Qual:0
	AD[28]	A22	A3:4		STOP#	A38	+ C2:3
	AD[27]	B23	A3:3		IRDY#	B35	+ C2:1
	AD[26]	A23	A3:2		TRDY#	A36	+ C2:2
	AD[25]	B24	A3:1		C/BE#[3]	B26	+ C3:3
	AD[24]	A25	A3:0		C/BE#[2]	B33	+ C3:2
	AD[23]	B27	A2:7		C/BE#[1]	B44	+ C3:1
	AD[22]	A28	A2:6		C/BE#[0]	A52	+ C3:0
	AD[21]	B29	A2:5	Intrpt (Off)	INTD#	B08	C0:3
	AD[20]	A29	A2:4		INTC#	A07	C0:2
	AD[19]	B30	A2:3		INTB#	B07	C0:1
	AD[18]	A31	A2:2		INTA#	A06	C0:0
	AD[17]	B32	A2:1	Misc (Off)	REQ#	B18	C0:5
	AD[16]	A32	A2:0		GNT#	A17	C0:6
	AD[15]	A44	D3:7		LOCK#	B39	C2:6
	AD[14]	B45	D3:6		IDSEL	A26	C0:4
	AD[13]	A46	D3:5		PERR#	B40	C2:5
	AD[12]	B47	D3:4		PAR	A43	C2:4
AD[11]	A47	D3:3	SERR		B42	Clock:2	
AD[10]	B48	D3:2	CLK	B16	+ Clock:0		
AD[9]	A49	D3:1	Ungrouped	SBO#	A41	C2:7	
AD[8]	B52	D3:0		M66EN	B49	C1:6	
AD[7]	B53	D2:7		SERR#	B42	Clock:2	
AD[6]	A54	D2:6		SDONE	A40	Clock:1	
AD[5]	B55	D2:5					
AD[4]	A55	D2:4					
AD[3]	B56	D2:3					
AD[2]	A57	D2:2					
AD[1]	B58	D2:0					
AD[0]	A58	D2:1					

Note: All signals listed above are required for proper disassembly

Table 5 - PCI32HSD Channel Grouping and Wiring

5.0 Clock Selection

5.1 General Information

There are three clocking options available when using the NEX-PCI64HS software support packages. Each selection is explained in detail below.

The clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.2 Clocking Options – Explanation

Bus Cycle Acquisition

This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable (PCI32HS and PCI32HSD only)

In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid non-Dual Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge

In this mode, data will be acquired on every rising edge of the PCI CLK signal. Although the display software will attempt to filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

6.0 Viewing Data

6.1 Viewing Timing Data on the TLA

By default, the TLA will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: the main acquisition memory of the card (shown as PCI64HS, PCI64HSD, PCI32HS or PCI32HSD) and MagniVu acquisition memory (shown as PCI64HS-MagniVu, PCI64HSD-MagniVu, PCI32HS-Magnivu or PCI32HSD-MagniVu). The first choice (main acquisition memory) will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, MagniVu memory, will show all of the channels in 2GHz or 8GHz MagniVu mode (dependent on the acquisition card), so that edge relationships can be examined in greater detail. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

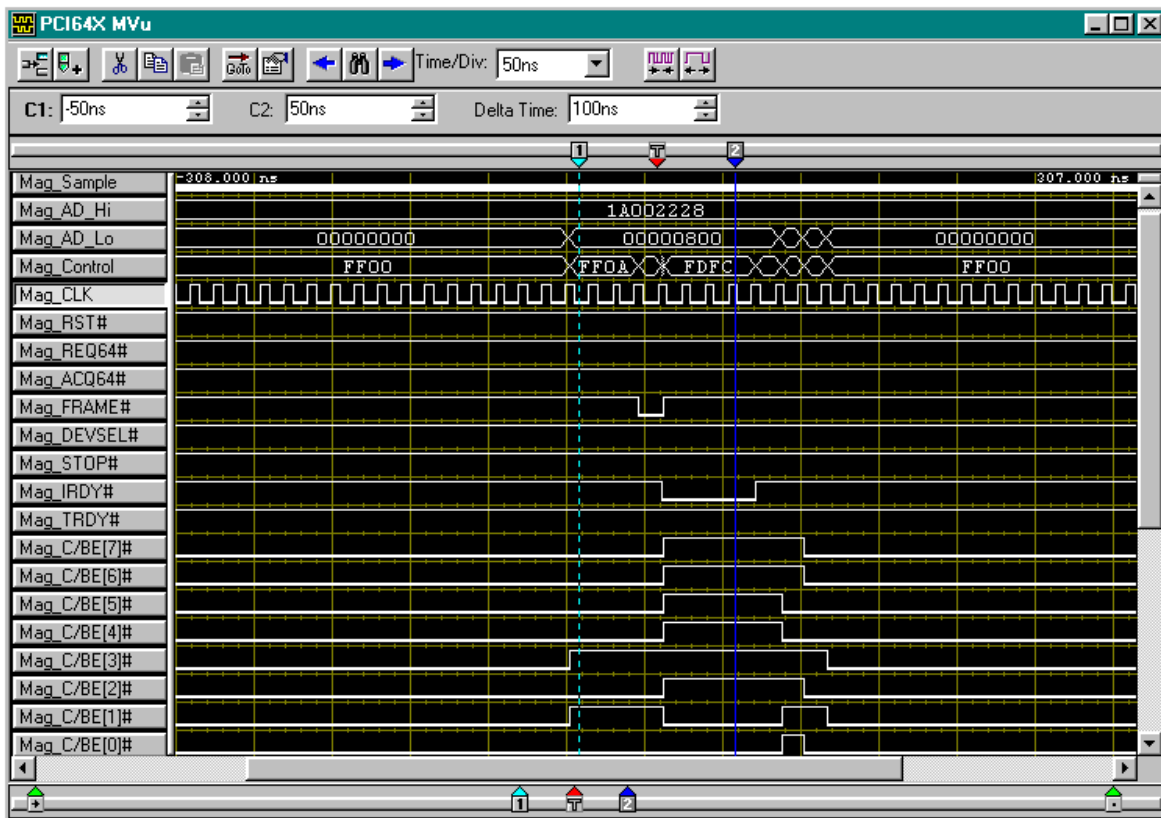


Figure 1 - PCI64HS MagniVu Display

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

Pattern	TLA Symbols	Meaning
0xxxxxxxxxxxxxx	RESET	Reset
1xx01111xxxx0000	INTERRUPT ACK	Interrupt Acknowledge
1xx01111xxxx0001	SPECIAL CYCLE	Special Cycle
1xx01111xxxx0010	I/O READ ADDR	I/O Read Address
1xx01111xxxx0011	I/O WRITE ADDR	I/O Write Address
1xx01111xxxx010x	RESERVED	Reserved
1xx01111xxxx0110	MEMORY RD DWORD ADDR	Memory Read DWORD Address
1xx01111xxxx0111	MEMORY WR ADDR	Memory Write Address
1xx01111xxxx1010	CONFIG READ ADDR	Configuration Read Address
1xx01111xxxx1011	CONFIG WRITE ADDRESS	Configuration Write Address
1xx01111xxxx1101	DUAL ADDR	Dual Address Cycle
1xx01111xxxx1110	MEMORY READ BLOCK	Memory Read Block
1xx01111xxxx1111	MEMORY WRITE BLOCK	Memory Write Block
1xx11101xxxxxxx	WAIT/MASTER ABORT	Wait or Master Abort
1xx11001xxxxxxx	TARGET ABORT	Target Abort
1xx10001xxxxxxx	RETRY	Retry Cycle
111x0x0011111110	BYTE 0	Byte 0 valid (D0-7)
111x0x0011111101	BYTE 1	Byte 1 valid (D8-15)
111x0x0011111011	BYTE 2	Byte 2 valid (D16-23)
111x0x0011110111	BYTE 3	Byte 3 valid (D24-31)
111x0x0011101111	BYTE 4	Byte 4 valid (D32-39)
111x0x0011011111	BYTE 5	Byte 5 valid (D40-47)
111x0x0010111111	BYTE 6	Byte 6 valid (D48-55)
111x0x0001111111	BYTE 7	Byte 7 valid (D56-63)
111x0x0011111100	BYTES 0,1	Bytes 0 & 1 valid (D0-15)
111x0x0011110011	BYTES 2,3	Bytes 2 & 3 valid (D16-31)
111x0x0011001111	BYTES 4,5	Bytes 4 & 5 valid (D32-47)
111x0x0000111111	BYTES 6,7	Bytes 6 & 7 valid (D48-63)
111x0x0011110000	BYTES 0-3	Bytes 0-3 valid (D0-31)
111x0x0000001111	BYTES 4-7	Bytes 4-7 valid (D32-63)
100x0x0000000000	BYTES 0-7	Bytes 0-7 valid (D0-63)
111x0x00xxx0000	LOW 32-BITS	Bytes 0-3 valid (D0-31)
1xxx0x0011111111	INVALID DATA	Invalid Data
1xx1xxxxxxxxxxxx	FRAME HI	Frame Hi
1xx0xxxxxxxxxxxx	FRAME LO	Frame Lo

Signals, from left to right: RST#, REQ64#, ACQ64#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

Table 6 - PCI64HS / PCI64HSD Control Symbol Table

Pattern	TLA Symbols	Meaning
0xxxxxxxxx	RESET	Reset
1011110000	INTERRUPT ACK	Interrupt Acknowledge
1011110001	SPECIAL CYCLE	Special Cycle
1011110010	I/O READ ADDR	I/O Read Address
1011110011	I/O WRITE ADDR	I/O Write Address
101111010x	RESERVED	Reserved
1011110110	MEMORY RD DWORD ADDR	Memory Read DWORD Address
1011110111	MEMORY WR ADDR	Memory Write Address
1011111010	CONFIG READ ADDR	Configuration Read Address
1011111011	CONFIG WRITE ADDRESS	Configuration Write Address
1011111101	DUAL ADDR	Dual Address Cycle
1011111110	MEMORY READ BLOCK	Memory Read Block
1011111111	MEMORY WRITE BLOCK	Memory Write Block
111101xxxx	WAIT/MASTER ABORT	Wait or Master Abort
111001xxxx	TARGET ABORT	Target Abort
110001xxxx	RETRY	Retry Cycle
1x0x001110	DATA BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA BYTES 0,1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA BYTES 2,3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#,
C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

Table 7 – PCI32HS / PCI32HSD Control Symbol Table

7.0 Using the Disassembly Software

7.1 General

The NEX-PCI64HS software supports decode the PCI bus transactions and display the information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the NEX-PCI64HS software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the PCI64HS/D and PCI32HS/D software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps or 125ps in the TLA (depending on the acquisition card used), permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Display

The TLA application, since it is a Windows program, has a similar type of user interface as other Windows-based applications. Please refer to the TLA Users Manual for detailed information on what can be done in the Listing display window.

Sample	PCI64X AD_Hi	PCI64X AD_Lo	PCI64X Mnemonics	Timestamp
	-----	FFFE0000	Memory Not Prefetchable	
	-----	FFFE0000	Decoder for 128KB Memory Space	
438	-----	04000010	CONFIG WRITE ADDRESS	6.904,570,000 ms
	-----	04000010	Type 0 Register 4 Function 0	
439	-----	00000000	CONFIG WRITE DATA	6.904,600,000 ms
	-----	00000000	Write to Base Address Register 0	
440	-----	04000008	CONFIG READ ADDRESS	6.908,491,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
441	-----	03000002	CONFIG READ DATA	6.908,536,500 ms
	-----	03000002	Class 0x03 - Display controller	
	-----	03000002	Sub-Class 0x00	
	-----	03000002	Prog. I/F 0x00 - VGA compatible	
	-----	03000002	Revision ID 2	
442	-----	04000010	CONFIG READ ADDRESS	6.937,764,500 ms
	-----	04000010	Type 0 Register 4 Function 0	
443	-----	-----00	CONFIG READ DATA	6.937,809,000 ms
	-----	-----00	Invalid Base Address data	
	-----	-----00	Base Address Register 0	
	-----	-----00	Memory Address Register	
	-----	-----00	Locate anywhere in 32-bit space	
	-----	-----00	Memory Not Prefetchable	
	-----	-----00	Decoder for 16 bytes Memory Space	
444	-----	04000008	CONFIG READ ADDRESS	6.941,296,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
445	-----	03000002	CONFIG READ DATA	6.941,341,500 ms

Figure 2 - PCI64HS Disassembly

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one),

and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PCI disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

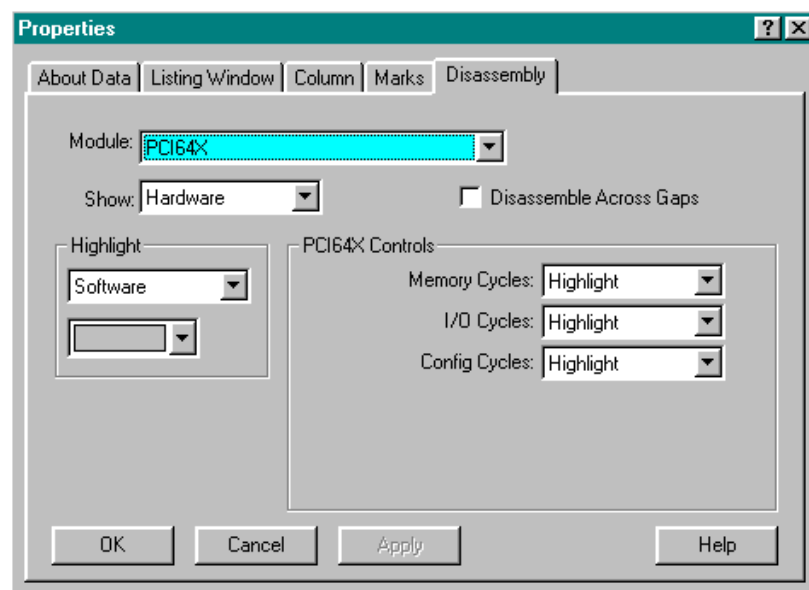


Figure 3 - PCI64HS Cycle Filtering Window

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

Appendix A: Necessary Signals for Clocking

To properly acquire PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

Appendix B: Considerations

The NEX-PCI64HS is an extender card that is also designed to permit monitoring the PCI bus signals. This permits the user to see exactly what is happening at the target. Every effort has been taken to keep trace length as short as possible. It is entirely possible, however, that placing a target card onto the NEX-PCI64HS extender will result in improper operation of the target card.

Appendix C: PCI Local Bus Pinout

Information given here is for the +5V and +3.3V PCI Board definitions:

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
1	-12V	TRST#	-12V	TRST#	32-bit start
2	TCK	+12V	TCK	+12V	
3	Ground	TMS	Ground	TMS	
4	TDO	TDI	TDO	TDI	
5	+5V	+5V	+5V	+5V	
6	+5V	INTA#	+5V	INTA#	
7	INTB#	INTC#	INTB#	INTC#	
8	INTD#	+5V	INTD#	+5V	
9	PRSNT1#	Reserved	PRSNT1#	Reserved	
10	Reserved	+5V	Reserved	+3.3V	
11	PRSNT2#	Reserved	PRSNT2#	Reserved	
12	Ground	Ground	KEYWAY	KEYWAY	3.3V key
13	Ground	Ground	KEYWAY	KEYWAY	
14	Reserved	Reserved	Reserved	Reserved	3.3V key
15	Ground	RST#	Ground	RST#	
16	CLK	+5V	CLK	+3.3V	
17	Ground	GNT#	Ground	GNT#	
18	REQ#	Ground	REQ#	Ground	
19	+V I/O	Reserved	+V I/O	Reserved	
20	AD[31]	AD[30]	AD[31]	AD[30]	
21	AD[29]	+3.3V	AD[29]	+3.3V	
22	Ground	AD[28]	Ground	AD[28]	
23	AD[27]	AD[26]	AD[27]	AD[26]	
24	AD[25]	Ground	AD[25]	Ground	
25	+3.3V	AD[24]	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	AD[23]	+3.3V	
28	Ground	AD[22]	Ground	AD[22]	
29	AD[21]	AD[20]	AD[21]	AD[20]	
30	AD[19]	Ground	AD[19]	Ground	
31	+3.3V	AD[18]	+3.3V	AD[18]	
32	AD[17]	AD[16]	AD[17]	AD[16]	

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
33	C/BE[2]#	+3.3V	C/BE[2]#	+3.3V	
34	Ground	FRAME#	Ground	FRAME#	
35	IRDY#	Ground	IRDY#	Ground	
36	+3.3V	TRDY#	+3.3V	TRDY#	
37	DEVSEL#	Ground	DEVSEL#	Ground	
38	Ground	STOP#	Ground	STOP#	
39	LOCK#	+3.3V	LOCK#	+3.3V	
40	PERR#	SDONE	PERR#	SDONE	
41	+3.3V	SBO#	+3.3V	SBO#	
42	SERR#	Ground	SERR#	Ground	
43	+3.3V	PAR	+3.3V	PAR	
44	C/BE[1]#	AD[15]	C/BE[1]#	AD[15]	
45	AD[14]	+3.3V	AD[14]	+3.3V	
46	Ground	AD[13]	Ground	AD[13]	
47	AD[12]	AD[11]	AD[12]	AD[11]	
48	AD[10]	Ground	AD[10]	Ground	
49	Ground	AD[9]	M66EN	AD[9]	
50	KEYWAY	KEYWAY	Ground	Ground	5V key
51	KEYWAY	KEYWAY	Ground	Ground	5V key
52	AD[8]	C/BE[0]#	AD[8]	C/BE[0]#	
53	AD[7]	+3.3V	AD[7]	+3.3V	
54	+3.3V	AD[6]	+3.3V	AD[6]	
55	AD[5]	AD[4]	AD[5]	AD[4]	
56	AD[3]	Ground	AD[3]	Ground	
57	Ground	AD[2]	Ground	AD[2]	
58	AD[1]	AD[0]	AD[1]	AD[0]	
59	+5V	+5V	+3.3V	+3.3V	
60	ACK64#	REQ64#	ACK64#	REQ64#	
61	+5V	+5V	+5V	+5V	
62	+5V	+5V	+5V	+5V	32-bit end

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
	KEYWAY	KEYWAY	KEYWAY	KEYWAY	64-bit spacer
	KEYWAY	KEYWAY	KEYWAY	KEYWAY	64-bit spacer
63	Reserved	Ground	Reserved	Ground	
64	Ground	C/BE[7]#	Ground	C/BE[7]#	
65	C/BE[6]#	C/BE[5]#	C/BE[6]#	C/BE[5]#	
66	C/BE[4]#	+5V	C/BE[4]#	+3.3V	
67	Ground	PAR64	Ground	PAR64	
68	AD[63]	AD[62]	AD[63]	AD[62]	
69	AD[61]	Ground	AD[61]	Ground	
70	+5V	AD[60]	+3.3V	AD[60]	
71	AD[59]	AD[58]	AD[59]	AD[58]	
72	AD[57]	Ground	AD[57]	Ground	
73	Ground	AD[56]	Ground	AD[56]	
74	AD[55]	AD[54]	AD[55]	AD[54]	
75	AD[53]	+5V	AD[53]	+3.3V	
76	Ground	AD[52]	Ground	AD[52]	
77	AD[51]	AD[50]	AD[51]	AD[50]	
78	AD[49]	Ground	AD[49]	Ground	
79	+5V	AD[48]	+3.3V	AD[48]	
80	AD[47]	AD[46]	AD[47]	AD[46]	
81	AD[45]	Ground	AD[45]	Ground	
82	Ground	AD[44]	Ground	AD[44]	
83	AD[43]	AD[42]	AD[43]	AD[42]	
84	AD[41]	+5V	AD[41]	+3.3V	
85	Ground	AD[40]	Ground	AD[40]	
86	AD[39]	AD[38]	AD[39]	AD[38]	
87	AD[37]	Ground	AD[37]	Ground	
88	+5V	AD[36]	+3.3V	AD[36]	
89	AD[35]	AD[34]	AD[35]	AD[34]	
90	AD[33]	Ground	AD[33]	Ground	
91	Ground	AD[32]	Ground	AD[32]	
92	Reserved	Reserved	Reserved	Reserved	
93	Reserved	Ground	Reserved	Ground	
94	Ground	Reserved	Ground	Reserved	64-bit end

Appendix E: NEX-PCI64HS Mictor Pinout

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	CLK:0	CLK	B16	36	6	CLK:1	DEVSEL#	B37
4	7	A3:7	AD[31]	B20	35	8	A1:7	AD[15]	A44
5	9	A3:6	AD[30]	A20	34	10	A1:6	AD[14]	B45
6	11	A3:5	AD[29]	B21	33	12	A1:5	AD[13]	A46
7	13	A3:4	AD[28]	A22	32	14	A1:4	AD[12]	B47
8	15	A3:3	AD[27]	B23	31	16	A1:3	AD[11]	A47
9	17	A3:2	AD[26]	A23	30	18	A1:2	AD[10]	B48
10	19	A3:1	AD[25]	B24	29	20	A1:1	AD[9]	A49
11	21	A3:0	AD[24]	A25	28	22	A1:0	AD[8]	B52
12	23	A2:7	AD[23]	B27	27	24	A0:7	AD[7]	B53
13	25	A2:6	AD[22]	A28	26	26	A0:6	AD[6]	A54
14	27	A2:5	AD[21]	B29	25	28	A0:5	AD[5]	B55
15	29	A2:4	AD[20]	A29	24	30	A0:4	AD[4]	A55
16	31	A2:3	AD[19]	B30	23	32	A0:3	AD[3]	B56
17	33	A2:2	AD[18]	A31	22	34	A0:2	AD[2]	A57
18	35	A2:1	AD[17]	B32	21	36	A0:1	AD[1]	A58
19	37	A2:0	AD[16]	A32	20	38	A0:0	AD[0]	B58

Group A Mictor Connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	CLK:3	RST#	A15	36	6	QUAL:1	<i>Do not use</i>	-----
4	7	C3:7	C/BE[7]#	A64	35	8	C1:7	unused	-----
5	9	C3:6	C/BE[6]#	B65	34	10	C1:6	M66EN	B49
6	11	C3:5	C/BE[5]#	A65	33	12	C1:5	REQ64#	A60
7	13	C3:4	C/BE[4]#	B66	32	14	C1:4	PAR64	A67
8	15	C3:3	C/BE[3]#	B26	31	16	C1:3	unused	-----
9	17	C3:2	C/BE[2]#	B33	30	18	C1:2	unused	-----
10	19	C3:1	C/BE[1]#	B44	29	20	C1:1	unused	-----
11	21	C3:0	C/BE[0]#	A52	28	22	C1:0	unused	-----
12	23	C2:7	SBO#	A41	27	24	C0:7	ACQ64#	B60
13	25	C2:6	LOCK#	B39	26	26	C0:6	GNT#	A17
14	27	C2:5	PERR#	B40	25	28	C0:5	REQ#	B18
15	29	C2:4	PAR	A43	24	30	C0:4	IDSEL	A26
16	31	C2:3	STOP#	A38	23	32	C0:3	INTD#	B08
17	33	C2:2	TRDY#	A36	22	34	C0:2	INTC#	A07
18	35	C2:1	IRDY#	B35	21	36	C0:1	INTB#	B07
19	37	C2:0	FRAME#	A34	20	38	C0:0	INTA#	A06

Group C Mictor Connector

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	QUAL:0	SDONE	A40	36	6	CLK:2	SERR	B42
4	7	D3:7	AD[63]	B68	35	8	D1:7	AD[47]	B80
5	9	D3:6	AD[62]	A68	34	10	D1:6	AD[46]	A80
6	11	D3:5	AD[61]	B69	33	12	D1:5	AD[45]	B81
7	13	D3:4	AD[60]	A70	32	14	D1:4	AD[44]	A82
8	15	D3:3	AD[59]	B71	31	16	D1:3	AD[43]	B83
9	17	D3:2	AD[58]	A71	30	18	D1:2	AD[42]	A83
10	19	D3:1	AD[57]	B72	29	20	D1:1	AD[41]	B84
11	21	D3:0	AD[56]	A73	28	22	D1:0	AD[40]	A85
12	23	D2:7	AD[55]	B74	27	24	D0:7	AD[39]	B86
13	25	D2:6	AD[54]	A74	26	26	D0:6	AD[38]	A86
14	27	D2:5	AD[53]	B75	25	28	D0:5	AD[37]	B87
15	29	D2:4	AD[52]	A76	24	30	D0:4	AD[36]	A88
16	31	D2:3	AD[51]	B77	23	32	D0:3	AD[35]	B89
17	33	D2:2	AD[50]	A77	22	34	D0:2	AD[34]	A89
18	35	D2:1	AD[49]	B78	21	36	D0:1	AD[33]	B90
19	37	D2:0	AD[48]	A79	20	38	D0:0	AD[32]	A91

Group D Mictor Connector

Appendix F: NEX-PCI64HS P6860/P6419 Compression Pinout

For further information on the P6860 / P6419 Connectorless probe compression footprint, please refer to the “P68xx Series Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-04.

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK1-	GND	-----
A13	CK1+	DEVSEL#	B37
B12	A1:7	AD[15]	A44
B10	A1:6	AD[14]	B45
A12	A1:5	AD[13]	A46
A10	A1:4	AD[12]	B47
B9	A1:3	AD[11]	A47
B7	A1:2	AD[10]	B48
A9	A1:1	AD[9]	A49
A7	A1:0	AD[8]	B52
B6	A0:7	AD[7]	B53
B4	A0:6	AD[6]	A54
A6	A0:5	AD[5]	B55
A4	A0:4	AD[4]	A55
B3	A0:3	AD[3]	B56
B1	A0:2	AD[2]	A57
A3	A0:1	AD[1]	A58
A1	A0:0	AD[0]	B58

Probe Connection A0/A1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK0-	GND	-----
A13	CK0+	CLK	B16
B12	A3:7	AD[31]	B20
B10	A3:6	AD[30]	A20
A12	A3:5	AD[29]	B21
A10	A3:4	AD[28]	A22
B9	A3:3	AD[27]	B23
B7	A3:2	AD[26]	A23
A9	A3:1	AD[25]	B24
A7	A3:0	AD[24]	A25
B6	A2:7	AD[23]	B27
B4	A2:6	AD[22]	A28
A6	A2:5	AD[21]	B29
A4	A2:4	AD[20]	A29
B3	A2:3	AD[19]	B30
B1	A2:2	AD[18]	A31
A3	A2:1	AD[17]	B32
A1	A2:0	AD[16]	A32

Probe Connection A2/A3

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	Q1-	GND	-----
A13	Q1+	Do not use	DNU
B12	C1:7	unused	-----
B10	C1:6	M66EN	B49
A12	C1:5	REQ64#	A60
A10	C1:4	PAR64	A67
B9	C1:3	unused	-----
B7	C1:2	unused	-----
A9	C1:1	unused	-----
A7	C1:0	unused	-----
B6	C0:7	ACQ64#	B60
B4	C0:6	GNT#	A17
A6	C0:5	REQ#	B18
A4	C0:4	IDSEL	A26
B3	C0:3	INTD#	B08
B1	C0:2	INTC#	A07
A3	C0:1	INTB#	B07
A1	C0:0	INTA#	A06

Probe Connection C0/C1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK3-	GND	-----
A13	CLK3+	RST#	A15
B12	C3:7	C/BE[7]#	A64
B10	C3:6	C/BE[6]#	B65
A12	C3:5	C/BE[5]#	A65
A10	C3:4	C/BE[4]#	B66
B9	C3:3	C/BE[3]#	B26
B7	C3:2	C/BE[2]#	B33
A9	C3:1	C/BE[1]#	B44
A7	C3:0	C/BE[0]#	A52
B6	C2:7	SBO#	A41
B4	C2:6	LOCK#	B39
A6	C2:5	PERR#	B40
A4	C2:4	PAR	A43
B3	C2:3	STOP#	A38
B1	C2:2	TRDY#	A36
A3	C2:1	IRDY#	B35
A1	C2:0	FRAME#	A34

Probe Connection C2/C3

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK2-	GND	-----
A13	CK2	SERR	B42
B12	D1:7	AD[47]	B80
B10	D1:6	AD[46]	A80
A12	D1:5	AD[45]	B81
A10	D1:4	AD[44]	A82
B9	D1:3	AD[43]	B83
B7	D1:2	AD[42]	A83
A9	D1:1	AD[41]	B84
A7	D1:0	AD[40]	A85
B6	D0:7	AD[39]	B86
B4	D0:6	AD[38]	A86
A6	D0:5	AD[37]	B87
A4	D0:4	AD[36]	A88
B3	D0:3	AD[35]	B89
B1	D0:2	AD[34]	A89
A3	D0:1	AD[33]	B90
A1	D0:0	AD[32]	A91

Probe Connection D0/D1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	Q0-	GND	-----
A13	Q0+	SDONE	A40
B12	D3:7	AD[63]	B68
B10	D3:6	AD[62]	A68
A12	D3:5	AD[61]	B69
A10	D3:4	AD[60]	A70
B9	D3:3	AD[59]	B71
B7	D3:2	AD[58]	A71
A9	D3:1	AD[57]	B72
A7	D3:0	AD[56]	A73
B6	D2:7	AD[55]	B74
B4	D2:6	AD[54]	A74
A6	D2:5	AD[53]	B75
A4	D2:4	AD[52]	A76
B3	D2:3	AD[51]	B77
B1	D2:2	AD[50]	A77
A3	D2:1	AD[49]	B78
A1	D2:0	AD[48]	A79

Probe Connection D2/D3

Appendix G: NEX-PCI64HS P6960 D-Max Pinout

For further information on the P6960 probes please refer to the “P69xx Series High-Density Logic Analyzer Probes with D-Max Probing Technology Instruction Manual”, Tektronix part number 071-1528-02.

Connect NEX-M2P69X adapter to NEX-PCI64HS Mictor connection point “GROUP A”							
Pad	TLA Channel	PCI Signal Name	PCI Pin #	Pad	TLA Channel	PCI Signal Name	PCI Pin #
B20	Q0-	GND	-----	A8	CK0-	GND	-----
B21	Q0+	DEVSEL#	B37	A7	CK0+	CLK	B16
B14	D3:7	AD[15]	A44	A14	A3:7	AD[31]	B20
B15	D3:6	AD[14]	B45	A13	A3:6	AD[30]	A20
A16	D3:5	AD[13]	A46	B12	A3:5	AD[29]	B21
A17	D3:4	AD[12]	B47	B11	A3:4	AD[28]	A22
B17	D3:3	AD[11]	A47	A11	A3:3	AD[27]	B23
B18	D3:2	AD[10]	B48	A10	A3:2	AD[26]	A23
A19	D3:1	AD[09]	A49	B9	A3:1	AD[25]	B24
A20	D3:0	AD[08]	B52	B8	A3:0	AD[24]	A25
A22	D2:7	AD[07]	B53	B6	A2:7	AD[23]	B27
A23	D2:6	AD[06]	A54	B5	A2:6	AD[22]	A28
B23	D2:5	AD[05]	B55	A5	A2:5	AD[21]	B29
B24	D2:4	AD[04]	A55	A4	A2:4	AD[20]	A29
A25	D2:3	AD[03]	B56	B3	A2:3	AD[19]	B30
A26	D2:2	AD[02]	A57	B2	A2:2	AD[18]	A31
B26	D2:1	AD[01]	A58	A2	A2:1	AD[17]	B32
B27	D2:0	AD[00]	B58	A1	A2:0	AD[16]	A32

Probe Connection D2/D3

Probe Connection A2/A3

Connect NEX-M2P69X adapter to NEX-PCI64HS Mictor connection point "GROUP C"							
Pad	TLA Channel	PCI Signal Name	PCI Pin #	Pad	TLA Channel	PCI Signal Name	PCI Pin #
B20	Q1-	GND	-----	A1	CK3-	GND	-----
B21	Q1+	Do not use	DNU	A7	CK3+	RST#	A15
B14	C1:7	Unused	-----	A14	C3:7	C/BE[7]#	A64
B15	C1:6	M66EN	B49	A13	C3:6	C/BE[6]#	B65
A16	C1:5	REQ64#	A60	B12	C3:5	C/BE[5]#	A65
A17	C1:4	PAR64	A67	B11	C3:4	C/BE[4]#	B66
B17	C1:3	Unused	-----	A11	C3:3	C/BE[3]#	B26
B18	C1:2	Unused	-----	A10	C3:2	C/BE[2]#	B33
A19	C1:1	Unused	-----	B9	C3:1	C/BE[1]#	B44
A20	C1:0	Unused	-----	B8	C3:0	C/BE[0]#	A52
A22	C0:7	ACQ64#	B60	B6	C2:7	SBO#	A41
A23	C0:6	GNT#	A17	B5	C2:6	LOCK#	B39
B23	C0:5	REQ#	B18	A5	C2:5	PERR#	B40
B24	C0:4	IDSEL	A26	A4	C2:4	PAR	A43
A25	C0:3	INTD#	B08	B3	C2:3	STOP#	A38
A26	C0:2	INTC#	A07	A1	C2:2	TRDY#	A36
B26	C0:1	INTB#	B07	A7	C2:1	IRDY#	B35
B27	C0:0	INTA#	A06	A14	C2:0	FRAME#	A34

Probe Connection C0/C1

Probe Connection C2/C3

Connect NEX-M2P69X adapter to NEX-PCI64HS Mictor connection point "GROUP D"							
Pad	TLA Channel	PCI Signal Name	PCI Pin #	Pad	TLA Channel	PCI Signal Name	PCI Pin #
B20	CK2-	GND	-----	A8	CK1-	GND	-----
B21	CK2+	SERR#	B42	A7	CK1+	SDONE	A40
B14	D1:7	AD[47]	B80	A14	A1:7	AD[63]	B68
B15	D1:6	AD[46]	A80	A13	A1:6	AD[62]	A68
A16	D1:5	AD[45]	B81	B12	A1:5	AD[61]	B69
A17	D1:4	AD[44]	A82	B11	A1:4	AD[60]	A70
B17	D1:3	AD[43]	B83	A11	A1:3	AD[59]	B71
B18	D1:2	AD[42]	A83	A10	A1:2	AD[58]	A71
A19	D1:1	AD[41]	B84	B9	A1:1	AD[57]	B72
A20	D1:0	AD[40]	A85	B8	A1:0	AD[56]	A73
A22	D0:7	AD[39]	B86	B6	A0:7	AD[55]	B74
A23	D0:6	AD[38]	A86	B5	A0:6	AD[54]	A74
B23	D0:5	AD[37]	B87	A5	A0:5	AD[53]	B75
B24	D0:4	AD[36]	A88	A4	A0:4	AD[52]	A76
A25	D0:3	AD[35]	B89	B3	A0:3	AD[51]	B77
A26	D0:2	AD[34]	A89	B2	A0:2	AD[50]	A77
B26	D0:1	AD[33]	B90	A2	A0:1	AD[49]	B78
B27	D0:0	AD[32]	A91	A1	A0:0	AD[48]	A79

Probe Connection D0/D1

Probe Connection A0/A1

Appendix H: References

Tektronix TLA700 System User's Manual

Tektronix TLA700 Module User's Manual

P6434 Mass Termination Probe Instruction Manual
Tektronix part number 070-9793-04

P68xx Series Logic Analyzer Probes Instruction Manual
Tektronix part number 071-1059-04

P69xx Series High-Density Logic Analyzer Probes with D-Max Probing Technology
Instruction Manual
Tektronix part number 071-1528-02

PCI Local Bus Specification

Production Version; Revision 2.1s - June 1, 1995

Published by:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
800-433-5177 (U.S.)
503-797-4207 (International)
503-234-6762 (FAX)

PCI System Architecture

Third Edition

Mindshare, Inc. (Tom Shanley / Don Anderson)

Published by Addison Wesley

ISBN 0-201-40993-3

Appendix I: Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.