



NEX-PCIINTR_x

PCI Bus Adapter Users Manual

Including these Software Support packages:
PCIINT32 PCIINT64

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1.0 OVERVIEW

1.1 General Information

The NEX-PCIINTR adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA700 acquisition module to a 32 or 64-bit PCI backplane. (The PCI designation refers to the Peripheral Component Interconnect Local Bus specification.) Connections are made through four (4) Tektronix P6960 probes. The P6960 probes are available from Tektronix.

Two different NEX-PCIINTR cards are available. One supports a +5V target (NEX-PCIINTR5); the other supports a +3.3V target (NEX-PCIINTR3). Each card has its edge connector keyed for the specific voltage support, and cannot be plugged into a wrong slot. Two different boards were necessary to prevent damage that might be caused by accidentally plugging a +3.3V target into a +5V slot.

The included NEX-PCIINT64 and NEX-PCIINT32 software permits the acquisition of all PCI bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. For instance, references to the TLA700 apply to a TLA7xxx chassis with one or more 7Ax4 acquisition cards.

Appendix D is a silk-screen print of the NEX-PCIINTR Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the PCI Local Bus specification and the Tektronix TLA700 Logic Analyzer. Also, in the case of the TLA700, it is expected that the user is familiar with Windows.

Please see Appendix F for contact information.

2.0 SOFTWARE INSTALLATION

One CD has been included with the NEX-PCIINTR Bus Adapter. This CD includes both control software and this manual you are reading.

The PCIINT64 or PCIINT32 software is loaded in the same method as other Windows programs. Place the Install CD in the CD drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the CD and install the PCIINT64 or PCIINT32 support in its proper place on the hard disk.

To load PCIINT64 or PCIINT32 support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose PCIINT64 or PCIINT32 and click on **Okay**.

2.1 TLA700

The NEX-PCIINT64 / NEX-PCIINT32 software is loaded in the same method as other Windows programs. Place the appropriate Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the PCIINT64 or PCIINT32 support in its proper place on the hard disk.

To load PCIINT64 or PCIINT32 support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose PCIINT64 or PCIINT32 and click on **Okay**.

3.0 CONFIGURING the NEX-PCIINTR BUS ADAPTER

3.1 General Information

Use the supplied jumper to short (jumper across pins 2-3) or break (Jumper across pins 1-2) the connection between TDI and TDO (J8). If the target card does not support JTAG Boundary Scan then the two pins should be shorted together.

4.0 CONNECTING to the NEX-PCIINTR ADAPTER

4.1 General

The NEX-PCIINTR is an extender card that is also designed to permit monitoring the PCI bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will violate the PCI specification for stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, series resistors have been added to each signal to isolate the effect of the stub running to the TLA connection pads. The design also features a controlled impedance and matched trace length layout.

4.2 TLA Connections

To use a TLA700 with the NEX-PCIINTR adapter board it is necessary to use the P6960 high-density probes for connecting to the board. Connect the probe heads of the P6960 as shown on the silk screen of the NEX-PCIINTR adapter. Table 1 shows the wiring and Channel Grouping for the 136-channel TLA700 NEX-PCIINTR connections.

4.3 CONNECTING P6960 PROBES to the NEX-PCIINTR ADAPTER

IMPORTANT!

The PCIINTR adapter has four points where P6960 probes are attached. Care should be used when attaching these probes to make sure the attached probes are not pulled away from the NEX-PCIINTR module. After attaching the four P6960 probes the included Velcro strip must be attached to limit the possibility of damaging the adapter or P6960 probes by pulling the attached probes away from the adapter board. Figure 1 is a photo of the PCIINTR adapter with P6960 probes and the Velcro attached. Please note that you do not want to pull the Velcro as tightly as possible since this will pull the probes into the adapter. The Velcro is intended to keep the probes from being pulled away from the adapter and should be installed as shown in Figure 2. It is highly recommended that the user also strain reliefs the P6960 probes so the probes do not put stress on the adapter.

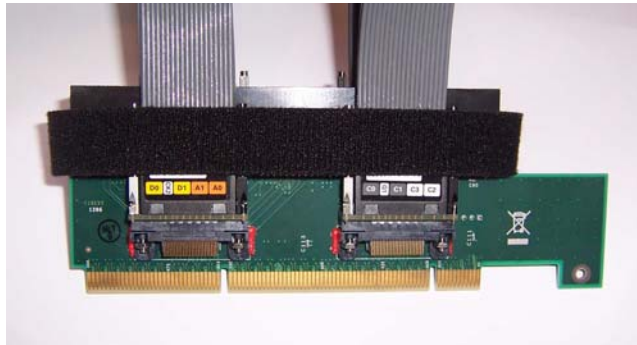


Figure 1- Velcro attached after the P6960 probes are attached



Figure 2- Top view of PCIINTR module with P6960 probes connected and velcro attached
Note the probes are not pulled in toward the PCIINTR module.

Group Name	Signal Name	PCI Pin #	TLA700 Input	Group Name	Signal Name	PCI Pin #	TLA700 input
AD_Hi (Hex)	AD[63]	B68	E1:7	AD_Lo (Hex)	AD[31]	B20	A3:3
	AD[62]	A68	A1:7		AD[30]	A20	A3:4
	AD[61]	B69	E3:7		AD[29]	B21	A3:6
	AD[60]	A70	D1:7		AD[28]	A22	A3:5
	AD[59]	B71	E3:5		AD[27]	B23	D3:7
	AD[58]	A71	D1:5		AD[26]	A23	A3:7
	AD[57]	B72	E3:6		AD[25]	B24	D3:5
	AD[56]	A73	D1:6		AD[24]	A25	D3:6
	AD[55]	B74	E3:4		AD[23]	B27	D3:4
	AD[54]	A74	D1:4		AD[22]	A28	D3:2
	AD[53]	B75	E3:3		AD[21]	B29	D3:1
	AD[52]	A76	D1:3		AD[20]	A29	D2:5
	AD[51]	B77	E3:1		AD[19]	B30	D2:6
	AD[50]	A77	D1:1		AD[18]	A31	D2:4
	AD[49]	B78	E3:2		AD[17]	B32	D2:1
	AD[48]	A79	D1:2		AD[16]	A32	D2:3
	AD[47]	B80	E2:7		AD[15]	A44	A0:2
	AD[46]	A80	D0:5		AD[14]	B45	E0:1
	AD[45]	B81	E2:5		AD[13]	A46	A0:1
	AD[44]	A82	D0:7		AD[12]	B47	E0:3
	AD[43]	B83	E2:6		AD[11]	A47	A0:3
	AD[42]	A83	D0:4		AD[10]	B48	E0:4
	AD[41]	B84	E2:4		AD[9]	A49	A0:6
	AD[40]	A85	D0:6		AD[8]	B52	E0:5
	AD[39]	B86	E2:3		AD[7]	B53	E0:7
	AD[38]	A86	D0:1		AD[6]	A54	A0:5
	AD[37]	B87	E2:1		AD[5]	B55	E1:0
	AD[36]	A88	D0:3		AD[4]	A55	A0:7
	AD[35]	B89	E2:2		AD[3]	B56	E1:1
	AD[34]	A89	D0:2		AD[2]	A57	A1:2
	AD[33]	B90	E2:0		AD[1]	B58	E1:3
	AD[32]	A91	D0:0		AD[0]	A58	A1:1

Table 1- NEX-PCIINTR TLA Channel Grouping

Note: All signals listed above are required for proper disassembly

Group Name	Signal Name	PCI Pin #	TLA700 Input	Group Name	Signal Name	PCI Pin #	TLA700 input
Control (Sym)	RST#	A15	+ Q1	Intrpt (Off)	INTD#	B08	C0:3
	REQ64#/ECC[6]	A60	A1:3		INTC#	A07	C0:1
	ACK64#/ECC[1]	B60	E1:4		INTB#	B07	C0:2
	FRAME#	A34	+ Clock:3		INTA#	A06	C0:0
	DEVSEL#	B37	C2:2	Misc (Off)	REQ#	B18	C1:0
	STOP#	A38	C2:0		GNT#	A17	C1:2
	IRDY#	B35	C2:3		LOCK#	B39	C3:1
	TRDY#	A36	C2:1		IDSEL	A26	C3:4
	C/BE#[7]	A64	A1:4		PERR#	B40	C3:2
	C/BE#[6]	B65	E1:6		PAR/ECC[0]	A43	A0:0
	C/BE#[5]	A65	A1:6	SERR#	B42	C2:5	
	C/BE#[4]	B66	E1:5	CLK	B16	+ Clock:0	
	C/BE#[3]	B26	D3:3	Ungrouped	PAR64/ECC[7]	A67	A1:5
	C/BE#[2]	B33	D2:2		M66EN	B49	E0:6
	C/BE#[1]	B44	E0:2		SMBCLK	A40	C3:0
	C/BE#[0]	A52	A0:4		RST#	A15	+Q1
			SMBDAT		A41	C2:7	
			TDO		B4	Not connected	
			TRST#		A1	Not connected	
			TMS		A3	Not connected	
			TDI		A4	Not connected	
			TCK		B2	Not connected	
			ECC[5]		A9	A2:5	
			ECC[4]		B10	A2:7	
			ECC[3]		A11	A3:0	
			ECC[2]		B14	A3:2	
			PRSENT1#		B9	C0:5	
			PRSENT2#		B11	C1:0	
			PME#	A19	C1:3		
			Reserved B63	B63	Not connected		
			Reserved B92	B92	Not connected		
			Reserved A94	A94	Not connected		
			Reserved A92	A92	Not connected		
			Reserved B93	B93	Not connected		
			MODE2	B50	Not connected		

Table 1- NEX-PCIINTR TLA Channel Grouping (cont'd.)

Note: Signals with a '+' are required for proper clocking / disassembly

5.0 CLOCK SELECTION

5.1 General Information

There are three clocking options available when using either the NEX-PCIINT64 or NEX-PCIINT32 support package. Each selection is explained in detail below.

When using a TLA700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.2 Clocking Options - Explanation

Bus Cycle Acquisition - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable (32-bit only) - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge - In this mode, data will be acquired on every rising edge of the PCI CLK signal. The disassembly will filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

6.0 VIEWING DATA

6.1 Viewing Timing Data on the TLA700

By default, the TLA700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PCIINT64 and PCIINT64-MagniVu (or PCIINT32 and PCIINT32-MagniVu when using 32-bit support). The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PCIINT64-MagniVu (or PCIINT32-MagniVu), will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA700 System User's Manual for additional information on formatting the Waveform display.

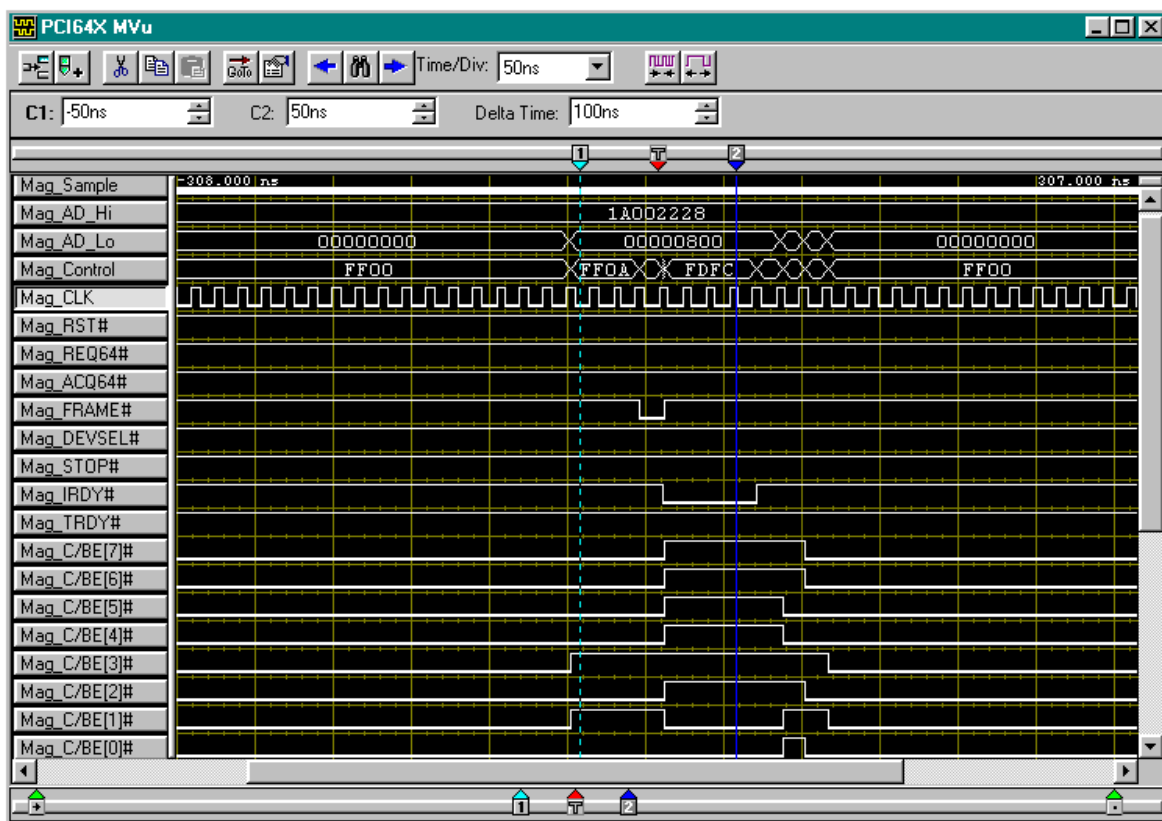


Figure 3- PCIINT64 MagniVu Display on TLA700

Pattern	TLA700 Symbols	Meaning
0xxxxxxxxxxxxx	RESET	Reset
11x01111xxxx0000	INTERRUPT ACK	Interrupt Acknowledge
11x01111xxxx0001	SPECIAL CYCLE	Special Cycle
11x01111xxxx0010	I/O READ ADDR	I/O Read Address
11x01111xxxx0011	I/O WRITE ADDR	I/O Write Address
1xx01111xxxx010x	RESERVED	Reserved
11x01111xxxx0110	MEMORY RD DWORD ADDR	Memory Read DWORD Address
1xx01111xxxx0111	MEMORY WR ADDR	Memory Write Address
1xx01111xxxx1000	ALIAS TO MEM RD BLK	Alias to Memory Read Block
1xx01111xxxx1001	ALIAS TO MEM WRT BLK	Alias to Memory Write Block
11x01111xxxx1010	CONFIG READ ADDR	Configuration Read Address
11x01111xxxx1011	CONFIG WRITE ADDRESS	Configuration Write Address
1xx01111xxxx1100	SPLIT COMPLETION	Split Completion
1xx01111xxxx1101	DUAL ADDR	Dual Address Cycle
1xx01111xxxx1110	MEMORY READ BLOCK	Memory Read Block
1xx01111xxxx1111	MEMORY WRITE BLOCK	Memory Write Block
1xx11101xxxxxxxxx	WAIT/MASTER ABORT	Wait or Master Abort
1xx11001xxxxxxxxx	TARGET ABORT	Target Abort
1xx10001xxxxxxxxx	RETRY	Retry Cycle
111x0x0011111110	BYTE 0	Byte 0 valid (D0-7)
111x0x0011111101	BYTE 1	Byte 1 valid (D8-15)
111x0x0011111011	BYTE 2	Byte 2 valid (D16-23)
111x0x0011110111	BYTE 3	Byte 3 valid (D24-31)
111x0x0011101111	BYTE 4	Byte 4 valid (D32-39)
111x0x0011011111	BYTE 5	Byte 5 valid (D40-47)
111x0x0010111111	BYTE 6	Byte 6 valid (D48-55)
111x0x0001111111	BYTE 7	Byte 7 valid (D56-63)
111x0x0011111100	BYTES 0,1	Bytes 0 & 1 valid (D0-15)
111x0x0011110011	BYTES 2,3	Bytes 2 & 3 valid (D16-31)
111x0x0011001111	BYTES 4,5	Bytes 4 & 5 valid (D32-47)
111x0x0000111111	BYTES 6,7	Bytes 6 & 7 valid (D48-63)
111x0x0011110000	BYTES 0-3	Bytes 0-3 valid (D0-31)
111x0x0000001111	BYTES 4-7	Bytes 4-7 valid (D32-63)
100x0x0000000000	BYTES 0-7	Bytes 0-3 valid (D0-63)
111x0x00xxxx0000	LOW 32-BITS	Low 32-bits valid
1xxx0x0011111111	INVALID DATA	Invalid Data
1xxx00x0xxxxxxxxx	DISC AT NEX ADB	Disconnect at next ADB
1xxx10x0xxxxxxxxx	SNGL DATA PHASE DISC	Single Data Phase Disconnect
1xx1xxxxxxxxxxxxx	FRAME HI	Frame Hi
1xx0xxxxxxxxxxxxx	FRAME LO	Frame Lo

Table 2- PCIINT64_Ctrl Control Symbol Table

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

7.0 USING the DISASSEMBLY SOFTWARE

7.1 General

The PCIINT64 and PCIINT32 support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the PCIINT64 and PCIINT32 software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the PCIINT64 / PCIINT32 software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps in the TLA700 series, permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Using the TLA700

The TLA700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window

Sample	PCI64X AD_Hi	PCI64X AD_Lo	PCI64X Mnemonics	Timestamp
	-----	FFFE0000	Memory Not Prefetchable	
	-----	FFFE0000	Decoder for 128KB Memory Space	
438	-----	04000010	CONFIG WRITE ADDRESS	6.904,570,000 ms
	-----	04000010	Type 0 Register 4 Function 0	
439	-----	00000000	CONFIG WRITE DATA	6.904,600,000 ms
	-----	00000000	Write to Base Address Register 0	
440	-----	04000008	CONFIG READ ADDRESS	6.908,491,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
441	-----	03000002	CONFIG READ DATA	6.908,536,500 ms
	-----	03000002	Class 0x03 - Display controller	
	-----	03000002	Sub-Class 0x00	
	-----	03000002	Prog. I/F 0x00 - VGA compatible	
	-----	03000002	Revision ID 2	
442	-----	04000010	CONFIG READ ADDRESS	6.937,764,500 ms
	-----	04000010	Type 0 Register 4 Function 0	
443	-----	-----00	CONFIG READ DATA	6.937,809,000 ms
	-----	-----00	Invalid Base Address data	
	-----	-----00	Base Address Register 0	
	-----	-----00	Memory Address Register	
	-----	-----00	Locate anywhere in 32-bit space	
	-----	-----00	Memory Not Prefetchable	
	-----	-----00	Decoder for 16 bytes Memory Space	
444	-----	04000008	CONFIG READ ADDRESS	6.941,296,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
445	-----	03000002	CONFIG READ DATA	6.941,341,500 ms

Figure 4- PCIINT64 Disassembly

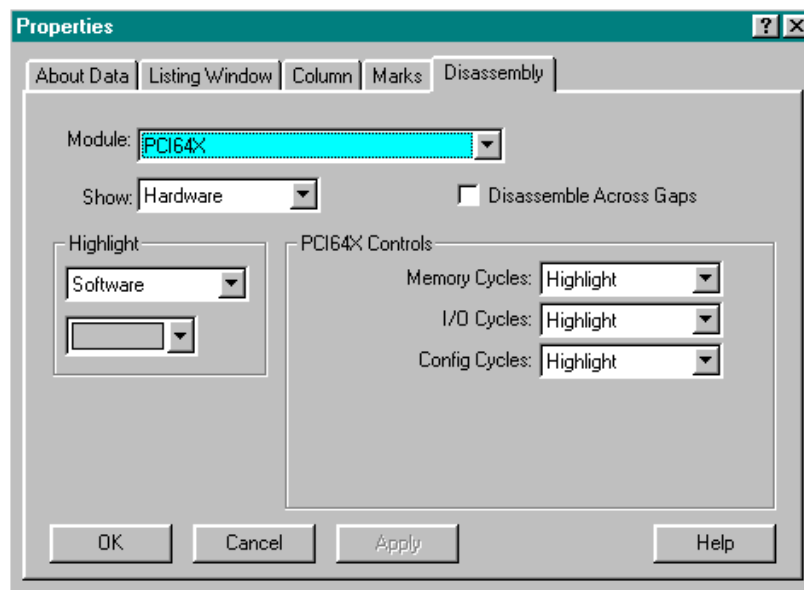


Figure 5- PCIINT64 Cycle Filtering Window

contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark (disabled in PCI64HS)

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PCIINT64 / PCIINT32 disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

APPENDIX A - Necessary Signals for Clocking

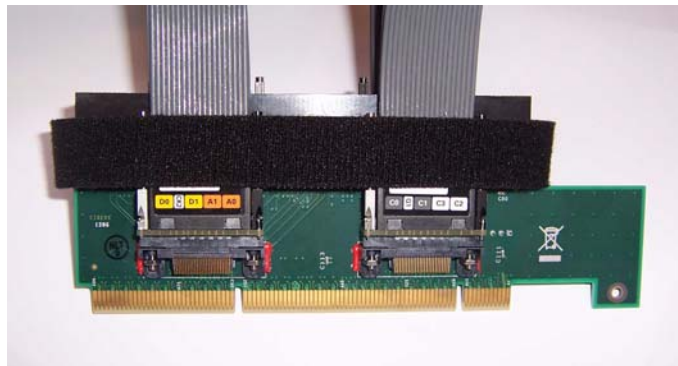
To properly acquire PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

APPENDIX B - Considerations

The NEX-PCIINTR is an extender card that is also designed to permit monitoring the PCI bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will violate the PCI specification for stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, series termination resistors have been added to each signal to reduce the electrical effect of the stub. The adapter design is also impedance controlled and matched trace length to maintain signal integrity

IMPORTANT – CONNECTING P6960 PROBES to the NEX-PCIINTR ADAPTER

The PCIINTR adapter has four points where P6960 probes are attached. Care should be used when attaching these probes to make sure the attached probes are not pulled away from the NEX-PCIINTR module. After attaching the four P6960 probes the included Velcro strip must be attached to limit the possibility of damaging the adapter or P6960 probes by pulling the attached probes away from the adapter board. Figure 1 is a photo of the PCIINTR adapter with P6960 probes and the Velcro attached. Please note that you do not want to pull the Velcro as tightly as possible since this will pull the probes into the adapter. The Velcro is intended to keep the probes from being pulled away from the adapter and should be installed as shown in Figure 2. It is highly recommended that the user also strain reliefs the P6960 probes so the probes do not put stress on the adapter.



Velcro attached after the P6960 probes are attached



Top view of PCIINTR module with P6960 probes connected and Velcro attached.
Note the probes are not pulled in toward the PCIINTR module.

APPENDIX C - PCI Local Bus Pinout

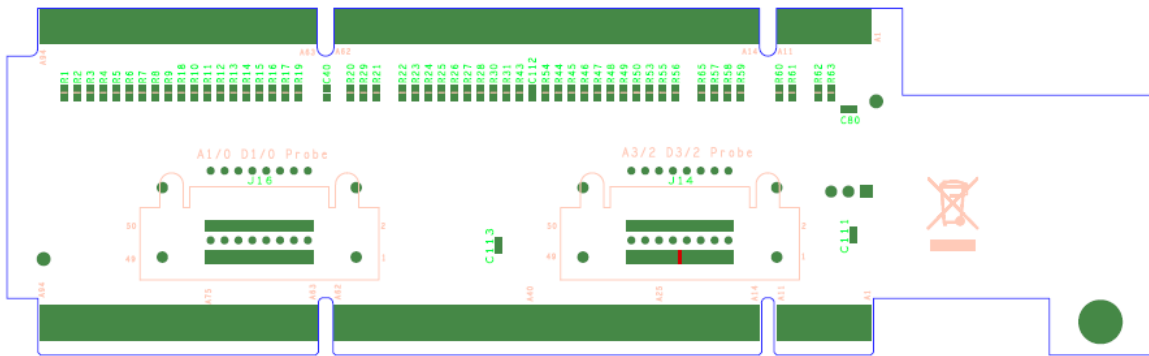
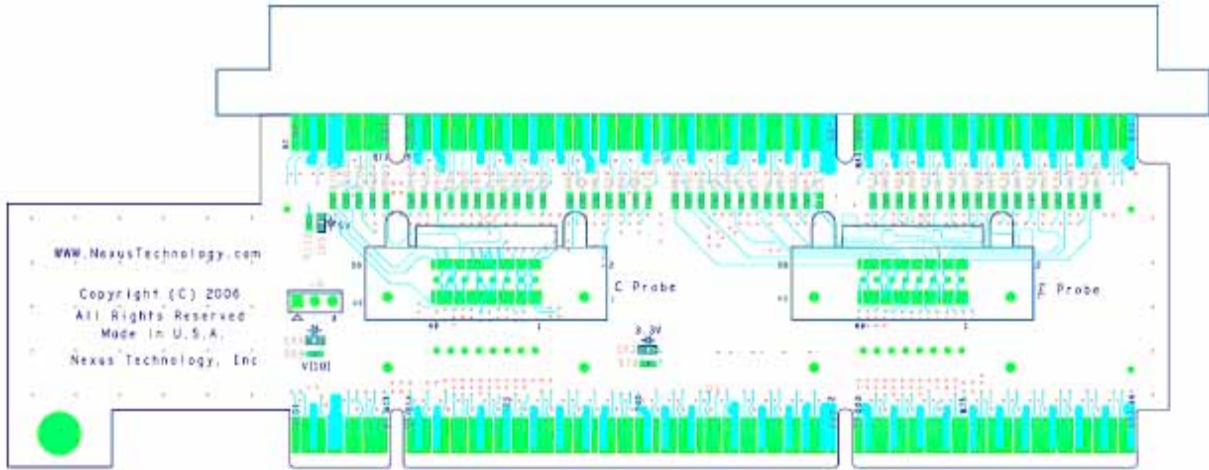
Information given here is for the +5V and +3.3V PCI Board definitions:

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
1	-12V	TRST#	-12V	TRST#	32-bit start
2	TCK	+12V	TCK	+12V	
3	Ground	TMS	Ground	TMS	
4	TDO	TDI	TDO	TDI	
5	+5V	+5V	+5V	+5V	
6	+5V	INTA#	+5V	INTA#	
7	INTB#	INTC#	INTB#	INTC#	
8	INTD#	+5V	INTD#	+5V	
9	PRSENT1#	Reserved	PRSENT1#	Reserved	
10	Reserved	+5V	Reserved	+3.3V	
11	PRSENT2#	Reserved	PRSENT2#	Reserved	
12	Ground	Ground	KEYWAY	KEYWAY	3.3V key
13	Ground	Ground	KEYWAY	KEYWAY	
14	Reserved	Reserved	Reserved	Reserved	
15	Ground	RST#	Ground	RST#	
16	CLK	+5V	CLK	+3.3V	
17	Ground	GNT#	Ground	GNT#	
18	REQ#	Ground	REQ#	Ground	
19	+V I/O	Reserved	+V I/O	Reserved	
20	AD[31]	AD[30]	AD[31]	AD[30]	
21	AD[29]	+3.3V	AD[29]	+3.3V	
22	Ground	AD[28]	Ground	AD[28]	
23	AD[27]	AD[26]	AD[27]	AD[26]	
24	AD[25]	Ground	AD[25]	Ground	
25	+3.3V	AD[24]	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	AD[23]	+3.3V	
28	Ground	AD[22]	Ground	AD[22]	
29	AD[21]	AD[20]	AD[21]	AD[20]	
30	AD[19]	Ground	AD[19]	Ground	
31	+3.3V	AD[18]	+3.3V	AD[18]	
32	AD[17]	AD[16]	AD[17]	AD[16]	

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
33	C/BE[2]#	+3.3V	C/BE[2]#	+3.3V	
34	Ground	FRAME#	Ground	FRAME#	
35	IRDY#	Ground	IRDY#	Ground	
36	+3.3V	TRDY#	+3.3V	TRDY#	
37	DEVSEL#	Ground	DEVSEL#	Ground	
38	Ground	STOP#	Ground	STOP#	
39	LOCK#	+3.3V	LOCK#	+3.3V	
40	PERR#	SDONE	PERR#	SDONE	
41	+3.3V	SBO#	+3.3V	SBO#	
42	SERR#	Ground	SERR#	Ground	
43	+3.3V	PAR	+3.3V	PAR	
44	C/BE[1]#	AD[15]	C/BE[1]#	AD[15]	
45	AD[14]	+3.3V	AD[14]	+3.3V	
46	Ground	AD[13]	Ground	AD[13]	
47	AD[12]	AD[11]	AD[12]	AD[11]	
48	AD[10]	Ground	AD[10]	Ground	
49	Ground	AD[9]	M66EN	AD[9]	
50	KEYWAY	KEYWAY	Ground	Ground	5V key
51	KEYWAY	KEYWAY	Ground	Ground	5V key
52	AD[8]	C/BE[0]#	AD[8]	C/BE[0]#	
53	AD[7]	+3.3V	AD[7]	+3.3V	
54	+3.3V	AD[6]	+3.3V	AD[6]	
55	AD[5]	AD[4]	AD[5]	AD[4]	
56	AD[3]	Ground	AD[3]	Ground	
57	Ground	AD[2]	Ground	AD[2]	
58	AD[1]	AD[0]	AD[1]	AD[0]	
59	+5V	+5V	+3.3V	+3.3V	
60	ACK64#	REQ64#	ACK64#	REQ64#	
61	+5V	+5V	+5V	+5V	
62	+5V	+5V	+5V	+5V	32-bit end

Pin #	+5V Side B Component Side	+5V Side A Solder Side	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
	KEYWAY	KEYWAY	KEYWAY	KEYWAY	64-bit spacer
	KEYWAY	KEYWAY	KEYWAY	KEYWAY	64-bit spacer
63	Reserved	Ground	Reserved	Ground	
64	Ground	C/BE[7]#	Ground	C/BE[7]#	
65	C/BE[6]#	C/BE[5]#	C/BE[6]#	C/BE[5]#	
66	C/BE[4]#	+5V	C/BE[4]#	+3.3V	
67	Ground	PAR64	Ground	PAR64	
68	AD[63]	AD[62]	AD[63]	AD[62]	
69	AD[61]	Ground	AD[61]	Ground	
70	+5V	AD[60]	+3.3V	AD[60]	
71	AD[59]	AD[58]	AD[59]	AD[58]	
72	AD[57]	Ground	AD[57]	Ground	
73	Ground	AD[56]	Ground	AD[56]	
74	AD[55]	AD[54]	AD[55]	AD[54]	
75	AD[53]	+5V	AD[53]	+3.3V	
76	Ground	AD[52]	Ground	AD[52]	
77	AD[51]	AD[50]	AD[51]	AD[50]	
78	AD[49]	Ground	AD[49]	Ground	
79	+5V	AD[48]	+3.3V	AD[48]	
80	AD[47]	AD[46]	AD[47]	AD[46]	
81	AD[45]	Ground	AD[45]	Ground	
82	Ground	AD[44]	Ground	AD[44]	
83	AD[43]	AD[42]	AD[43]	AD[42]	
84	AD[41]	+5V	AD[41]	+3.3V	
85	Ground	AD[40]	Ground	AD[40]	
86	AD[39]	AD[38]	AD[39]	AD[38]	
87	AD[37]	Ground	AD[37]	Ground	
88	+5V	AD[36]	+3.3V	AD[36]	
89	AD[35]	AD[34]	AD[35]	AD[34]	
90	AD[33]	Ground	AD[33]	Ground	
91	Ground	AD[32]	Ground	AD[32]	
92	Reserved	Reserved	Reserved	Reserved	
93	Reserved	Ground	Reserved	Ground	
94	Ground	Reserved	Ground	Reserved	64-bit end

APPENDIX D - NEX-PCIINTR Silk Screen



APPENDIX E - NEX- PCIINTR P6960 Compression Pinouts

For further information on the P6960 Connectorless probe compression footprint please refer to the Tektronix “P69XX Series Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1528-02.

Pad #	Samtec pin	TLA Channel	PCI Signal
A8	30	Q3-	GND
A7	28	Q3+	
A14	52	E3:7	AD61
A13	46	E3:6	AD57
B12	45	E3:5	AD59
B11	39	E3:4	AD55
A11	40	E3:3	AD53
A10	34	E3:2	AD49
B9	33	E3:1	AD51
B8	27	E3:0	
B6	21	E2:7	AD47
B5	15	E2:6	AD43
A5	22	E2:5	AD45
A4	16	E2:4	AD41
B3	9	E2:3	AD39
B2	3	E2:2	AD35
A2	10	E2:1	AD37
A1	4	E2:0	AD33

Probe Connection – E

Pad #	Samtec pin	TLA Channel	PCI Signal
B20	75	Q2-	GND
B21	77	Q2+	
B14	51	E1:7	AD63
B15	57	E1:6	C/BE6#
A16	58	E1:5	C/BE4# ACK64# /
A17	64	E1:4	ECC[1]
B17	63	E1:3	AD1
B18	69	E1:2	AD5
A19	70	E1:1	AD3
A20	76	E1:0	
A22	80	E0:7	AD7
A23	86	E0:6	M66EN
B23	81	E0:5	AD8
B24	85	E0:4	AD10
A25	92	E0:3	AD12
A26	98	E0:2	C/BE1#
B26	91	E0:1	AD14
B27	97	E0:0	

Probe Connection – E

Pad #	Samtec pin	TLA Channel	PCI Signal
A8	30	CK0-	GND
A7	28	CK0+	CLK
A14	52	A3:7	AD26
A13	46	A3:6	AD29
B12	45	A3:5	AD28
B11	39	A3:4	AD30
A11	40	A3:3	AD31
A10	34	A3:2	ECC[2]
B9	33	A3:1	
B8	27	A3:0	ECC[3]
B6	21	A2:7	ECC[4]
B5	15	A2:6	
A5	22	A2:5	ECC[5]
A4	16	A2:4	
B3	9	A2:3	
B2	3	A2:2	
A2	10	A2:1	
A1	4	A2:0	

Probe Connection – A3/2-D3/2

Pad #	Samtec pin	TLA Channel	PCI Signal
B20	75	Q0-	GND
B21	77	Q0+	GND
B14	51	D3:7	AD27
B15	57	D3:6	AD24
A16	58	D3:5	AD25
A17	64	D3:4	AD23
B17	63	D3:3	C/BE3#
B18	69	D3:2	AD22
A19	70	D3:1	AD21
A20	76	D3:0	
A22	80	D2:7	
A23	86	D2:6	AD19
B23	81	D2:5	AD20
B24	85	D2:4	AD18
A25	92	D2:3	AD16
A26	98	D2:2	C/BE2#
B26	91	D2:1	AD17
B27	97	D2:0	

Probe Connection – A3/2-D3/2

APPENDIX E - NEX-PCIINTR P6960 Compression Pinouts (cont'd.)

Pad #	Samtec pin	TLA Channel	PCI Signal
A8	30	CK1-	GND
A7	28	CK1+	GND
A14	52	A1:7	AD62
A13	46	A1:6	C/BE5# PAR64 /
B12	45	A1:5	ECC[7]
B11	39	A1:4	C/BE7# REQ64# /
A11	40	A1:3	ECC[6]
A10	34	A1:2	AD2
B9	33	A1:1	AD0
B8	27	A1:0	
B6	21	A0:7	AD4
B5	15	A0:6	AD9
A5	22	A0:5	AD6
A4	16	A0:4	C/BE0#
B3	9	A0:3	AD11
B2	3	A0:2	AD15
A2	10	A0:1	AD13 PAR /
A1	4	A0:0	ECC[0]

Probe Connection – A1/0-D1/0

Pad #	Samtec pin	TLA Channel	PCI Signal
B20	75	CK2-	GND
B21	77	CK2+	GND
B14	51	D1:7	AD60
B15	57	D1:6	AD56
A16	58	D1:5	AD58
A17	64	D1:4	AD54
B17	63	D1:3	AD52
B18	69	D1:2	AD48
A19	70	D1:1	AD50
A20	76	D1:0	
A22	80	D0:7	AD44
A23	86	D0:6	AD40
B23	81	D0:5	AD46
B24	85	D0:4	AD42
A25	92	D0:3	AD36
A26	98	D0:2	AD34
B26	91	D0:1	AD38
B27	97	D0:0	AD32

Probe Connection – A1/0-D1/0

Pad #	Samtec pin	TLA Channel	PCI Signal
A8	30	CK3-	GND
A7	28	CK3+	FRAME#
A14	52	C3:7	
A13	46	C3:6	
B12	45	C3:5	
B11	39	C3:4	IDSEL
A11	40	C3:3	
A10	34	C3:2	PERR#
B9	33	C3:1	LOCK#
B8	27	C3:0	SMBCLK
B6	21	C2:7	SMBDAT
B5	15	C2:6	
A5	22	C2:5	SERR#
A4	16	C2:4	
B3	9	C2:3	IRDY#
B2	3	C2:2	DEVSEL#
A2	10	C2:1	TRDY#
A1	4	C2:0	STOP#

Probe Connection – C

Pad #	Samtec pin	TLA Channel	PCI Signal
B20	75	Q1-	GND
B21	77	Q1+	RST#
B14	51	C1:7	
B15	57	C1:6	
A16	58	C1:5	
A17	64	C1:4	
B17	63	C1:3	PME#
B18	69	C1:2	GNT#
A19	70	C1:1	REQ#
A20	76	C1:0	PRSNT2#
A22	80	C0:7	
A23	86	C0:6	
B23	81	C0:5	PRSNT1#
B24	85	C0:4	
A25	92	C0:3	INTD#
A26	98	C0:2	INTB#
B26	91	C0:1	INTC#
B27	97	C0:0	INTA#

Probe Connection – C

APPENDIX F - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX G - References

Tektronix TLA700 System User's Manual

Tektronix TLA700 Module User's Manual

P69XX Series Logic Analyzer Probes Instruction Manual
Tektronix part number 071-1528-02

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