



NEX-PCISWL

PCI Disassembly Software Users Manual

Including these Software Support packages:

PCI32L PCI32L68 PCI64L

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1.0 OVERVIEW

1.1 General Information

This manual covers the NEX-PCI32SWL 32-bit and NEX-PCI3264SWL 64-bit PCI Bus Support software packages. Please disregard all references to 64-bit PCI if only 32-bit PCI is needed.

The PCI32SWL and PCI3264SWL analysis software provides acquisition of all 32- and 64-bit PCI bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. For instance, references to a TLA apply to a TLA704, TLA711, TLA714, TLA720 or TLA600 series Logic Analyzer. Also, references to PCI32 support apply to both the PCI32L (102/136-channel support) and PCI32L68 (68-channel support) unless otherwise indicated.

This manual assumes that the user is familiar with the PCI Local Bus specification and the Tektronix TLA600/700 Logic Analyzer. Also, it is expected that the user is familiar with Windows 95, 98 or 2000 depending on the operating system that the logic analyzer is running.

2.0 CONNECTING TO THE PCI BUS

2.1 Mictor Connector vs. Square Pins

Since the NEX-PCI32SWL and NEX-PCI3264SWL packages are software only it is up to the user to determine how to interface the Logic Analyzer to the PCI Bus. This connection can be accomplished in two ways: One is by designing Mictor connectors onto the target, the second method is via stake pins such as those found on a generic extender board / break-out adapter.

Designing Mictor connectors onto the target requires far less real estate and is a much easier and faster connection to make. Tektronix P6434 probes are then required to connect the TLA to these Mictor connectors. Two P6434 probes are required for 32-bit PCI support and three P6434 probes are required for 64-bit PCI support. Each P6434 probe consists of one high-density probe tip (which connects to the adapter board) and two module ends (which connect to the acquisition card). It is important to note that where the module ends connect to the acquisition card will depend on how many channels the acquisition card has. Be very careful in noting where Pin 1 is on each probe tip, and follow the P6434 Mass Termination Probe manual for instructions on applying the labels. For complete mechanical pinout information of the Mictor connector (i.e. the location of pin 1 and how the count sequence is defined around the Mictor connector) please refer to the Tektronix P6434 Mass Termination Probe Instruction Manual. A link to this document is available on our web site (<http://www.busboards.com>) in the “Available Literature” section.

Square pins (0.25” square on 0.1” centers) require more physical space than Mictors, but can be easier to route to than Mictors, and also provide easy connection points for use with other test equipment such as oscilloscopes. Tektronix P6417 or P6418 probes are used to connect the TLA to square pins, and the included flying leadsets may also be necessary. Refer to the Tektronix P6417 & P6418 Logic Analyzer Probes manual for further information.

All probes must be purchased directly from Tektronix – none are included with the NEX-PCI32SWL or NEX-PCI3264SWL products.

2.2 32-bit PCI TLA 102-/136-channel P6434 Mictor Connections

When using a 102- or 136-channel TLA for 32-bit PCI support, the necessary acquisition data sections are A0-A3 and C0-C3. One P6434 plugs onto the Group A Mictor connector designed onto the target and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434 plugs onto the Group C Mictor connector on the target and connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. Table 1 shows the wiring and Channel Grouping for the 32-bit 102/136-channel TLA connection.

2.3 32-bit PCI TLA 68-channel P6434 Mictor Connections

When using a 68-channel TLA for 32-bit PCI support different software and wiring is necessary. Table 2 shows the wiring and Channel Grouping for the TLA when used with the PCI32L68 software. When using Mictors the wiring for the Group C connector is the same for 68-channel use as it is for 102- and 136-channel support but connecting the P6434 cables to the TLA is different. The necessary acquisition data sections are A0-A3, C2, C3, D1, and D0. One P6434 plugs onto the Group A Mictor connector on the target and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434 plugs onto the Group C Mictor connector and then the lower data channels connect to the Yellow (D0 and D1) locations and the higher data channels connect to the White (C2 and C3) locations on the acquisition card. Refer to the Tektronix P6434 Mass Termination Probe Instruction Manual for further information.

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
Addr_Dat (Hex)	AD[31]	B20	+ A3:7	Control (Sym)	RST#	A15	+ C3:5
	AD[30]	A20	+ A3:6		FRAME#	A34	+ C2:0
	AD[28]	A22	+ A3:4		DEVSEL#	B37	+ CLK1
	AD[27]	B23	+ A3:3		STOP#	A38	+ C2:3
	AD[26]	A23	+ A3:2		IRDY#	B35	+ C2:1
	AD[25]	B24	+ A3:1		TRDY#	A36	+ C2:2
	AD[24]	A25	+ A3:0		C/BE#[3]	B26	+ C2:7
	AD[23]	B27	+ A2:7	C/BE#[2]	B33	+ C2:6	
	AD[22]	A28	+ A2:6	C/BE#[1]	B44	+ C2:5	
	AD[21]	B29	+ A2:5	C/BE#[0]	A52	+ C2:4	
	AD[20]	A29	+ A2:4	Intrpt	INTD#	B08	C0:3
	AD[19]	B30	+ A2:3		INTC#	A07	C0:2
	AD[18]	A31	+ A2:2		INTB#	B07	C0:1
	AD[17]	B32	+ A2:1		INTA#	A06	C0:0
	AD[16]	A32	+ A2:0	Misc	REQ#	B18	C0:5
	AD[15]	A44	+ A1:7		GNT#	A17	C0:6
	AD[14]	B45	+ A1:6		LOCK#	B39	C3:4
	AD[13]	A46	+ A1:5		IDSEL	A26	C0:4
	AD[12]	B47	+ A1:4		PERR#	B40	C3:3
AD[11]	A47	+ A1:3	PAR		A43	C3:2	
AD[9]	A49	+ A1:1	SERR#		B42	C3:1	
AD[8]	B52	+ A1:0	CLK	B16	+ CLK3		
AD[7]	B53	+ A0:7	Ungroupe d	SDONE	A40	C3:6	
AD[6]	A54	+ A0:6		SBO#	A41	C1:3	
AD[5]	B55	+ A0:5		ACQ64#	B60	C1:1	
AD[4]	A55	+ A0:4		REQ64#	A60	C1:0	
AD[3]	B56	+ A0:3		M66EN	B49	C0:7	
AD[2]	A57	+ A0:2	Aux_1	Aux_1:[7-0]	-----	D3	
AD[1]	B58	+ A0:1	Aux_0	Aux_0:[7-0]	-----	D2	
AD[0]	A58	+ A0:0					

Table 1- PCI32L TLA 102-/136-channel Grouping

Note: Signals with a '+' are required for proper clocking / disassembly

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input
Addr_Dat (Hex)	AD[31]	B20	+ A3:7	Control (Sym)	RST#	A15	+ C3:5
	AD[30]	A20	+ A3:6		FRAME#	A34	+ C2:0
	AD[28]	A22	+ A3:4		DEVSEL#	B37	+ CLK1
	AD[27]	B23	+ A3:3		STOP#	A38	+ C2:3
	AD[26]	A23	+ A3:2		IRDY#	B35	+ C2:1
	AD[25]	B24	+ A3:1		TRDY#	A36	+ C2:2
	AD[24]	A25	+ A3:0		C/BE#[3]	B26	+ C2:7
	AD[23]	B27	+ A2:7		C/BE#[2]	B33	+ C2:6
	AD[22]	A28	+ A2:6		C/BE#[1]	B44	+ C2:5
	AD[21]	B29	+ A2:5		C/BE#[0]	A52	+ C2:4
	AD[20]	A29	+ A2:4	Intrpt	INTD#	B08	D0:3
	AD[19]	B30	+ A2:3		INTC#	A07	D0:2
	AD[18]	A31	+ A2:2		INTB#	B07	D0:1
	AD[17]	B32	+ A2:1		INTA#	A06	D0:0
	AD[16]	A32	+ A2:0	Misc	REQ#	B18	D0:5
	AD[15]	A44	+ A1:7		GNT#	A17	D0:6
	AD[14]	B45	+ A1:6		LOCK#	B39	C3:4
	AD[13]	A46	+ A1:5		IDSEL	A26	D0:4
	AD[12]	B47	+ A1:4		PERR#	B40	C3:3
	AD[11]	A47	+ A1:3		PAR	A43	C3:2
AD[9]	A49	+ A1:1	SERR#		B42	C3:1	
AD[8]	B52	+ A1:0	CLK	B16	+ CLK3		
AD[7]	B53	+ A0:7	Ungroupe d	SDONE	A40	C3:6	
AD[6]	A54	+ A0:6		SBO#	A41	D1:3	
AD[5]	B55	+ A0:5		ACQ64#	B60	D1:1	
AD[4]	A55	+ A0:4		REQ64#	A60	D1:0	
AD[3]	B56	+ A0:3		M66EN	B49	D0:7	
AD[2]	A57	+ A0:2					
AD[1]	B58	+ A0:1					
AD[0]	A58	+ A0:0					

Table 2- PCI32L68 TLA 68-channel Grouping

Note: Signals with a '+' are required for proper clocking / disassembly

2.4 64-bit PCI TLA 102-/136-channel P6434 Mictor Connections

When using a 102- or 136-channel TLA for 64-bit PCI support, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. One P6434 plugs onto the Group A Mictor connector on the target and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434 plugs onto the Group C Mictor connector connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. The third P6434 plugs onto the Group D Mictor connector and then connects to the Yellow (D0 and D1) and Blue (D2 and D3) locations on the acquisition card. Table 3 shows the wiring and Channel Grouping for the 102/136-channel TLA PCI64L software.

Group Name	Signal Name	PCI Pin #	TLA input	Group Name	Signal Name	PCI Pin #	TLA input	
AD_Hi (Hex)	AD[63]	B68	D3:7	AD_Lo (Hex)	AD[31]	B20	A3:7	
	AD[62]	A68	D3:6		AD[30]	A20	A3:6	
	AD[61]	B69	D3:5		AD[29]	B21	A3:5	
	AD[60]	A70	D3:4		AD[28]	A22	A3:4	
	AD[59]	B71	D3:3		AD[27]	B23	A3:3	
	AD[58]	A71	D3:2		AD[26]	A23	A3:2	
	AD[57]	B72	D3:1		AD[25]	B24	A3:1	
	AD[56]	A73	D3:0		AD[24]	A25	A3:0	
	AD[55]	B74	D2:7		AD[23]	B27	A2:7	
	AD[54]	A74	D2:6		AD[22]	A28	A2:6	
	AD[53]	B75	D2:5		AD[21]	B29	A2:5	
	AD[52]	A76	D2:4		AD[20]	A29	A2:4	
	AD[51]	B77	D2:3		AD[19]	B30	A2:3	
	AD[50]	A77	D2:2		AD[18]	A31	A2:2	
	AD[49]	B78	D2:1		AD[17]	B32	A2:1	
	AD[48]	A79	D2:0		AD[16]	A32	A2:0	
	AD[47]	B80	D1:7		AD[15]	A44	A1:7	
	AD[46]	A80	D1:6		AD[14]	B45	A1:6	
	AD[45]	B81	D1:5		AD[13]	A46	A1:5	
	AD[44]	A82	D1:4		AD[12]	B47	A1:4	
	AD[43]	B83	D1:3		AD[11]	A47	A1:3	
	AD[42]	A83	D1:2		AD[10]	B48	A1:2	
	AD[41]	B84	D1:1		AD[9]	A49	A1:1	
	AD[40]	A85	D1:0		AD[8]	B52	A1:0	
	AD[39]	B86	D0:7		AD[7]	B53	A0:7	
	AD[38]	A86	D0:6		AD[6]	A54	A0:6	
	AD[37]	B87	D0:5		AD[5]	B55	A0:5	
	AD[36]	A88	D0:4		AD[4]	A55	A0:4	
	AD[35]	B89	D0:3		AD[3]	B56	A0:3	
	AD[34]	A89	D0:2		AD[2]	A57	A0:2	
	AD[33]	B90	D0:1		AD[1]	B58	A0:1	
	AD[32]	A91	D0:0		AD[0]	A58	A0:0	
Control (Sym)	RST#	A15	+ C3:5	Intrpt	INTD#	B08	C0:3	
	REQ64#	A60	+ C1:0		INTC#	A07	C0:2	
	ACK64#	B60	+ C1:1		INTB#	B07	C0:1	
	FRAME#	A34	+ C2:0	Misc	INTA#	A06	C0:0	
	DEVSEL#	B37	+ CLK1		REQ#	B18	C0:5	
	STOP#	A38	+ C2:3		GNT#	A17	C0:6	
	IRDY#	B35	+ C2:1		LOCK#	B39	C3:4	
	TRDY#	A36	+ C2:2		IDSEL	A26	C0:4	
	C/BE#[7]	A64	+ C1:7		PERR#	B40	C3:3	
	C/BE#[6]	B65	+ C1:6		PAR	A43	C3:2	
	C/BE#[5]	A65	+ C1:5		SERR#	B42	C3:1	
	C/BE#[3]	B26	+ C2:7		CLK	B16	+ CLK3	
	C/BE#[2]	B33	+ C2:6		Ungrouped	SDONE	A40	C3:6
	C/BE#[1]	B44	+ C2:5			SBO#	A41	C1:3
C/BE#[0]	A52	+ C2:4	M66EN	B49		C0:7		

Table 3- PCI64L TLA 102-/136-channel Grouping

Note: All signals listed above are required for proper disassembly

Note: Signals with a '+' are required for proper clocking / disassembly

3.0 SOFTWARE INSTALLATION

Two disks are included with the NEX-PCI32SWL:

NEX-PCI32L - 32-bit PCI support for TLA600/700 102- and 136-channel modules

NEX-PCI32L68 - 32-bit support for a TLA600/700 68-channel module

Three disks are included with the NEX-PCI3264SWL. The two disks mentioned above and:

NEX-PCI64L - 64-bit PCI support for TLA600/700 102-and 136-channel modules

The PCI support software is loaded in the same method as other Windows programs. Place the NEX-PCI32L, NEX-PCI32L68 or NEX-PCI64L Install disk in the floppy drive of the TLA.

Select **Control Panel** and run **Add/Remove Programs**, choose **Install, Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose either PCI32L, PCI32L68 or PCI64L and click on **Okay**.

4.0 CLOCK SELECTION

4.1 General Information

There are three clocking options available when using the 32-bit PCI32L and PCI32L68 supports, and two selections when using the PCI64L support package. Each is explained in detail below.

The clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

4.2 Clocking Options - Explanation

Bus Cycle Acquisition - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable (32-bit support only) - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge - In this mode, data will be acquired on every rising edge of the PCI CLK signal. The support software will filter and display these cycles accordingly, although incorrect decoding may occur occasionally because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

5.0 VIEWING DATA

5.1 Viewing Timing Data on the TLA

By default, the TLA will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PCI32L, PCI32L68,

or PCI64L, and PCI32L-MagniVu, PCI32L68-MagniVu, or PCI64L-MagniVu. The first (PCI32L, PCI32L68, or PCI64L) will show the same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PCI32L-MagniVu, PCI32L68-MagniVu, or PCI64L-MagniVu will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA700 System User's Manual for additional information on formatting the Waveform display.

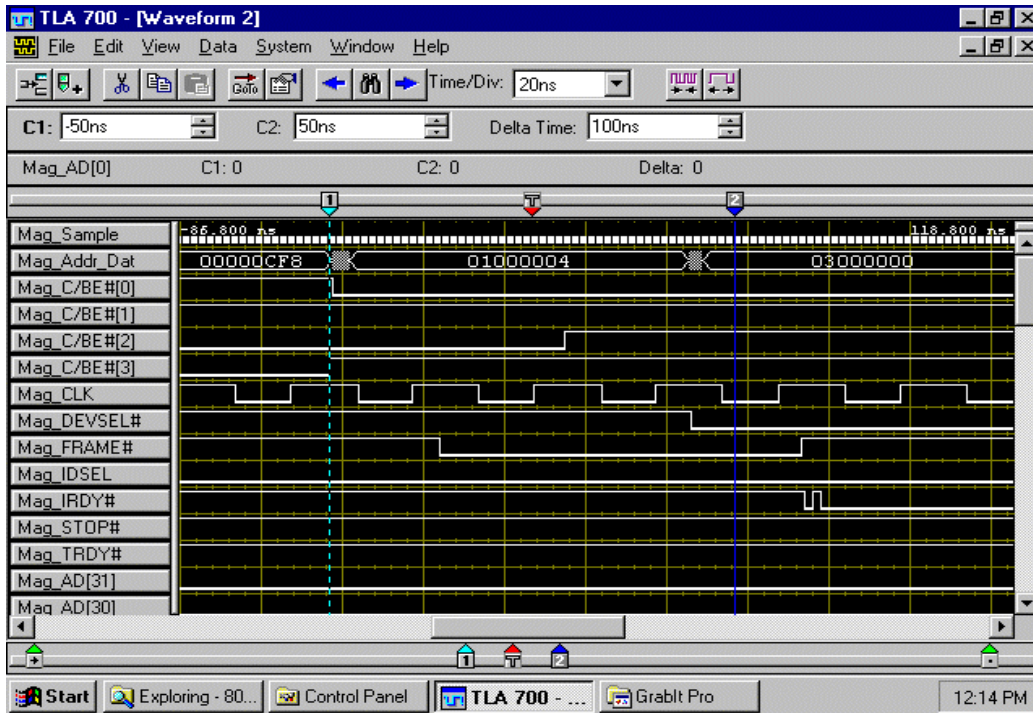


Figure 1- PCI32L TLA MagniVu Display

Pattern	TLA Symbol	Meaning
0xxxxxxxxx	RESET	Reset
1011110000	INTERRUPT ACK	Interrupt Acknowledge
1011110001	SPECIAL CYCLE	Special Cycle
1011110010	I/O READ ADDRESS	I/O Read
1011110011	I/O WRITE ADDRESS	I/O Write
101111010x	RESERVED	Reserved
1011110110	MEMORY READ ADDRESS	Memory Read
1011110111	MEMORY WRITE ADDRESS	Memory Write
101111100x	RESERVED	Reserved
1011111010	CONFIG READ ADDRESS	Configuration Read
1011111011	CONFIG WRITE ADDRESS	Configuration Write
1011111100	MEMORY READ MULTIPLE	Memory Read Multiple
1011111101	DUAL ADDRESS	Dual Address Cycle
1011111110	MEMORY READ LINE	Memory Read Line
1011111111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
1x0x001110	DATA - BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA - BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA - BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA - BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA - BYTES 0 & 1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA - BYTES 2 & 3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA - BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo

Table 4- PCI32L & PCI32L68 Control Symbol Table

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

Pattern	TLA Symbols	Meaning
0xxxxxxxxxxxxxx	RESET	Reset
1xx01111xxxx0000	INTERRUPT ACK	Interrupt Acknowledge
1xx01111xxxx0001	SPECIAL CYCLE	Special Cycle
1xx01111xxxx0010	I/O READ ADDRESS	I/O Read
1xx01111xxxx0011	I/O WRITE ADDRESS	I/O Write
1xx01111xxxx010x	RESERVED	Reserved
1xx01111xxxx0110	MEMORY READ ADDRESS	Memory Read
1xx01111xxxx0111	MEMORY WRITE ADDRESS	Memory Write
1xx01111xxxx100x	RESERVED	Reserved
1xx01111xxxx1010	CONFIG READ ADDRESS	Configuration Read
1xx01111xxxx1011	CONFIG WRITE ADDRESS	Configuration Write
1xx01111xxxx1100	MEMORY READ MULTIPLE	Memory Read Multiple
1xx01111xxxx1101	DUAL ADDRESS	Dual Address Cycle
1xx01111xxxx1110	MEMORY READ LINE	Memory Read Line
1xx01111xxxx1111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
1xx11101xxxxxxxxx	WAIT/MASTER ABORT	Wait or Master Abort
1xx11001xxxxxxxxx	TARGET ABORT	Target Abort
1xx10001xxxxxxxxx	RETRY	Retry Cycle
111x0x0011111110	BYTE 0	Byte 0 valid (D0-7)
111x0x0011111101	BYTE 1	Byte 1 valid (D8-15)
111x0x0011111011	BYTE 2	Byte 2 valid (D16-23)
111x0x0011110111	BYTE 3	Byte 3 valid (D24-31)
111x0x0011101111	BYTE 4	Byte 4 valid (D32-39)
111x0x0011011111	BYTE 5	Byte 5 valid (D40-47)
111x0x0010111111	BYTE 6	Byte 6 valid (D48-55)
111x0x0001111111	BYTE 7	Byte 7 valid (D56-63)
111x0x0011111100	BYTES 0,1	Bytes 0 & 1 valid (D0-15)
111x0x0011110011	BYTES 2,3	Bytes 2 & 3 valid (D16-31)
111x0x0011001111	BYTES 4,5	Bytes 4 & 5 valid (D32-47)
111x0x0000111111	BYTES 6,7	Bytes 6 & 7 valid (D48-63)
111x0x0011110000	BYTES 0-3	Bytes 0-3 valid (D0-31)
111x0x0000001111	BYTES 4-7	Bytes 4-7 valid (D32-63)
100x0x0000000000	BYTES 0-7	Bytes 0-3 valid (D0-63)
111x0x00xxxx0000	LOW 32-BITS	Lower 32-bit (bytes 0-3) operation
1xxx0x0011111111	INVALID DATA	Invalid Data
1xx1xxxxxxxxxxxxxx	FRAME HI	Frame Hi
1xx0xxxxxxxxxxxxxx	FRAME LO	Frame Lo

Table 5- PCI64L Control Symbol Table

Signals, from left to right: RST#, REQ64#, ACQ64#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

6.0 USING THE DISASSEMBLY SOFTWARE

6.1 General

The PCI32L, PCI32L68 and PCI64L support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the PCI32L, PCI32L68 and PCI64L software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 4.2 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps in the TLA700 series, permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

6.2 Disassembly Using the TLA

The TLA Logic Analyzer, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties

- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark (disabled)

Sample	PCI64X AD_Hi	PCI64X AD_Lo	PCI64X Mnemonics	Timestamp
	-----	FFFE0000	Memory Not Prefetchable	
	-----	FFFE0000	Decoder for 128KB Memory Space	
438	-----	04000010	CONFIG WRITE ADDRESS	6.904,570,000 ms
	-----	04000010	Type 0 Register 4 Function 0	
439	-----	00000000	CONFIG WRITE DATA	6.904,600,000 ms
	-----	00000000	Write to Base Address Register 0	
440	-----	04000008	CONFIG READ ADDRESS	6.908,491,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
441	-----	03000002	CONFIG READ DATA	6.908,536,500 ms
	-----	03000002	Class 0x03 - Display controller	
	-----	03000002	Sub-Class 0x00	
	-----	03000002	Prog. I/F 0x00 - VGA compatible	
	-----	03000002	Revision ID 2	
442	-----	04000010	CONFIG READ ADDRESS	6.937,764,500 ms
	-----	04000010	Type 0 Register 4 Function 0	
443	-----	-----00	CONFIG READ DATA	6.937,809,000 ms
	-----	-----00	Invalid Base Address data	
	-----	-----00	Base Address Register 0	
	-----	-----00	Memory Address Register	
	-----	-----00	Locate anywhere in 32-bit space	
	-----	-----00	Memory Not Prefetchable	
	-----	-----00	Decoder for 16 bytes Memory Space	
444	-----	04000008	CONFIG READ ADDRESS	6.941,296,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
445	-----	03000002	CONFIG READ DATA	6.941,341,500 ms

Figure 2- PCI64L Disassembly

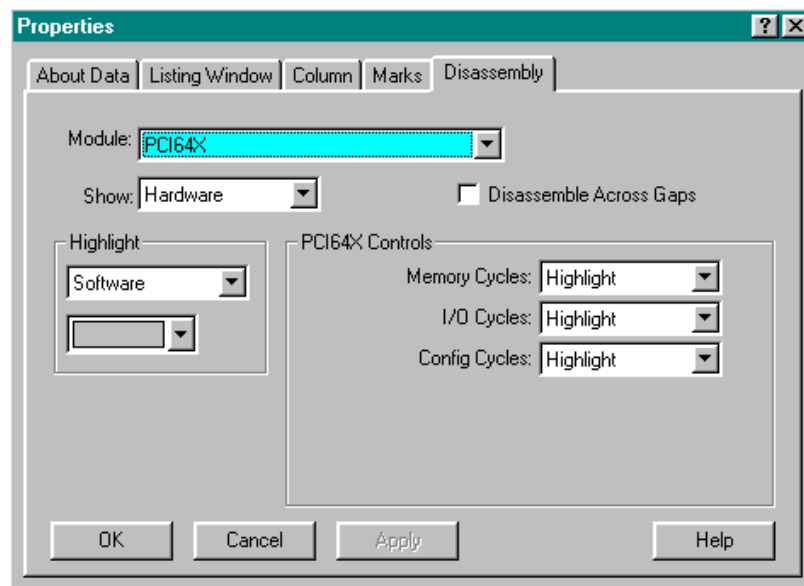


Figure 3- PCI64L Cycle Filtering Window

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PCI32L / PCI32L68 / PCI64L disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

APPENDIX A - PCI 32-bit Mictor Pinout

The following Mictor wiring must be followed if the NEX-PCI32L or NEX-PCI32L68 disassembly software is to be used. Please refer to the Tektronix P6434 Mass Termination Probe Instruction Manual for further information on designing the Mictor connectors into your target. TLA inputs that show dashes ('---') in the PCI Signal and Pin Number columns are unassigned, and may be connected to any target signal desired.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	CLK0	---	---	36	6	CLK1	DEVSEL#	B37
4	7	A3:7	AD[31]	B20	35	8	A1:7	AD[15]	A44
5	9	A3:6	AD[30]	A20	34	10	A1:6	AD[14]	B45
6	11	A3:5	AD[29]	B21	33	12	A1:5	AD[13]	A46
7	13	A3:4	AD[28]	A22	32	14	A1:4	AD[12]	B47
8	15	A3:3	AD[27]	B23	31	16	A1:3	AD[11]	A47
9	17	A3:2	AD[26]	A23	30	18	A1:2	AD[10]	B48
10	19	A3:1	AD[25]	B24	29	20	A1:1	AD[9]	A49
11	21	A3:0	AD[24]	A25	28	22	A1:0	AD[8]	B52
12	23	A2:7	AD[23]	B27	27	24	A0:7	AD[7]	B53
13	25	A2:6	AD[22]	A28	26	26	A0:6	AD[6]	A54
14	27	A2:5	AD[21]	B29	25	28	A0:5	AD[5]	B55
15	29	A2:4	AD[20]	A29	24	30	A0:4	AD[4]	A55
16	31	A2:3	AD[19]	B30	23	32	A0:3	AD[3]	B56
17	33	A2:2	AD[18]	A31	22	34	A0:2	AD[2]	A57
18	35	A2:1	AD[17]	B32	21	36	A0:1	AD[1]	B58
19	37	A2:0	AD[16]	A32	20	38	A0:0	AD[0]	A58

Mictor Group A

Note:

1. All signals on this Mictor required for proper clocking and disassembly

APPENDIX A - PCI 32-bit Mictor Pinout (cont'd.)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	CLK3 ¹	CLK	B16	36	6	QUAL1	---	---
4	7	C3:7	---	---	35	8	C1:7	---	---
5	9	C3:6	SDONE	A40	34	10	C1:6	---	---
6	11	C3:5	RST#	A15	33	12	C1:5	---	---
7	13	C3:4	LOCK#	B39	32	14	C1:4	---	---
8	15	C3:3	PERR#	B40	31	16	C1:3	SBO#	A41
9	17	C3:2	PAR	A43	30	18	C1:2	---	---
10	19	C3:1	SERR#	B42	29	20	C1:1	ACQ64#	B60
11	21	C3:0	---	---	28	22	C1:0	REQ64#	A60
12	23	C2:7 ¹	C/BE[3]#	B26	27	24	C0:7	M66EN	B49
13	25	C2:6 ¹	C/BE[2]#	B33	26	26	C0:6	GNT#	A17
14	27	C2:5 ¹	C/BE[1]#	B44	25	28	C0:5	REQ#	B18
15	29	C2:4 ¹	C/BE[0]#	A52	24	30	C0:4	IDSEL	A26
16	31	C2:3 ¹	STOP#	A38	23	32	C0:3	INTD#	B08
17	33	C2:2 ¹	TRDY#	A36	22	34	C0:2	INTC#	A07
18	35	C2:1 ¹	IRDY#	B35	21	36	C0:1	INTB#	B07
19	37	C2:0 ¹	FRAME #	A34	20	38	C0:0	INTA#	A06

Group C Mictor

Notes:

1. These signals are required for proper 32-bit clocking and disassembly.

APPENDIX B - PCI 32-bit P6860 Compression Pinout

The following probe footprint wiring must be followed if the NEX-PCI32L or NEX-PCI32L68 disassembly software is to be used. For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00. TLA inputs that show dashes (‘---’) in the PCI Signal and Pin Number columns are unassigned, and may be connected to any target signal desired.

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CLK1-	GND	GND
A13	CLK1+	DEVSEL#	B37
B12	A1:7	AD[15]	A44
B10	A1:6	AD[14]	B45
A12	A1:5	AD[13]	A46
A10	A1:4	AD[12]	B47
B9	A1:3	AD[11]	A47
B7	A1:2	AD[10]	B48
A9	A1:1	AD[9]	A49
A7	A1:0	AD[8]	B52
B6	A0:7	AD[7]	B53
B4	A0:6	AD[6]	A54
A6	A0:5	AD[5]	B55
A4	A0:4	AD[4]	A55
B3	A0:3	AD[3]	B56
B1	A0:2	AD[2]	A57
A3	A0:1	AD[1]	B58
A1	A0:0	AD[0]	A58

Probe Connection A0/A1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CLK0-	GND	GND
A13	CLK0+	---	---
B12	A3:7	AD[31]	B20
B10	A3:6	AD[30]	A20
A12	A3:5	AD[29]	B21
A10	A3:4	AD[28]	A22
B9	A3:3	AD[27]	B23
B7	A3:2	AD[26]	A23
A9	A3:1	AD[25]	B24
A7	A3:0	AD[24]	A25
B6	A2:7	AD[23]	B27
B4	A2:6	AD[22]	A28
A6	A2:5	AD[21]	B29
A4	A2:4	AD[20]	A29
B3	A2:3	AD[19]	B30
B1	A2:2	AD[18]	A31
A3	A2:1	AD[17]	B32
A1	A2:0	AD[16]	A32

Probe Connection A2/A3

Note:

All signals are required for proper clocking and disassembly.

APPENDIX B - PCI 32-bit P6860 Compression Pinout (cont'd.)

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	Q1-	Gnd	Gnd
A13	Q1+	---	---
B12	C1:7	---	---
B10	C1:6	---	---
A12	C1:5	---	---
A10	C1:4	---	---
B9	C1:3	SBO#	A41
B7	C1:2	---	---
A9	C1:1	ACQ64#	B60
A7	C1:0	REQ64#	A60
B6	C0:7	M66EN	B49
B4	C0:6	GNT#	A17
A6	C0:5	REQ#	B18
A4	C0:4	IDSEL	A26
B3	C0:3	INTD#	B08
B1	C0:2	INTC#	A07
A3	C0:1	INTB#	B07
A1	C0:0	INTA#	A06

Probe Connection C0/C1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+ ¹	CLK	B16
B12	C3:7	---	---
B10	C3:6	SDONE	A40
A12	C3:5	RST#	A15
A10	C3:4	LOCK#	B39
B9	C3:3	PERR#	B40
B7	C3:2	PAR	A43
A9	C3:1	SERR#	B42
A7	C3:0	---	---
B6	C2:7 ¹	C/BE[3]#	B26
B4	C2:6 ¹	C/BE[2]#	B33
A6	C2:5 ¹	C/BE[1]#	B44
A4	C2:4 ¹	C/BE[0]#	A52
B3	C2:3 ¹	STOP#	A38
B1	C2:2 ¹	TRDY#	A36
A3	C2:1 ¹	IRDY#	B35
A1	C2:0 ¹	FRAME#	A34

Probe Connection C2/C3

Notes:

1. These signals are required for proper 32-bit clocking and disassembly.

APPENDIX C - PCI 32-bit P6960 Pinout

The following probe footprint wiring must be followed if the NEX-PCI32L68 disassembly software is to be used. For further information on the P6960 D-Max probe footprint, please refer to the “P69xx Series High-Density Logic Analyzer Probes with D-Max Probing Technology” Instruction Manual, Tektronix part number 071-1528-02. TLA inputs that show dashes (‘---’) in the PCI Signal column are unassigned, and may be connected to any target signal desired.

Probe 2 Pad	TLA Input	PCI Signal	Probe 2 Pad	TLA Input	PCI Signal
A8	CK1-	GND	B20	CK2-	
A7	CK1+	DEVSEL ¹	B21	CK2+	---
A14	A1:7	AD[15] ¹	B14	D1:7	---
A13	A1:6	AD[14] ¹	B15	D1:6	---
B12	A1:5	AD[13] ¹	A16	D1:5	---
B11	A1:4	AD[12] ¹	A17	D1:4	---
A11	A1:3	AD[11] ¹	B17	D1:3	SBO#
A10	A1:2	AD[10] ¹	B18	D1:2	---
B9	A1:1	AD[9] ¹	A19	D1:1	ACQ64#
B8	A1:0	AD[8] ¹	A20	D1:0	REQ64#
B6	A0:7	AD[7] ¹	A22	D0:7	M66EN
B5	A0:6	AD[6] ¹	A23	D0:6	GNT#
A5	A0:5	AD[5] ¹	B23	D0:5	REQ#
A4	A0:4	AD[4] ¹	B24	D0:4	IDSEL
B3	A0:3	AD[3] ¹	A25	D0:3	INTD#
B2	A0:2	AD[2] ¹	A26	D0:2	INTC#
A2	A0:1	AD[1] ¹	B26	D0:1	INTB#
A1	A0:0	AD[0] ¹	B27	D0:0	INTA#

Probe 1 Pad	TLA Input	PCI Signal	Probe 1 Pad	TLA Input	PCI Signal
A8	CK3-	GND	B20	CK0-	---
A7	CK3+	CLK ¹	B21	CK0+	---
A14	C3:7	---	B14	A3:7	AD[31] ¹
A13	C3:6	SDONE	B15	A3:6	AD[30] ¹
B12	C3:5	RST# ¹	A16	A3:5	AD[29] ¹
B11	C3:4	LOCK#	A17	A3:4	AD[28] ¹
A11	C3:3	PERR#	B17	A3:3	AD[27] ¹
A10	C3:2	PAR	B18	A3:2	AD[26] ¹
B9	C3:1	SERR#	A19	A3:1	AD[25] ¹
B8	C3:0	---	A20	A3:0	AD[24] ¹
B6	C2:7	C/BE[3]# ¹	A22	A2:7	AD[23] ¹
B5	C2:6	C/BE[2]# ¹	A23	A2:6	AD[22] ¹
A5	C2:5	C/BE[1]# ¹	B23	A2:5	AD[21] ¹
A4	C2:4	C/BE[0]# ¹	B24	A2:4	AD[20] ¹
B3	C2:3	STOP# ¹	A25	A2:3	AD[19] ¹
B2	C2:2	TRDY# ¹	A26	A2:2	AD[18] ¹
A2	C2:1	IRDY# ¹	B26	A2:1	AD[17] ¹
A1	C2:0	FRAME# ¹	B27	A2:0	AD[16] ¹

Notes:

1. These signals are required for proper 32-bit clocking and disassembly

APPENDIX D - PCI 32-/64-bit Mictor Pinout

The following Mictor wiring must be followed if the NEX-PCI64L disassembly software is to be used. Please refer to the Tektronix P6434 Mass Termination Probe Instruction Manual for further information on designing the Mictor connectors into your target. TLA inputs that show dashes ('---') in the PCI Signal and Pin Number columns are unassigned, and may be connected to any target signal desired.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	CLK0	---	---	36	6	CLK1	DEVSEL#	B37
4	7	A3:7	AD[31]	B20	35	8	A1:7	AD[15]	A44
5	9	A3:6	AD[30]	A20	34	10	A1:6	AD[14]	B45
6	11	A3:5	AD[29]	B21	33	12	A1:5	AD[13]	A46
7	13	A3:4	AD[28]	A22	32	14	A1:4	AD[12]	B47
8	15	A3:3	AD[27]	B23	31	16	A1:3	AD[11]	A47
9	17	A3:2	AD[26]	A23	30	18	A1:2	AD[10]	B48
10	19	A3:1	AD[25]	B24	29	20	A1:1	AD[9]	A49
11	21	A3:0	AD[24]	A25	28	22	A1:0	AD[8]	B52
12	23	A2:7	AD[23]	B27	27	24	A0:7	AD[7]	B53
13	25	A2:6	AD[22]	A28	26	26	A0:6	AD[6]	A54
14	27	A2:5	AD[21]	B29	25	28	A0:5	AD[5]	B55
15	29	A2:4	AD[20]	A29	24	30	A0:4	AD[4]	A55
16	31	A2:3	AD[19]	B30	23	32	A0:3	AD[3]	B56
17	33	A2:2	AD[18]	A31	22	34	A0:2	AD[2]	A57
18	35	A2:1	AD[17]	B32	21	36	A0:1	AD[1]	B58
19	37	A2:0	AD[16]	A32	20	38	A0:0	AD[0]	A58

Group A Mictor

Notes:

1. All signals on this Mictor required for proper 32- or 64-bit clocking and disassembly.

APPENDIX D - PCI 32-/64-bit Mictor Pinout (cont'd.)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	CLK3 ¹	CLK	B16	36	6	QUAL1	---	---
4	7	C3:7	---	---	35	8	C1:7 ²	C/BE[7]#	A64
5	9	C3:6	SDONE	A40	34	10	C1:6 ²	C/BE[6]#	B65
6	11	C3:5 ¹	RST#	A15	33	12	C1:5 ²	C/BE[5]#	A65
7	13	C3:4	LOCK#	B39	32	14	C1:4 ²	C/BE[4]#	B66
8	15	C3:3	PERR#	B40	31	16	C1:3	SBO#	A41
9	17	C3:2	PAR	A43	30	18	C1:2	PAR64	A67
10	19	C3:1	SERR#	B42	29	20	C1:1 ²	ACQ64#	B60
11	21	C3:0	---	---	28	22	C1:0 ²	REQ64#	A60
12	23	C2:7 ¹	C/BE[3]#	B26	27	24	C0:7	M66EN	B49
13	25	C2:6 ¹	C/BE[2]#	B33	26	26	C0:6	GNT#	A17
14	27	C2:5 ¹	C/BE[1]#	B44	25	28	C0:5	REQ#	B18
15	29	C2:4 ¹	C/BE[0]#	A52	24	30	C0:4	IDSEL	A26
16	31	C2:3 ¹	STOP#	A38	23	32	C0:3	INTD#	B08
17	33	C2:2 ¹	TRDY#	A36	22	34	C0:2	INTC#	A07
18	35	C2:1 ¹	IRDY#	B35	21	36	C0:1	INTB#	B07
19	37	C2:0 ¹	FRAME#	A34	20	38	C0:0	INTA#	A06

Group C Mictor

Notes:

1. These signals are required for proper 32- or 64-bit clocking and disassembly
2. These signals are required for proper 64-bit disassembly

APPENDIX D - PCI 32-/64-bit Mictor Pinout (cont'd.)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	PCI Signal Name	PCI Pin #
3	5	QUAL0	---	---	36	6	CLK2	---	---
4	7	D3:7	AD[63]	B68	35	8	D1:7	AD[47]	B80
5	9	D3:6	AD[62]	A68	34	10	D1:6	AD[46]	A80
6	11	D3:5	AD[61]	B69	33	12	D1:5	AD[45]	B81
7	13	D3:4	AD[60]	A70	32	14	D1:4	AD[44]	A82
8	15	D3:3	AD[59]	B71	31	16	D1:3	AD[43]	B83
9	17	D3:2	AD[58]	A71	30	18	D1:2	AD[42]	A83
10	19	D3:1	AD[57]	B72	29	20	D1:1	AD[41]	B84
11	21	D3:0	AD[56]	A73	28	22	D1:0	AD[40]	A85
12	23	D2:7	AD[55]	B74	27	24	D0:7	AD[39]	B86
13	25	D2:6	AD[54]	A74	26	26	D0:6	AD[38]	A86
14	27	D2:5	AD[53]	B75	25	28	D0:5	AD[37]	B87
15	29	D2:4	AD[52]	A76	24	30	D0:4	AD[36]	A88
16	31	D2:3	AD[51]	B77	23	32	D0:3	AD[35]	B89
17	33	D2:2	AD[50]	A77	22	34	D0:2	AD[34]	A89
18	35	D2:1	AD[49]	B78	21	36	D0:1	AD[33]	B90
19	37	D2:0	AD[48]	A79	20	38	D0:0	AD[32]	A91

Group D Mictor

Notes:

1. All signals on this Mictor required for proper 64-bit disassembly.

APPENDIX E - PCI 32-/64-bit P6860 Compression Pinout

The following wiring must be followed if the NEX-PCI64L disassembly software is to be used. For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00. TLA inputs that show dashes (‘---’) in the PCI Signal and Pin Number columns are unassigned, and may be connected to any target signal desired.

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK1-	Gnd	Gnd
A13	CLK1	DEVSEL#	B37
B12	A1:7	AD[15]	A44
B10	A1:6	AD[14]	B45
A12	A1:5	AD[13]	A46
A10	A1:4	AD[12]	B47
B9	A1:3	AD[11]	A47
B7	A1:2	AD[10]	B48
A9	A1:1	AD[9]	A49
A7	A1:0	AD[8]	B52
B6	A0:7	AD[7]	B53
B4	A0:6	AD[6]	A54
A6	A0:5	AD[5]	B55
A4	A0:4	AD[4]	A55
B3	A0:3	AD[3]	B56
B1	A0:2	AD[2]	A57
A3	A0:1	AD[1]	B58
A1	A0:0	AD[0]	A58

Probe Connection A0/A1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK0-	Gnd	Gnd
A13	CLK0	---	---
B12	A3:7	AD[31]	B20
B10	A3:6	AD[30]	A20
A12	A3:5	AD[29]	B21
A10	A3:4	AD[28]	A22
B9	A3:3	AD[27]	B23
B7	A3:2	AD[26]	A23
A9	A3:1	AD[25]	B24
A7	A3:0	AD[24]	A25
B6	A2:7	AD[23]	B27
B4	A2:6	AD[22]	A28
A6	A2:5	AD[21]	B29
A4	A2:4	AD[20]	A29
B3	A2:3	AD[19]	B30
B1	A2:2	AD[18]	A31
A3	A2:1	AD[17]	B32
A1	A2:0	AD[16]	A32

Probe Connection A2/A3

Notes:

1. All signals are required for proper 32- or 64-bit clocking and disassembly.

APPENDIX E - PCI 32-/64-bit P6860 Compression Pinout (cont'd.)

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	Q1-	Gnd	Gnd
A13	Q1+	---	---
B12	C1:7 ²	C/BE[7]#	A64
B10	C1:6 ²	C/BE[6]#	B65
A12	C1:5 ²	C/BE[5]#	A65
A10	C1:4 ²	C/BE[4]#	B66
B9	C1:3	SBO#	A41
B7	C1:2	PAR64	A67
A9	C1:1 ²	ACQ64#	B60
A7	C1:0 ²	REQ64#	A60
B6	C0:7	M66EN	B49
B4	C0:6	GNT#	A17
A6	C0:5	REQ#	B18
A4	C0:4	IDSEL	A26
B3	C0:3	INTD#	B08
B1	C0:2	INTC#	A07
A3	C0:1	INTB#	B07
A1	C0:0	INTA#	A06

Probe Connection C0/C1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+ ¹	CLK	B16
B12	C3:7	---	---
B10	C3:6	SDONE	A40
A12	C3:5 ¹	RST#	A15
A10	C3:4	LOCK#	B39
B9	C3:3	PERR#	B40
B7	C3:2	PAR	A43
A9	C3:1	SERR#	B42
A7	C3:0	---	---
B6	C2:7 ¹	C/BE[3]#	B26
B4	C2:6 ¹	C/BE[2]#	B33
A6	C2:5 ¹	C/BE[1]#	B44
A4	C2:4 ¹	C/BE[0]#	A52
B3	C2:3 ¹	STOP#	A38
B1	C2:2 ¹	TRDY#	A36
A3	C2:1 ¹	IRDY#	B35
A1	C2:0 ¹	FRAME#	A34

Probe Connection C2/C3

Notes:

1. These signals are required for proper 32- or 64-bit clocking and disassembly
2. These signals are required for proper 64-bit disassembly

APPENDIX E - PCI 32-/64-bit P6860 Compression Pinout (cont'd.)

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	CK2-	Gnd	Gnd
A13	CK2+	---	---
B12	D1:7	AD[47]	B80
B10	D1:6	AD[46]	A80
A12	D1:5	AD[45]	B81
A10	D1:4	AD[44]	A82
B9	D1:3	AD[43]	B83
B7	D1:2	AD[42]	A83
A9	D1:1	AD[41]	B84
A7	D1:0	AD[40]	A85
B6	D0:7	AD[39]	B86
B4	D0:6	AD[38]	A86
A6	D0:5	AD[37]	B87
A4	D0:4	AD[36]	A88
B3	D0:3	AD[35]	B89
B1	D0:2	AD[34]	A89
A3	D0:1	AD[33]	B90
A1	D0:0	AD[32]	A91

Probe Connection D0/D1

Pad #	TLA Channel	PCI Signal Name	PCI Pin #
A15	Q0-	Gnd	Gnd
A13	Q0+	---	---
B12	D3:7	AD[63]	B68
B10	D3:6	AD[62]	A68
A12	D3:5	AD[61]	B69
A10	D3:4	AD[60]	A70
B9	D3:3	AD[59]	B71
B7	D3:2	AD[58]	A71
A9	D3:1	AD[57]	B72
A7	D3:0	AD[56]	A73
B6	D2:7	AD[55]	B74
B4	D2:6	AD[54]	A74
A6	D2:5	AD[53]	B75
A4	D2:4	AD[52]	A76
B3	D2:3	AD[51]	B77
B1	D2:2	AD[50]	A77
A3	D2:1	AD[49]	B78
A1	D2:0	AD[48]	A79

Probe Connection D2/D3

Notes:

1. All signals required for proper 64-bit disassembly.

APPENDIX F - PCI 32-/64-bit P6960 Pinout

Probe 3 Pad	TLA Input	PCI Signal	Probe 3 Pad	TLA Input	PCI Signal	Probe 2 Pad	TLA Input	PCI Signal
A8	CK0-	GND	B20	Q0-		A8	CK1-	GND
A7	CK0+	---	B21	Q0+	---	A7	CLK1	DEVSEL# ¹
A14	A3:7	AD[31] ¹	B14	D3:7	AD[63] ₂	A14	A1:7	AD[15] ¹
A13	A3:6	AD[30] ¹	B15	D3:6	AD[62] ₂	A13	A1:6	AD[14] ¹
B12	A3:5	AD[29] ¹	A16	D3:5	AD[61] ₂	B12	A1:5	AD[13] ¹
B11	A3:4	AD[28] ¹	A17	D3:4	AD[60] ₂	B11	A1:4	AD[12] ¹
A11	A3:3	AD[27] ¹	B17	D3:3	AD[59] ₂	A11	A1:3	AD[11] ¹
A10	A3:2	AD[26] ¹	B18	D3:2	AD[58] ₂	A10	A1:2	AD[10] ¹
B9	A3:1	AD[25] ¹	A19	D3:1	AD[57] ₂	B9	A1:1	AD[9] ¹
B8	A3:0	AD[24] ¹	A20	D3:0	AD[56] ₂	B8	A1:0	AD[8] ¹
B6	A2:7	AD[23] ¹	A22	D2:7	AD[55] ₂	B6	A0:7	AD[7] ¹
B5	A2:6	AD[22] ¹	A23	D2:6	AD[54] ₂	B5	A0:6	AD[6] ¹
A5	A2:5	AD[21] ¹	B23	D2:5	AD[53] ₂	A5	A0:5	AD[5] ¹
A4	A2:4	AD[20] ¹	B24	D2:4	AD[52] ₂	A4	A0:4	AD[4] ¹
B3	A2:3	AD[19] ¹	A25	D2:3	AD[51] ₂	B3	A0:3	AD[3] ¹
B2	A2:2	AD[18] ¹	A26	D2:2	AD[50] ₂	B2	A0:2	AD[2] ¹
A2	A2:1	AD[17] ¹	B26	D2:1	AD[49] ₂	A2	A0:1	AD[1] ¹
A1	A2:0	AD[16] ¹	B27	D2:0	AD[48] ₂	A1	A0:0	AD[0] ¹

Probe 2 Pad	TLA Input	PCI Signal	Probe 1 Pad	TLA Input	PCI Signal	Probe 1 Pad	TLA Input	PCI Signal
B20	CK2-	---	A8	CK3-	GND	B20	Q1-	---
B21	CK2+	---	A7	CK3+	CLK ¹	B21	Q1+	---
B14	D1:7	AD[47] ²	A14	C3:7	---	B14	C1:7	C/BE[7]# ²
B15	D1:6	AD[46] ²	A13	C3:6	SDONE	B15	C1:6	C/BE[6]# ²
A16	D1:5	AD[45] ²	B12	C3:5	RST# ¹	A16	C1:5	C/BE[5]# ²
A17	D1:4	AD[44] ²	B11	C3:4	LOCK#	A17	C1:4	C/BE[4]# ²
B17	D1:3	AD[43] ²	A11	C3:3	PERR#	B17	C1:3	SBO#
B18	D1:2	AD[42] ²	A10	C3:2	PAR	B18	C1:2	PAR64
A19	D1:1	AD[41] ²	B9	C3:1	SERR#	A19	C1:1	ACQ64# ²
A20	D1:0	AD[40] ²	B8	C3:0	---	A20	C1:0	REQ64# ²
A22	D0:7	AD[39] ²	B6	C2:7	C/BE[3]# ¹	A22	C0:7	M66EN
A23	D0:6	AD[38] ²	B5	C2:6	C/BE[2]# ¹	A23	C0:6	GNT#
B23	D0:5	AD[37] ²	A5	C2:5	C/BE[1]# ¹	B23	C0:5	REQ#
B24	D0:4	AD[36] ²	A4	C2:4	C/BE[0]# ¹	B24	C0:4	IDSEL
A25	D0:3	AD[35] ²	B3	C2:3	STOP# ¹	A25	C0:3	INTD#
A26	D0:2	AD[34] ²	B2	C2:2	TRDY# ¹	A26	C0:2	INTC#
B26	D0:1	AD[33] ²	A2	C2:1	IRDY# ¹	B26	C0:1	INTB#
B27	D0:0	AD[32] ²	A1	C2:0	FRAME# ¹	B27	C0:0	INTA#

Notes:

2. These signals are required for proper 32- or 64-bit clocking and disassembly
3. These signals are required for proper 64-bit disassembly

APPENDIX G - Necessary Signals for Clocking

To properly acquire PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data or for proper disassembly of the acquired data.

APPENDIX H - PCI Local Bus Pinout

Information given here is for the 64-bit Universal Board definitions:

Pin #	Side B - Component Side	Side A - Solder Side	Comments
1	-12V	TRST#	32-bit start
2	TCK	+12V	
3	Ground	TMS	
4	TDO	TDI	
5	+5V	+5V	
6	+5V	INTA#	
7	INTB#	INTC#	
8	INTD#	+5V	
9	PRSENT1#	Reserved	
10	Reserved	+V I/O	
11	PRSENT2#	Reserved	
12	KEYWAY	KEYWAY	3.3V key
13	KEYWAY	KEYWAY	3.3V key
14	Reserved	Reserved	
15	Ground	RST#	
16	CLK	+V I/O	
17	Ground	GNT#	
18	REQ#	Ground	
19	+V I/O	Reserved	
20	AD[31]	AD[30]	
21	AD[29]	+3.3V	
22	Ground	AD[28]	
23	AD[27]	AD[26]	
24	AD[25]	Ground	
25	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	
28	Ground	AD[22]	
29	AD[21]	AD[20]	
30	AD[19]	Ground	
31	+3.3V	AD[18]	
32	AD[17]	AD[16]	
33	C/BE[2]#	+3.3V	
34	Ground	FRAME#	
35	IRDY#	Ground	
36	+3.3V	TRDY#	
37	DEVSEL#	Ground	
38	Ground	STOP#	
39	LOCK#	+3.3V	
40	PERR#	SDONE	
41	+3.3V	SBO#	
42	SERR#	GROUND	
43	+3.3V	PAR	
44	C/BE[1]#	AD[15]	
45	AD[14]	+3.3V	
46	Ground	AD[13]	
47	AD[12]	AD[11]	

APPENDIX H - PCI Local Bus Pinout (cont'd.)

Pin #	Side B - Component Side	Side A - Solder Side	Comments
48	AD[10]	Ground	
49	M66EN	AD[9]	
50	KEYWAY	KEYWAY	5V key
51	KEYWAY	KEYWAY	5V key
52	AD[8]	C/BE[0]#	
53	AD[7]	+3.3V	
54	+3.3V	AD[6]	
55	AD[5]	AD[4]	
56	AD[3]	Ground	
57	Ground	AD[2]	
58	AD[1]	AD[0]	
59	+V I/O	+V I/O	
60	ACK64#	REQ64#	
61	+5V	+5V	
62	+5V	+5V	32-bit end
	KEYWAY	KEYWAY	64-bit spacer
	KEYWAY	KEYWAY	64-bit spacer
63	Reserved	Ground	64-bit start
64	Ground	C/BE[7]#	
65	C/BE[6]#	C/BE[5]#	
66	C/BE[4]#	+V I/O	
67	Ground	PAR64	
68	AD[63]	AD[62]	
69	AD[61]	Ground	
70	+V I/O	AD[60]	
71	AD[59]	AD[58]	
72	AD[57]	Ground	
73	Ground	AD[56]	
74	AD[55]	AD[54]	
75	AD[53]	+V I/O	
76	Ground	AD[52]	
77	AD[51]	AD[50]	
78	AD[49]	Ground	
79	+V I/O	AD[48]	
80	AD[47]	AD[46]	
81	AD[45]	Ground	
82	Ground	AD[44]	
83	AD[43]	AD[42]	
84	AD[41]	+V I/O	
85	Ground	AD[40]	
86	AD[39]	AD[38]	
87	AD[37]	Ground	
88	+V I/O	AD[36]	
89	AD[35]	AD[34]	
90	AD[33]	Ground	
91	Ground	AD[32]	
92	Reserved	Reserved	
93	Reserved	Ground	
94	Ground	Reserved	

APPENDIX I - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX J - References

Tektronix Logic Analyzer Family V4.0 Software User's Manual
071-0863-00

Tektronix P6434 Mass Termination Probe Manual
070-9793-02

Tektronix P6417 & P6418 Logic Analyzer Probes Manual
071-0567-00

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