NEX-PCIX

PCI-X Bus Adapter Users Manual

Including these Software Support packages:

PCIX64 PCI64PCX PCI32PCX

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1.0 OVERVIEW

1.1 General Information

The NEX-PCIX adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA600 or TLA700, acquisition module to a 64-bit PCI-X backplane. (The PCI-X designation refers to the PCI-X Addendum to the Peripheral Component Interconnect Local Bus specification.) Connections are made through P6434 Mass Termination probes. The P6434 probes are available from Tektronix.

The included NEX-PCIX64 software permits the acquisition of all PCI-X bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. For instance, references to the TLA600 or TLA700 apply to any TLA600 or TLA700 with a minimun 102 channel acquisition card.

Appendix D is a silk-screen print of the NEX-PCIX Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the PCI-X Local Bus specification and the Tektronix TLA600 and TLA700 Logic Analyzer. It is also expected that the user is familiar with Windows 98.

2.0 SOFTWARE INSTALLATION

One 3½" diskette has been included with the NEX-PCIX Bus Adapter.

2.1 TLA600/TLA700

The PCIX64 software is loaded in the same method as other Win98 programs. Place the appropriate Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the PCIX64 support in its proper place on the hard disk.

To load PCIX64 support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose PCIX64 and click on **Okay**.

3.0 CONFIGURING the NEX-PCIX BUS ADAPTER

3.1 General Information

Not all 64-bit PCI–X signals are monitored by either the TLA600 or TLA700. (Refer to Table 1 for a list of acquired signals.) The remaining signals have been brought to a 2x14 header so that they can be monitored, if desired, simply by connecting unused data channels to them. The signals are on the pins nearest the signal names. The leftmost row of pins (opposite the signal names) are all connected to signal ground.

Use the supplied jumper to short or break the connection between TDI and TDO (JP1). If the target card does not support JTAG Boundary Scan then the two pins should be shorted together.

4.0 CONNECTING to the NEX-PCIX ADAPTER

4.1 General

The NEX-PCIX is an extender card that is also designed to permit monitoring the PCI-X bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will violate the PCI-X specification for stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, series resistors have been added to each signal to isolate the effect of the stub running to the mictor connector The design also features a controlled impedence and matched trace length layout.

4.2 TLA700

To use a TLA600/700 with the NEX-PCIX adapter board it is necessary to use the P6434 high-density probes for connecting to the board. Each P6434 probe consists of one high-density probe tip (which connects to the adapter board) and two module ends (which connect to the acquisition card). It is important to note that where the module ends connect to the acquisition card will depend on how many channels the acquisition card has. Be very careful in noting where Pin 1 is on each probe tip, and follow the P6434 Mass Termination Probe manual for instructions on applying the labels.

When using a 102/136-channel acquisition module, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. One P6434 plugs onto the Group A connector on the PCIX adapter and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434 plugs onto the Group C connector on the PCIX adapter and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. The third P6434 plugs onto the Group D connector on the PCIX adapter and then connects to the Yellow (D0 and D1) and Blue (D2 and D3) locations on the acquisition card. Table 1 shows the wiring and Channel Grouping for the 102/136-channel TLA600/700 NEX-PCIX connection.

Group Name	Signal Name	PCI-X Pin #	TLA600/700 input	Group Name	Signal Name	PCI-X Pin #	TLA600/700 input
AD_Hi	AD[63]	B68	D3:7	AD_Lo	AD[31]	B20	A3:7
(Hex)	AD[62]	A68	D3:6	(Hex)	AD[30]	A20	A3:6
	AD[61]	B69	D3:5		AD[29]	B21	A3:5
	AD[60]	A70	D3:4		AD[28]	A22	A3:4
	AD[59]	B71	D3:3		AD[27]	B23	A3:3
	AD[58]	A71	D3:2		AD[26]	A23	A3:2
	AD[57]	B72	D3:1		AD[25]	B24	A3:1
	AD[56]	A73	D3:0		AD[24]	A25	A3:0
	AD[55]	B74	D2:7		AD[23]	B27	A2:7
	AD[54]	A74	D2:6		AD[22]	A28	A2:6
	AD[53]	B75	D2:5		AD[21]	B29	A2:5
	AD[52]	A76	D2:4		AD[20]	A29	A2:4
	AD[51]	B77	D2:3		AD[19]	B30	A2:3
	AD[50]	A77	D2:2		AD[18]	A31	A2:2
	AD[49]	B78	D2:1		AD[17]	B32	A2:1
	AD[48]	A79	D2:0		AD[16]	A32	A2:0
	AD[47]	B80	D1:7		AD[15]	A44	A1:7
	AD[46]	A80	D1:6		AD[14]	B45	A1:6
	AD[45]	B81	D1:5		AD[13]	A46	A1:5
	AD[44]	A82	D1:4		AD[12]	B47	A1:4
	AD[43]	B83	D1:3		AD[11]	A47	A1:3
	AD[42]	A83	D1:2		AD[10]	B48	A1:2
	AD[41]	B84	D1:1		AD[9]	A49	A1:1
	AD[40]	A85	D1:0		AD[8]	B52	A1:0
	AD[39]	B86	D0:7		AD[7]	B53	A0:7
	AD[38]	A86	D0:6		AD[6]	A54	A0:6
	AD[37]	B87	D0:5		AD[5]	B55	A0:5
	AD[36]	A88	D0:4		AD[4]	A55	A0:4
	AD[35]	B89	D0:3		AD[3]	B56	A0:3
	AD[34]	A89	D0:2		AD[2]	A57	A0:2
	AD[33]	B90	D0:1		AD[1]	B58	A0:1
	AD[32]	A91	D0:0		AD[0]	A58	A0:0

Table 1- NEX-PCIX TLA600/700 (102/136-channel) Wiring

Note: All signals listed above are required for proper disassembly

Group Name	Signal Name	PCI-X Pin #	TLA600/700 input
Control (Sym)	RST#	A15	+ Clock:3
	REQ64#	A60	+ C1:5
	ACK64#	B60	+ C0:7
	FRAME#	A34	+ C2:0
	DEVSEL#	B37	+ Clock:1
	STOP#	A38	+ C2:3
	IRDY#	B35	+ C2:1
	TRDY#	A36	+ C2:2
	C/BE#[7]	A64	+ C3:7
	C/BE#[6]	B65	+ C3:6
	C/BE#[5]	A65	+ C3:5
	C/BE#[4]	B66	+ C3:4
	C/BE#[3]	B26	+ C3:3
	C/BE#[2]	B33	+ C3:2
	C/BE#[1]	B44	+ C3:1
	C/BE#[0]	A52	+ C3:0
Intrpt (Off)	INTD#	B08	C0:3
	INTC#	A07	C0:2
	INTB#	B07	C0:1
	INTA#	A06	C0:0
Misc (Off)	PCIXCAP	B38	+ Qual:1
	REQ#	B18	C0:5
	GNT#	A17	C0:6
	LOCK#	B39	C2:6
	IDSEL	A26	C0:4
	PERR#	B40	C2:5
	PAR	A43	C2:4
	SERR	B42	Clock:2
	CLK	B16	+ Clock:0
BusMode	PCIXCAP	B38	+ Qual:1
Ungrouped	PAR64	A67	C1:4
	SBO#	A41	C2:7
	M66EN	B49	C1:6
	SERR#	B42	Clock:2
	SDONE	A40	Qual:0

Table 1 - NEX-PCIX TLA600/700 (102/136-channel) Wiring (cont'd.)

Note: Signals with a '+' are required for proper clocking / disassembly

5.0 CLOCK SELECTION

5.1 General Information

There is one Clocking Select Field that needs to be set properly for accurate PCI-X bus acquisitions to occur. Its selections are explained in detail below.

The clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.2 Clocking Select Field - Explanation

Bus Cycle Acquisition - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will ***not*** be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable (32-bit only) - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge - In this mode, data will be acquired on every rising edge of the PCI CLK signal. The disassembly will filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

6.0 VIEWING DATA

6.1 Viewing Timing Data on the TLA600/700

By default, the TLA600 and TLA700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PCIX64 and PCIX64-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PCIX64-MagniVu will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600 or TLA700 System User's Manual for additional information on formatting the Waveform display.

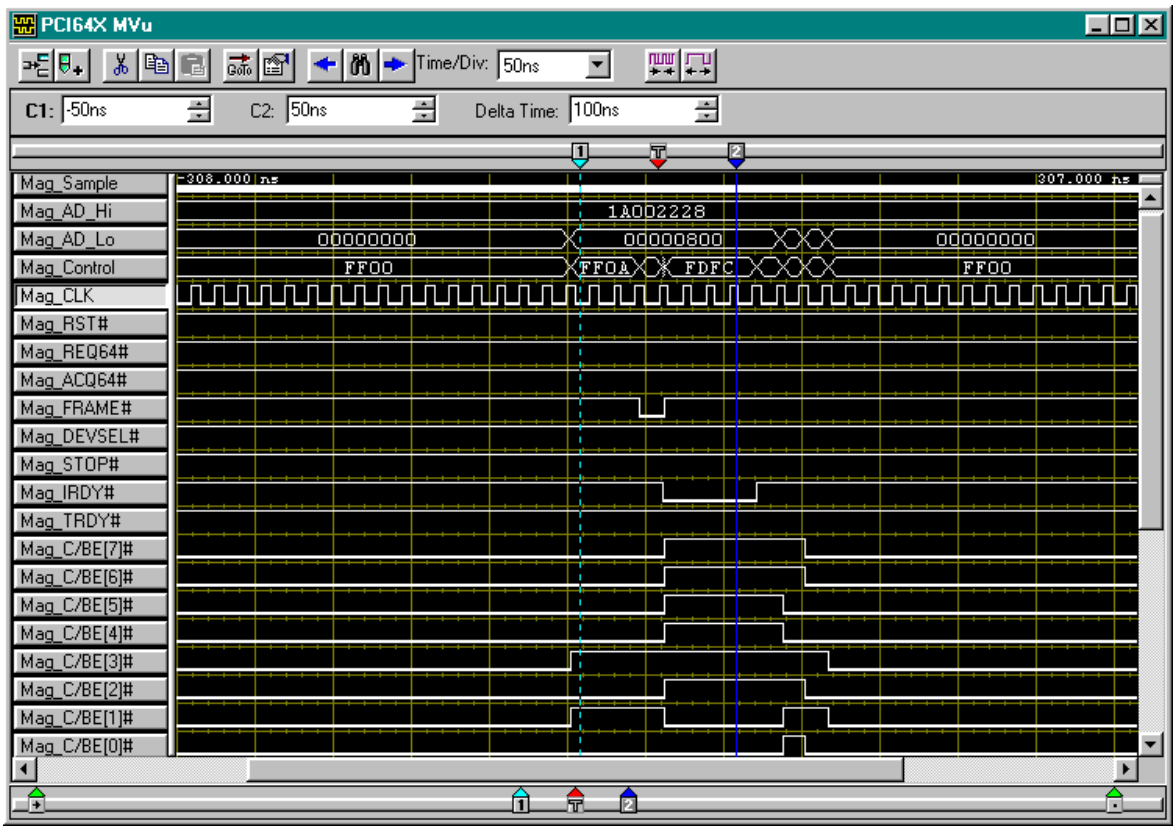


Figure 1- PCIX64 MagniVu Display on TLA700

Pattern	TLA600/700 Symbols	Meaning
0xxxxxxxxxxxxxxx	RESET	Reset
11x01111xxxx0000	INTERRUPT ACK	Interrupt Acknowledge
11x01111xxxx0001	SPECIAL CYCLE	Special Cycle
11x01111xxxx0010	I/O READ ADDR	I/O Read Address
11x01111xxxx0011	I/O WRITE ADDR	I/O Write Address
1xx01111xxxx010x	RESERVED	Reserved
11x01111xxxx0110	MEMORY RD DWORD ADDR	Memory Read DWORD Address
1xx01111xxxx0111	MEMORY WR ADDR	Memory Write Address
1xx01111xxxx1000	ALIAS TO MEM RD BLK	Alias to Memory Read Block
1xx01111xxxx1001	ALIAS TO MEM WRT BLK	Alias to Memory Write Block
11x01111xxxx1010	CONFIG READ ADDR	Configuration Read Address
11x01111xxxx1011	CONFIG WRITE ADDRESS	Configuration Write Address
1xx01111xxxx1100	SPLIT COMPLETION	Split Completion
1xx01111xxxx1101	DUAL ADDR	Dual Address Cycle
1xx01111xxxx1110	MEMORY READ BLOCK	Memory Read Block
1xx01111xxxx1111	MEMORY WRITE BLOCK	Memory Write Block
1xx11101xxxxxxxx	WAIT/MASTER ABORT	Wait or Master Abort
1xx11001xxxxxxxx	TARGET ABORT	Target Abort
1xx10001xxxxxxxx	RETRY	Retry Cycle
111x0x0011111110	BYTE 0	Byte 0 valid (D0-7)
111x0x0011111101	BYTE 1	Byte 1 valid (D8-15)
111x0x0011111011	BYTE 2	Byte 2 valid (D16-23)
111x0x0011110111	BYTE 3	Byte 3 valid (D24-31)
111x0x0011101111	BYTE 4	Byte 4 valid (D32-39)
111x0x0011011111	BYTE 5	Byte 5 valid (D40-47)
111x0x0010111111	BYTE 6	Byte 6 valid (D48-55)
111x0x0001111111	BYTE 7	Byte 7 valid (D56-63)
111x0x0011111100	BYTES 0,1	Bytes 0 & 1 valid (D0-15)
111x0x0011110011	BYTES 2,3	Bytes 2 & 3 valid (D16-31)
111x0x0011001111	BYTES 4,5	Bytes 4 & 5 valid (D32-47)
111x0x0000111111	BYTES 6,7	Bytes 6 & 7 valid (D48-63)
111x0x0011110000	BYTES 0-3	Bytes 0-3 valid (D0-31)
111x0x0000001111	BYTES 4-7	Bytes 4-7 valid (D32-63)
100x0x0000000000	BYTES 0-7	Bytes 0-3 valid (D0-63)
111x0x00xxxx0000	LOW 32-BITS	Low 32-bits valid
1xxx0x0011111111	INVALID DATA	Invalid Data
1xxx00x0xxxxxxxx	DISC AT NEX ADB	Disconnect at next ADB
1xxx10x0xxxxxxxx	SNGL DATA PHASE DISC	Single Data Phase Disconnect
1xx1xxxxxxxxxxx	FRAME HI	Frame Hi
1xx0xxxxxxxxxxx	FRAME LO	Frame Lo

Table 2- PCIX64_Ctrl Control Symbol Table

Signals, from left to right: RST#, REQ64#, ACK64#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

7.0 USING THE DISASSEMBLY SOFTWARE

7.1 General

The PCIX64 support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the PCIX64 software is its ability to intelligently acquire PCI-X data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the PCIX64 software is able to acquire only the PCI-X bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes. the user also has the ability to override this function and acquire data on every PCI-X CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

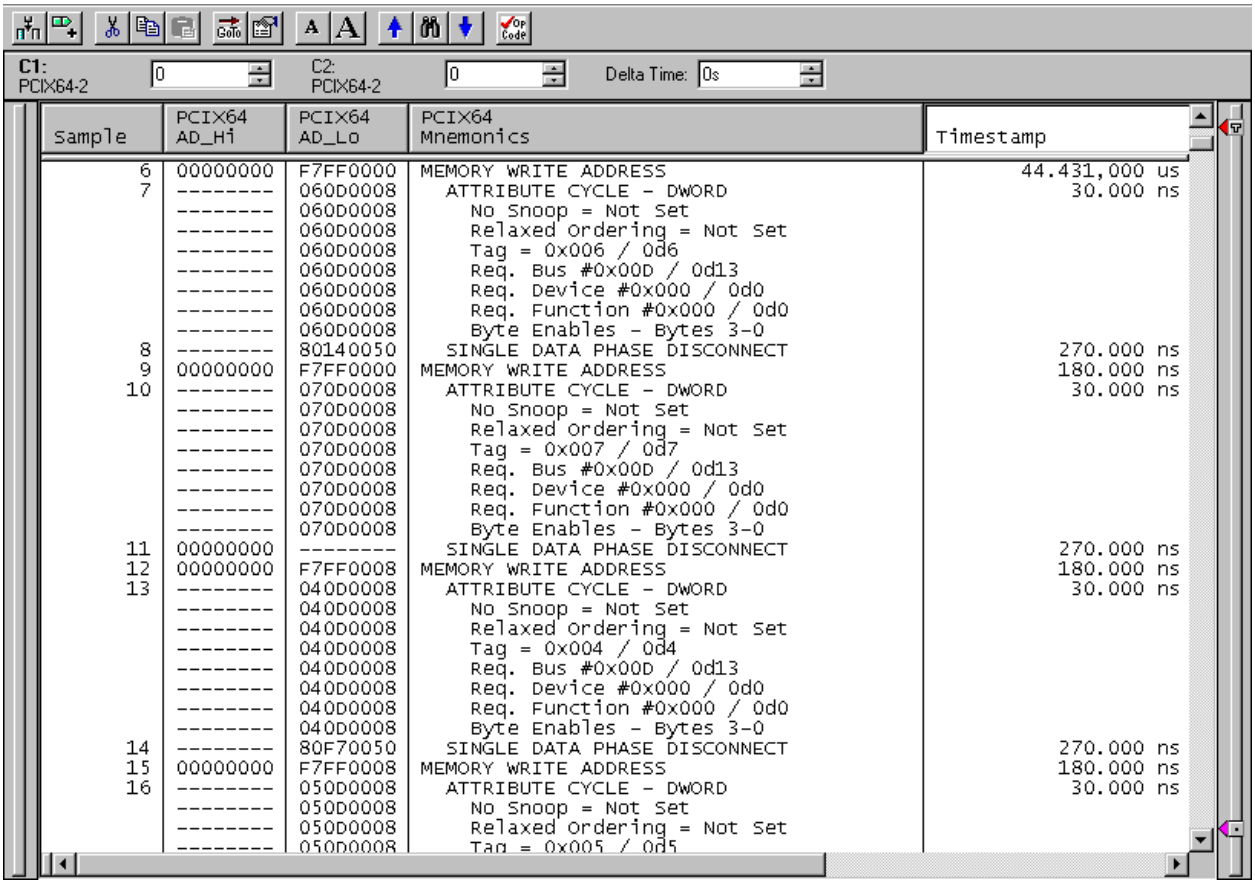
Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps in the TLA600/700 series permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Using the TLA600/700

The TLA600/700, since it is a Windows based instrument, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

Add Column - Adds a column to the display
Add Mark - Adds a user mark to the display
Cut - (may be grayed out) - Cuts the selection to the Clipboard

Copy - (may be grayed out) - Copies the selection to the Clipboard
Paste - (may be grayed out) - Inserts the contents of the Clipboard
Go To - Moves the display to the item of interest
Properties - Edits the current Listing Display properties
Smaller Font - Decreases the displayed font size
Larger Font - Increases the displayed font size
Search Backward - Moves to a previous data match
Define Search - Define data to be matched
Search Forward - Moves to the next data match
Mark Opcode - Permits placing an opcode mark (disabled in PCI64SW)



Sample	PCIX64 AD_Hi	PCIX64 AD_Lo	PCIX64 Mnemonics	Timestamp
6	00000000	F7FF0000	MEMORY WRITE ADDRESS	44.431,000 us
7	--------	060D0008	ATTRIBUTE CYCLE - DWORD	30.000 ns
	--------	060D0008	No Snoop = Not Set	
	--------	060D0008	Relaxed Ordering = Not Set	
	--------	060D0008	Tag = 0x006 / 0d6	
	--------	060D0008	Req. Bus #0x00D / 0d13	
	--------	060D0008	Req. Device #0x000 / 0d0	
	--------	060D0008	Req. Function #0x000 / 0d0	
	--------	060D0008	Byte Enables - Bytes 3-0	
8	--------	80140050	SINGLE DATA PHASE DISCONNECT	270.000 ns
9	00000000	F7FF0000	MEMORY WRITE ADDRESS	180.000 ns
10	--------	070D0008	ATTRIBUTE CYCLE - DWORD	30.000 ns
	--------	070D0008	No Snoop = Not Set	
	--------	070D0008	Relaxed Ordering = Not Set	
	--------	070D0008	Tag = 0x007 / 0d7	
	--------	070D0008	Req. Bus #0x00D / 0d13	
	--------	070D0008	Req. Device #0x000 / 0d0	
	--------	070D0008	Req. Function #0x000 / 0d0	
	--------	070D0008	Byte Enables - Bytes 3-0	
11	00000000	--------	SINGLE DATA PHASE DISCONNECT	270.000 ns
12	00000000	F7FF0008	MEMORY WRITE ADDRESS	180.000 ns
13	--------	040D0008	ATTRIBUTE CYCLE - DWORD	30.000 ns
	--------	040D0008	No Snoop = Not Set	
	--------	040D0008	Relaxed Ordering = Not Set	
	--------	040D0008	Tag = 0x004 / 0d4	
	--------	040D0008	Req. Bus #0x00D / 0d13	
	--------	040D0008	Req. Device #0x000 / 0d0	
	--------	040D0008	Req. Function #0x000 / 0d0	
	--------	040D0008	Byte Enables - Bytes 3-0	
14	--------	80F70050	SINGLE DATA PHASE DISCONNECT	270.000 ns
15	00000000	F7FF0008	MEMORY WRITE ADDRESS	180.000 ns
16	--------	050D0008	ATTRIBUTE CYCLE - DWORD	30.000 ns
	--------	050D0008	No Snoop = Not Set	
	--------	050D0008	Relaxed Ordering = Not Set	
	--------	050D0008	Tag = 0x005 / 0d5	

Figure 2- PCIX64 Disassembly

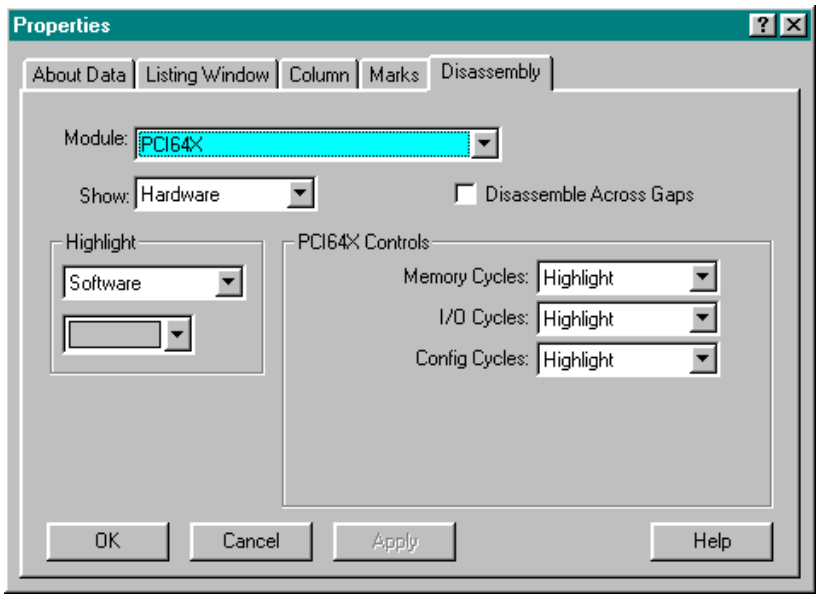


Figure 3- PCIX64 Cycle Filtering Window

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PCIX64 disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

APPENDIX A - Necessary Signals for Clocking

To properly acquire PCI-X bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, TRDY#, and STOP#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

APPENDIX B - Considerations

The NEX-PCIX is an extender card that is also designed to permit monitoring the PCI-X bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will violate the PCI-X specification for stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, series termination resistors have been added to each signal to reduce the electrical effect of the stub. The adapter design is also impedance controlled and matched trace length to maintain signal integrity

APPENDIX C – PCI-X Local Bus Pinout

Pin #	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
1	-12V	TRST#	
2	TCK	+12V	
3	Ground	TMS	
4	TDO	TDI	
5	+5V	+5V	
6	+5V	INTA#	
7	INTB#	INTC#	
8	INTD#	+5V	
9	PRSNT1#	Reserved	
10	Reserved	V(I/O)	
11	PRSNT2#	Reserved	
12	KEYWAY	KEYWAY	key
13	KEYWAY	KEYWAY	key
14	Reserved	AUX	
15	Ground	RST#	
16	CLK	V(I/O)	
17	Ground	GNT#	
18	REQ#	Ground	
19	+V I/O	PME	
20	AD[31]	AD[30]	
21	AD[29]	+3.3V	
22	Ground	AD[28]	
23	AD[27]	AD[26]	
24	AD[25]	Ground	
25	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	
28	Ground	AD[22]	
29	AD[21]	AD[20]	
30	AD[19]	Ground	
31	+3.3V	AD[18]	
32	AD[17]	AD[16]	

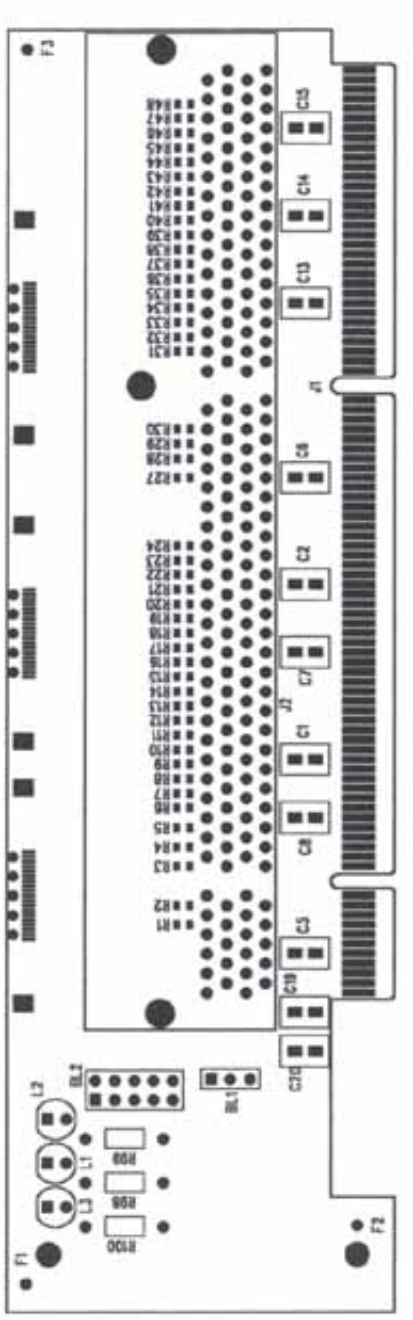
APPENDIX C – PCI-X Local Bus Pinout (cont'd.)

Pin #	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
33	C/BE[2]#	+3.3V	
34	Ground	FRAME#	
35	IRDY#	Ground	
36	+3.3V	TRDY#	
37	DEVSEL#	Ground	
38	PCIXCAP	STOP#	
39	LOCK#	+3.3V	
40	PERR#	SDONE	
41	+3.3V	SBO#	
42	SERR#	Ground	
43	+3.3V	PAR	
44	C/BE[1]#	AD[15]	
45	AD[14]	+3.3V	
46	Ground	AD[13]	
47	AD[12]	AD[11]	
48	AD[10]	Ground	
49	M66EN	AD[9]	
50	Ground	Ground	key
51	Ground	Ground	key
52	AD[8]	C/BE[0]#	
53	AD[7]	+3.3V	
54	+3.3V	AD[6]	
55	AD[5]	AD[4]	
56	AD[3]	Ground	
57	Ground	AD[2]	
58	AD[1]	AD[0]	
59	V(I/O)	V(I/O)	
60	ACK64#	REQ64#	
61	+5V	+5V	
62	+5V	+5V	

APPENDIX C – PCI-X Local Bus Pinout (cont'd.)

Pin #	+3.3V Side B Component Side	+3.3V Side A Solder Side	Comments
	KEYWAY	KEYWAY	
	KEYWAY	KEYWAY	
63	Reserved	Ground	
64	Ground	C/BE[7]#	
65	C/BE[6]#	C/BE[5]#	
66	C/BE[4]#	V(I/O)	
67	Ground	PAR64	
68	AD[63]	AD[62]	
69	AD[61]	Ground	
70	V(I/O)	AD[60]	
71	AD[59]	AD[58]	
72	AD[57]	Ground	
73	Ground	AD[56]	
74	AD[55]	AD[54]	
75	AD[53]	V(I/O)	
76	Ground	AD[52]	
77	AD[51]	AD[50]	
78	AD[49]	Ground	
79	V(I/O)	AD[48]	
80	AD[47]	AD[46]	
81	AD[45]	Ground	
82	Ground	AD[44]	
83	AD[43]	AD[42]	
84	AD[41]	V(I/O)	
85	Ground	AD[40]	
86	AD[39]	AD[38]	
87	AD[37]	Ground	
88	V(I/O)	AD[36]	
89	AD[35]	AD[34]	
90	AD[33]	Ground	
91	Ground	AD[32]	
92	Reserved	Reserved	
93	Reserved	Ground	
94	Ground	Reserved	

APPENDIX D - NEX-PCIX Outline



APPENDIX E - NEX-PCIX Mictor Pinout

Tek Mictor Pin #	AMP Mictor Pin #	TLA600 /700 Channel	PCI-X Signal Name	PCI-X Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600 /700 Channel	PCI-X Signal Name	PCI-X Pin #
3	5	CLK:0	CLK	B16	36	6	CLK:1	DEVSEL#	B37
4	7	A3:7	AD[31]	B20	35	8	A1:7	AD[15]	A44
5	9	A3:6	AD[30]	A20	34	10	A1:6	AD[14]	B45
6	11	A3:5	AD[29]	B21	33	12	A1:5	AD[13]	A46
7	13	A3:4	AD[28]	A22	32	14	A1:4	AD[12]	B47
8	15	A3:3	AD[27]	B23	31	16	A1:3	AD[11]	A47
9	17	A3:2	AD[26]	A23	30	18	A1:2	AD[10]	B48
10	19	A3:1	AD[25]	B24	29	20	A1:1	AD[9]	A49
11	21	A3:0	AD[24]	A25	28	22	A1:0	AD[8]	B52
12	23	A2:7	AD[23]	B27	27	24	A0:7	AD[7]	B53
13	25	A2:6	AD[22]	A28	26	26	A0:6	AD[6]	A54
14	27	A2:5	AD[21]	B29	25	28	A0:5	AD[5]	B55
15	29	A2:4	AD[20]	A29	24	30	A0:4	AD[4]	A55
16	31	A2:3	AD[19]	B30	23	32	A0:3	AD[3]	B56
17	33	A2:2	AD[18]	A31	22	34	A0:2	AD[2]	A57
18	35	A2:1	AD[17]	B32	21	36	A0:1	AD[1]	B58
19	37	A2:0	AD[16]	A32	20	38	A0:0	AD[0]	A58

Group A Mictor Connector

APPENDIX E - NEX-PCIX Mictor Pinout (cont'd.)

Tek Mictor Pin #	AMP Mictor Pin #	TLA600 /700 Channel	PCI-X Signal Name	PCI-X Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600 /700 Channel	PCI-X Signal Name	PCI-X Pin #
3	5	CLK:3	RST#	A15	36	6	QUAL:1	PCIXCAP	B38
4	7	C3:7	C/BE[7]#	A64	35	8	C1:7	unused	- - - - -
5	9	C3:6	C/BE[6]#	B65	34	10	C1:6	M66EN	B49
6	11	C3:5	C/BE[5]#	A65	33	12	C1:5	REQ64#	A60
7	13	C3:4	C/BE[4]#	B66	32	14	C1:4	PAR64	A67
8	15	C3:3	C/BE[3]#	B26	31	16	C1:3	unused	- - - - -
9	17	C3:2	C/BE[2]#	B33	30	18	C1:2	unused	- - - - -
10	19	C3:1	C/BE[1]#	B44	29	20	C1:1	unused	- - - - -
11	21	C3:0	C/BE[0]#	A52	28	22	C1:0	unused	- - - - -
12	23	C2:7	SBO#	A41	27	24	C0:7	ACK64#	B60
13	25	C2:6	LOCK#	B39	26	26	C0:6	GNT#	A17
14	27	C2:5	PERR#	B40	25	28	C0:5	REQ#	B18
15	29	C2:4	PAR	A43	24	30	C0:4	IDSEL	A26
16	31	C2:3	STOP#	A38	23	32	C0:3	INTD#	B08
17	33	C2:2	TRDY#	A36	22	34	C0:2	INTC#	A07
18	35	C2:1	IRDY#	B35	21	36	C0:1	INTB#	B07
19	37	C2:0	FRAME#	A34	20	38	C0:0	INTA#	A06

Group C Mictor Connector

APPENDIX E - NEX-PCIX Mictor Pinout (cont'd.)

Tek Mictor Pin #	AMP Mictor Pin #	TLA600 /700 Channel	PCI-X Signal Name	PCI-X Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA600 /700 Channel	PCI-X Signal Name	PCI-X Pin #
3	5	QUAL:0	SDONE	A40	36	6	CLK:2	SERR	B42
4	7	D3:7	AD[63]	B68	35	8	D1:7	AD[47]	B80
5	9	D3:6	AD[62]	A68	34	10	D1:6	AD[46]	A80
6	11	D3:5	AD[61]	B69	33	12	D1:5	AD[45]	B81
7	13	D3:4	AD[60]	A70	32	14	D1:4	AD[44]	A82
8	15	D3:3	AD[59]	B71	31	16	D1:3	AD[43]	B83
9	17	D3:2	AD[58]	A71	30	18	D1:2	AD[42]	A83
10	19	D3:1	AD[57]	B72	29	20	D1:1	AD[41]	B84
11	21	D3:0	AD[56]	A73	28	22	D1:0	AD[40]	A85
12	23	D2:7	AD[55]	B74	27	24	D0:7	AD[39]	B86
13	25	D2:6	AD[54]	A74	26	26	D0:6	AD[38]	A86
14	27	D2:5	AD[53]	B75	25	28	D0:5	AD[37]	B87
15	29	D2:4	AD[52]	A76	24	30	D0:4	AD[36]	A88
16	31	D2:3	AD[51]	B77	23	32	D0:3	AD[35]	B89
17	33	D2:2	AD[50]	A77	22	34	D0:2	AD[34]	A89
18	35	D2:1	AD[49]	B78	21	36	D0:1	AD[33]	B90
19	37	D2:0	AD[48]	A79	20	38	D0:0	AD[32]	A91

Group D Mictor Connector

APPENDIX F – NEX-PCI-X P6860 Compression Probe Pinout

For further information on the P6860 Connectorless probe compression footprint, please refer to the "P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual", Tektronix part number 071-1059-00.

Pad #	TLA Channel	PCI-X Signal Name	PCI-X Pin #
A15	CK1-	GND	- - - - -
A13	CK1+	DEVSEL#	B37
B12	A1:7	AD[15]	A44
B10	A1:6	AD[14]	B45
A12	A1:5	AD[13]	A46
A10	A1:4	AD[12]	B47
B9	A1:3	AD[11]	A47
B7	A1:2	AD[10]	B48
A9	A1:1	AD[9]	A49
A7	A1:0	AD[8]	B52
B6	A0:7	AD[7]	B53
B4	A0:6	AD[6]	A54
A6	A0:5	AD[5]	B55
A4	A0:4	AD[4]	A55
B3	A0:3	AD[3]	B56
B1	A0:2	AD[2]	A57
A3	A0:1	AD[1]	B58
A1	A0:0	AD[0]	A58

Probe Connection A0/A1

Pad #	TLA Channel	PCI-X Signal Name	PCI-X Pin #
A15	CK0-	GND	- - - - -
A13	CK0+	CLK	B16
B12	A3:7	AD[31]	B20
B10	A3:6	AD[30]	A20
A12	A3:5	AD[29]	B21
A10	A3:4	AD[28]	A22
B9	A3:3	AD[27]	B23
B7	A3:2	AD[26]	A23
A9	A3:1	AD[25]	B24
A7	A3:0	AD[24]	A25
B6	A2:7	AD[23]	B27
B4	A2:6	AD[22]	A28
A6	A2:5	AD[21]	B29
A4	A2:4	AD[20]	A29
B3	A2:3	AD[19]	B30
B1	A2:2	AD[18]	A31
A3	A2:1	AD[17]	B32
A1	A2:0	AD[16]	A32

Probe Connection A2/A3

APPENDIX F – NEX-PCI-X P6860 Compression Probe Pinout (cont'd.)

Pad #	TLA Channel	PCI-X Signal Name	PCI-X Pin #
A15	Q1-	GND	- - - - -
A13	Q1+	PCIXCAP	B38
B12	C1:7	unused	- - - - -
B10	C1:6	M66EN	B49
A12	C1:5	REQ64#	A60
A10	C1:4	PAR64	A67
B9	C1:3	unused	- - - - -
B7	C1:2	unused	- - - - -
A9	C1:1	unused	- - - - -
A7	C1:0	unused	- - - - -
B6	C0:7	ACK64#	B60
B4	C0:6	GNT#	A17
A6	C0:5	REQ#	B18
A4	C0:4	IDSEL	A26
B3	C0:3	INTD#	B08
B1	C0:2	INTC#	A07
A3	C0:1	INTB#	B07
A1	C0:0	INTA#	A06

Probe Connection C0/C1

Pad #	TLA Channel	PCI-X Signal Name	PCI-X Pin #
A15	CK3-	GND	- - - - -
A13	CLK3+	RST#	A15
B12	C3:7	C/BE[7]#	A64
B10	C3:6	C/BE[6]#	B65
A12	C3:5	C/BE[5]#	A65
A10	C3:4	C/BE[4]#	B66
B9	C3:3	C/BE[3]#	B26
B7	C3:2	C/BE[2]#	B33
A9	C3:1	C/BE[1]#	B44
A7	C3:0	C/BE[0]#	A52
B6	C2:7	SBO#	A41
B4	C2:6	LOCK#	B39
A6	C2:5	PERR#	B40
A4	C2:4	PAR	A43
B3	C2:3	STOP#	A38
B1	C2:2	TRDY#	A36
A3	C2:1	IRDY#	B35
A1	C2:0	FRAME#	A34

Probe Connection C2/C3

Pad #	TLA Channel	PCI-X Signal Name	PCI-X Pin #
A15	CK2-	GND	- - - - -
A13	CK2	SERR	B42
B12	D1:7	AD[47]	B80
B10	D1:6	AD[46]	A80
A12	D1:5	AD[45]	B81
A10	D1:4	AD[44]	A82
B9	D1:3	AD[43]	B83
B7	D1:2	AD[42]	A83
A9	D1:1	AD[41]	B84
A7	D1:0	AD[40]	A85
B6	D0:7	AD[39]	B86
B4	D0:6	AD[38]	A86
A6	D0:5	AD[37]	B87
A4	D0:4	AD[36]	A88
B3	D0:3	AD[35]	B89
B1	D0:2	AD[34]	A89
A3	D0:1	AD[33]	B90
A1	D0:0	AD[32]	A91

Probe Connection D0/D1

Pad #	TLA Channel	PCI-X Signal Name	PCI-X Pin #
A15	Q0-	GND	- - - - -
A13	Q0+	SDONE	A40
B12	D3:7	AD[63]	B68
B10	D3:6	AD[62]	A68
A12	D3:5	AD[61]	B69
A10	D3:4	AD[60]	A70
B9	D3:3	AD[59]	B71
B7	D3:2	AD[58]	A71
A9	D3:1	AD[57]	B72
A7	D3:0	AD[56]	A73
B6	D2:7	AD[55]	B74
B4	D2:6	AD[54]	A74
A6	D2:5	AD[53]	B75
A4	D2:4	AD[52]	A76
B3	D2:3	AD[51]	B77
B1	D2:2	AD[50]	A77
A3	D2:1	AD[49]	B78
A1	D2:0	AD[48]	A79

Probe Connection D2/D3

APPENDIX F - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: http://**www.nexustechnology.com**

Support Contact Information

Technical Support	**techsupport@nexustechnology.com**
General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX G - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

PCI Local Bus Specification
Production Version; Revision 2.1s - June 1, 1995
Published by:
PCI Special Interest Group
PO Box 14070
Portland OR 97214
800-433-5177 (U.S.)
503-797-4207 (International)
503-234-6762 (FAX)

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Production Version; Revision 1.0
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