



NEX-PMC
PMC Bus Adapter Users Manual
Including these Software Support packages:
PMC

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1.0 OVERVIEW

1.1 General Information

The NEX-PMC adapter has been designed to provide quick and easy connections to interface a 68-, 102-, or 136-channel TLA600/700, a 92A96 or a 92C96 acquisition module to a 32-bit PMC mezzanine card location. (The PMC designation refers to the PCI Mezzanine Card specification.) In addition, the method of connection permits the use of other acquisition cards, pattern generation cards or other measurement devices such as oscilloscopes.

The included NEX-PMC support software permits the acquisition of all PMC (PCI) bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. For instance, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA600/700 apply to a TLA704, TLA711, TLA714, TLA715, TLA720 or TLA721 chassis with one or more 7*2/3/4 acquisition cards.

This manual also assumes that the user is familiar with the PMC and PCI Local Bus specifications and the Tektronix TLA600/700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA600/700, it is expected that the user is familiar with M.S. Windows.

Appendix E is a silk-screen print of the NEX-PMC Adapter board. Referring to this drawing while reading the manual is suggested.

For information on using a Prism 32GPX/GPD module with this support, or if 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix F for contact information.

2.0 SOFTWARE INSTALLATION

One 3½” diskette has been included with the NEX-PMC Bus Adapter. It is used with the TLA600/700 series. Diskettes for the DAS9200 or TLA500 are available upon request. See Appendix F for contact information.

2.1 TLA600/700

The NEX-PMC software is loaded in the same manner as other Windows programs. Place the NEX-PMC Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the PMC support in its proper place on the hard disk.

To load PMC support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose PMC and click on **Okay**. Note that the Logic Analyzer card must be at least 68-channels in width.

2.1 DAS 9200/TLA510/TLA520

The included diskette should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing "PMC Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

3.0 CONNECTING to the NEX-PMC ADAPTER

3.1 General

The NEX-PMC adapter works as an extender for a PMC module. Easy probing of the PMC module under test is provided by extending the module beyond the front panel.

3.2 TLA600/700

When using a TLA600/700 with a 7*2/3/4 acquisition module, the necessary acquisition data sections are A0-A3, D0, D1, C2, and C3. These grouped channels (8 podlets to a group) should be connected to the locations denoted for the TLA. Follow the silk-screened information on the

board that shows the proper relationship between the signal and reference inputs. Note that the signal side of the podlets is the side with writing on it.

Connect the four clock leads to their specified locations at J1 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the TLA600/700 when used with the NEX-PMC adapter.

3.3 92A96

When using a 92A96, connect the grouped pods (8 podlets to a group) to their appropriate locations by following the silk-screen information printed on the adapter board. The 92A96 pods are labeled A0-A3, D0-D3, and C0-C3. Each pod has its proper location denoted on the silk-screen of the adapter board. When attaching the pods, follow the silk-screen information on the board showing the ground and signal pin locations. Note that the signal side of the podlets is the side with the color coding on it.

Connect the four clock leads (one per A96 cable) to their specified locations at J1 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the 92A96.

Group Name	Signal Name	PMC Pin #	92A96 input	TLA700 input	Group Name	Signal Name	PMC Pin #	92A96 input	TLA700 input
Addr/Dat	AD[31]	P1-20	A3:7	A3:7	Cmd/Size	DEVSEL#	P1-37	C3:0	D0:0
	AD[30]	P2-19	A3:6	A3:6		IRDY#	P1-36	C2:1	C2:1
	AD[29]	P2-20	A3:5	A3:5		TRDY#	P2-35	C2:2	C2:2
	AD[28]	P1-21	A3:4	A3:4		C/BE#[3]	P1-26	C2:7	C2:7
	AD[27]	P1-22	A3:3	A3:3		C/BE#[2]	P2-32	C2:6	C2:6
	AD[26]	P2-22	A3:2	A3:2		C/BE#[1]	P2-43	C2:5	C2:5
	AD[25]	P1-23	A3:1	A3:1		C/BE#[0]	P1-52	C2:4	C2:4
	AD[24]	P2-23	A3:0	A3:0	Control	TRST#	P2-2	C3:5	D0:5
	AD[23]	P2-26	A2:7	A2:7		GNT#	P1-16	C0:6	D1:6
	AD[22]	P1-27	A2:6	A2:6		STOP#	P2-38	C2:3	C2:3
	AD[21]	P1-28	A2:5	A2:5		LOCK#	P1-40	C3:4	D0:4
	AD[20]	P2-28	A2:4	A2:4		FRAME#	P1-33	C2:0	C2:0
	AD[19]	P1-29	A2:3	A2:3	IDSEL	P2-25	C0:4	D1:4	
	AD[18]	P2-29	A2:2	A2:2	Intrpt	INTD#	P1-9	C0:3	D1:3
	AD[17]	P1-32	A2:1	A2:1		INTC#	P1-6	C0:2	D1:2
	AD[16]	P2-31	A2:0	A2:0		INTB#	P1-5	C0:1	D1:1
	AD[15]	P1-46	A1:7	A1:7		INTA#	P1-4	C0:0	D1:0
	AD[14]	P2-45	A1:6	A1:6	Misc	REQ#	P1-17	C0:5	D1:5
	AD[13]	P2-46	A1:5	A1:5		PERR#	P2-39	C3:3	D0:3
	AD[12]	P1-47	A1:4	A1:4		PAR	P1-43	C3:2	D0:2
	AD[11]	P1-48	A1:3	A1:3		SERR#	P2-42	C3:1	D0:1
	AD[10]	P2-48	A1:2	A1:2	CLK	P1-13	C3:6	D0:6	
	AD[9]	P1-49	A1:1	A1:1	Aux_0	Aux_0:[7-0]	-----	D2	-----
	AD[8]	P2-49	A1:0	A1:0	Aux_1	Aux_1:[7-0]	-----	D3	-----
	AD[7]	P2-51	A0:7	A0:7					
	AD[6]	P1-53	A0:6	A0:6					
	AD[5]	P1-54	A0:5	A0:5					
	AD[4]	P1-55	A0:4	A0:4					
	AD[3]	P1-58	A0:3	A0:3	Clock:0	CLK=	P1-13		
	AD[2]	P1-59	A0:2	A0:2	Clock:1	unused	-----		
	AD[1]	P1-60	A0:1	A0:1	Clock:2	DEVSEL#=	P1-37		
AD[0]	P1-61	A0:0	A0:0	Clock:3	unused	-----			

Table 1- PMC TLA600 /700 / 92A96 Wiring

4.0 CLOCK SELECTION

4.1 General Information

There are three clocking options available when using the NEX-PMC support package. Each is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

When using a DAS9200 or TLA500, the clocking selection is made in the Clock menu. Open the select field labeled Clocking Select, choose the desired mode, then press <RETURN>.

4.2 Clocking Options - Explanation

Bus Cycle Acquisition - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge - In this mode, data will be acquired on every rising edge of the PMC (PCI) CLK signal. The disassembly will filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

5.0 VIEWING DATA

5.1 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PMC and PMC-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PMC-MagniVu, will show all of the channels in 2GHz/8GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

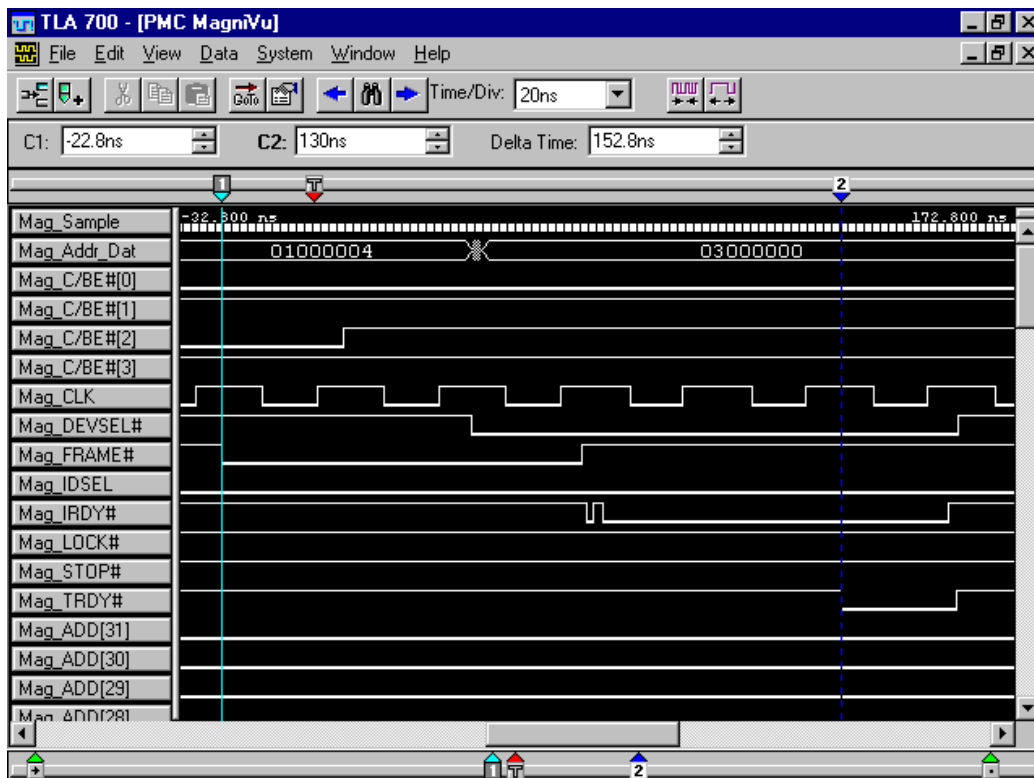


Figure 1- PMC MagniVu Display on TLA600/700

5.2 Viewing State Data on the DAS9200/TLA500

After an acquisition is made the DAS9200 Logic Analyzer will display the data in State Display mode (as a default only). Address / Data information is displayed in hexadecimal format; Control data is displayed using symbols; Interrupt, Miscellaneous, and both Auxiliary data groups default to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. A symbol table (PMC_Ctrl, Table 2) has been provided to show the type of transaction that occurred on the PMC (PCI) bus. This symbol table quickly shows whether the acquisition was a memory or I/O operation, a read or a write, etc.

It is important to note that changing the group, channel, or wiring of the Control group can result in incorrect symbol information being displayed.

5.3 Viewing Timing Data on the DAS9200/TLA500

It may be useful to display acquired information using the Timing Diagram display of the DAS9200. (Note that, unlike some other logic analyzers, with the DAS9200 there is no need to re-acquire PMC data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the DAS9200 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

Pattern	TLA600/700 / 92A96 Symbols	Meaning
0xxxxxxxxx	RESET	Reset
1011110000	INTERRUPT ACK	Interrupt Acknowledge
1011110001	SPECIAL CYCLE	Special Cycle
1011110010	I/O READ ADDRESS	I/O Read
1011110011	I/O WRITE ADDRESS	I/O Write
101111010x	RESERVED	Reserved
1011110110	MEMORY READ ADDRESS	Memory Read
1011110111	MEMORY WRITE ADDRESS	Memory Write
101111100x	RESERVED	Reserved
1011111010	CONFIG READ ADDRESS	Configuration Read
1011111011	CONFIG WRITE ADDRESS	Configuration Write
1011111100	MEMORY READ MULTIPLE	Memory Read Multiple
1011111101	DUAL ADDRESS	Dual Address Cycle
1011111110	MEMORY READ LINE	Memory Read Line
1011111111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
111101xxxx	WAIT/MASTER ABORT	Wait or Master Abort
110101xxxx	TARGET ABORT	Target Abort
110001xxxx	RETRY	Retry Cycle
1x0x001110	DATA - BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA - BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA - BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA - BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA - BYTES 0 & 1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA - BYTES 2 & 3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA - BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo

Table 2- PMC Control Symbol Table

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#,
C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

6.0 USING THE DISASSEMBLY SOFTWARE

6.1 General

The NEX-PMC support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PMC (PCI) Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the NEX-PMC software is its ability to intelligently acquire PMC data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the PMC software is able to acquire only the PMC (PCI) bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.3 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 125ps/500ps in the TLA600/700 series, and to 10ns in the DAS9200 / TLA500, permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

6.2 Disassembly Using the TLA600/700

The TLA600/700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window

Sample	PMC Addr_Dat	PMC Mnemonics	Timestamp
	03000043	Class 0x03 - Display controller	
	03000043	Sub-Class 0x00	
	03000043	Prog. I/F 0x00 - VGA compatible	
	03000043	Revision ID 67	
814	000C0000	MEMORY READ ADDRESS	23.106,000 us
815	----FFFF	MEMORY READ DATA	2.076,000 us
816	00000CF8	I/O WRITE ADDRESS	14.941,793,000 ns
817	80006804	I/O WRITE DATA	90.000 ns
818	01000004	CONFIG READ ADDRESS	1.685,000 us
	01000004	Type 0 Register 1 Function 0	
819	-----00	CONFIG READ DATA	150.000 ns
	-----00	Wait Cycle disabled	
	-----00	Parity Errors disabled	
	-----00	VGA Palette Snoop disabled	
	-----00	Mem Write & Inv. disabled	
	-----00	Special Cycle Recog. disabled	
	-----00	Master disabled	
	-----00	Memory Access disabled	
	-----00	I/O Access disabled	
820	00000CF8	I/O WRITE ADDRESS	13.451,000 us
821	80006804	I/O WRITE DATA	90.500 ns
822	01000004	CONFIG WRITE ADDRESS	1.684,500 us
	01000004	Type 0 Register 1 Function 0	

Figure 2- PMC Disassembly

Sample	PMC Addr_Dat	PMC Mnemonics	Timestamp
	03000043	Revision ID 67	
818	01000004	CONFIG READ ADDRESS	14.968,750,000 ns
	01000004	Type 0 Register 1 Function 0	
819	-----00	CONFIG READ DATA	150.000 ns
	-----00	Wait Cycle disabled	
	-----00	Parity Errors disabled	
	-----00	VGA Palette Snoop disabled	
	-----00	Mem Write & Inv. disabled	
	-----00	Special Cycle Recog. disabled	
	-----00	Master disabled	
	-----00	Memory Access disabled	
	-----00	I/O Access disabled	
822	01000004	CONFIG WRITE ADDRESS	15.226,000 us
	01000004	Type 0 Register 1 Function 0	
823	-----02	CONFIG WRITE DATA	151.000 ns
	-----02	Wait Cycle disabled	
	-----02	Parity Errors disabled	
	-----02	VGA Palette Snoop disabled	
	-----02	Mem Write & Inv. disabled	
	-----02	Special Cycle Recog. disabled	
	-----02	Master disabled	
	-----02	Memory Access enabled	
	-----02	I/O Access disabled	

Figure 3- PMC Disassembly with suppressed Memory and I/O Cycles

contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark (disabled in PMC support)

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PMC disassembly information is displayed. As mentioned previously, it is possible to choose which PMC (PCI) cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

6.3 Disassembly Using the DAS9200 / TLA500

To view PMC data in Disassembly form, simply click on the DISASM button in the lower part of the DAS/TLA display, or select Disasm in the Display column of the Main Menu. All PMC (PCI) transactions will be displayed and disassembled, and the Timestamp between each acquisition is displayed (Relative mode). To change the Timestamp format, press (or click) **F5** (Display Format) and open the Timestamp select field. The options available are: Relative (time from the previous sample), Delta (time from a user definable Delta mark), Absolute (time from when the acquisition card was started), and Off. Making a choice, closing the field, then pressing (or clicking) **F8** to Exit and Save will modify the Disassembly display appropriately.

To filter the displayed data, again move to the Display Format screen (press or click **F5**). The Hardware Display Mode (default) will display all PCI cycles by default.

By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Display Mode select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Display Mode select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Relative form) will be updated to show the time between displayed cycles.

APPENDIX A - Necessary Signals for Clocking

To properly acquire PMC bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

APPENDIX B - Considerations

B.1 PMC Loading

It must be noted that the NEX-PMC Bus Adapter does not provide any buffering of the PMC backplane signals. This was a conscious design decision that was made by balancing the tradeoffs of possible backplane loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-PMC adapter, to see the exact timing relationships and signal waveforms from the backplane. It is also much easier to connect pattern generators to the backplane since buffer direction is not a concern. It is believed that the signal loading of the TLA600/700 or 92A96 acquisition cards is low enough so that PMC signal degradation will not occur.

B.2 Pattern Generation

Because there is no buffer circuitry on the NEX-PMC Adapter, it is well suited for use with the 92S16 and 92S32 Pattern Generator modules available for the DAS 9200. By connecting pattern generator probes to the A96 signal connectors on the Adapter, desired bus activity can be simulated. This can be particularly effective when trying to debug interrupt or DMA conflicts.

It should be noted that, because of the pin spacing of the A96 connectors, it is not recommended that the Tektronix P6464 or P6465 pattern generator probes be used without adequately cooling their podlets. These probes use active podlets that can get very warm in use. A better choice would be the P6463 pods which do not have such cooling requirements.

APPENDIX C - Modifying the NEX-PMC Adapter

To monitor additional signals, the method is fairly simple. All PMC signals have been brought out to feed-throughs on the board, and there is one unused TLA600/700/A96 connectors on the board. This connector has feed-throughs near it to provide easy solder points. Use wire wrap wire to connect the PMC signals to these connectors.

APPENDIX D - PMC Pinout

Pin #	Signal Name	Signal Name	Pin #
1	TCK	-12	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE#1	+5V	8
9	INTD#	Reserved	10
11	Ground	Reserved	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19	V (I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V (I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	V (I/O)]	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64

P1/J1 Connectors

Pin #	Signal Name	Signal Name	Pin #
1	+12V	TRST#	2
3	TMT	TDO	4
5	TDI	GROUND	6
7	GROUND	RESERVED	8
9	RESERVED	RESERVED	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE#3	14
15	3.3V	BUSMODE#4	16
17	RESERVED	GROUND	18
19	AD[30]	AD[29]	20
21	GROUND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GROUND	30
31	AD[16]	C/BE[2]#	32
33	GROUND	RESERVED	34
35	TRDY#	+3.3V	36
37	GROUND	STOP#	38
39	PERR#	GROUND	40
41	+3.3V	SERR#	42
43	C/BE[1]#	GROUND	44
45	AD[14]	AD[13]	46
47	GROUND	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	RESERVED	52
53	+3.3V	RESERVED	54
55	RESERVED	GROUND	56
57	RESERVED	RESERVED	58
59	GROUND	RESERVED	60
61	ACK64#	+3.3V	62
63	GROUND	RESERVED	64

P2/J2 Connectors

Pin #	Signal Name	Signal Name	Pin #
1	I/O	I/O	2
3	I/O	I/O	4
5	I/O	I/O	6
7	I/O	I/O	8
9	I/O	I/O	10
11	I/O	I/O	12
13	I/O	I/O	14
15	I/O	I/O	16
17	I/O	I/O	18
19	I/O	I/O	20
21	I/O	I/O	22
23	I/O	I/O	24
25	I/O	I/O	26
27	I/O	I/O	28
29	I/O	I/O	30
31	I/O	I/O	32
33	I/O	I/O	34
35	I/O	I/O	36
37	I/O	I/O	38
39	I/O	I/O	40
41	I/O	I/O	42
43	I/O	I/O	44
45	I/O	I/O	46
47	I/O	I/O	48
49	I/O	I/O	50
51	I/O	I/O	52
53	I/O	I/O	54
55	I/O	I/O	56
57	I/O	I/O	58
59	I/O	I/O	60
61	I/O	I/O	62
63	I/O	I/O	64

P4/J4 Connectors

APPENDIX F

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX G - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Module User's Manual

Tektronix DAS 9200 System User's Manual

Tektronix DAS 9200 92A96 User's Manual

Draft Standard for a Common Mezzanine Card Family: CMC
IEEE P1386 / Draft 2.0 April 4, 1995

Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC
IEEE P1386.1 / Draft 2.0 April 4, 1995

PCI Local Bus Specification
Revision 2.1 June 1, 1995