



NEX-PMC64

PMC Bus Adapter Users Manual

Including these Software Support packages:
PMC64 PMC32

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1.0 OVERVIEW

1.1 General Information

The NEX-PMC64 adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA600/700, acquisition module to a 32 or 64-bit PMC/PCI backplane. (The PCI designation refers to the Peripheral Component Interconnect Local Bus specification.) Connections are made through P6434 Mass Termination probes available from Tektronix.

The NEX-PMC64 adapter supports 3.3V and 5V PMC applications.

The included NEX-PMC64 and NEX-PMC32 software permits the acquisition of all PCI bus cycles, ignoring all Wait and Idle cycles (although it is possible to acquire these cycles if desired). The software also post-processes the information to give the user complete disassembly of the bus transactions. Instead of simply viewing the data in raw form, all cycles are evaluated and, in the case of any Configuration transactions, complete information on the type of transaction is displayed in easy-to-read form.

Please note that this manual uses some terms generically. References to the TLA600/700 apply to a TLA704, 711, 714, 715, 720 or 721 chassis with one or more 7*3/4 acquisition cards.

Appendix D is a silk-screen print of the NEX-PMC64 Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the PCI Local Bus specification and the Tektronix TLA600/700 Logic Analyzer. Also, in the case of the TLA600/700, it is expected that the user is familiar with M.S. Windows.

2.0 SOFTWARE INSTALLATION

Two 3½” diskettes have been included with the NEX-PMC64 Bus Adapter. One is for 64-bit PMC/PCI (PMC64) and the other is for 32-bit PMC/PCI (PMC32).

2.1 TLA600/700

The NEX-PMC64 / NEX-PMC32 software is loaded in the same method as other Windows programs. Place the appropriate Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the PMC64 or PMC32 support in its proper place on the hard disk.

To load PMC64 or PMC32 support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose PMC64 or PMC32 and click on **Okay**.

3.0 CONFIGURING the NEX-PMC64 BUS ADAPTER

3.1 General Information

Not all PCI signals are monitored by the TLA600/700. (Refer to Table 1 or Table 2 for a list of acquired signals.)

Use the supplied jumper to short or break the connection between TDI and TDO (JP1). If the target card does not support JTAG Boundary Scan then the two pins should be shorted together.

4.0 CONNECTING to the NEX-PMC64 ADAPTER

4.1 General

The NEX-PMC64 is an extender card that is also designed to permit monitoring the PMC/PCI bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender adds stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, stub resistors have been added to all signals routed to mictor pins to isolate the effects of the stub. It is entirely possible, however, that placing a target card onto the NEX-PMC64 extender will result in improper operation of the target card or the target system.

4.2 TLA600/700 - 64-bit Operation

To use a TLA600/700 with the NEX-PMC64 adapter board it is necessary to use the P6434/P6860 high-density probes for connecting to the board. Each P6434/P6860 probe consists of one high-density probe tip (which connects to the adapter board) and two module ends (which connect to the acquisition card). It is important to note that where the module ends connect to the acquisition card will depend on how many channels the acquisition card has. Be very careful in noting where Pin 1 is on each probe tip, and follow the P6434 Mass Termination Probe manual or P6860 Compression Probe manual for instructions on applying the labels.

When using a 7*3/4 102/136-channel acquisition module for 64-bit support, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. One P6434/P6860 plugs onto the Group A connector on the PMC64 and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434/P6860 plugs onto the Group C connector on the PMC64 and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. The third P6434/P6860 plugs onto the Group D connector on the PMC64 and then connects to the Yellow (D0 and D1) and Blue (D2 and D3) locations on the acquisition card. Table 1 shows the wiring and Channel Grouping for the 102/136-channel TLA600/700 NEX-PMC64 connection.

4.3 TLA600/700 - 32-bit Operation

For 32-bit support with the NEX-PMC64 the necessary acquisition data sections are A0-A3 and C0-C3. One P6434/P6860 plugs onto the Group A connector on the PMC64 and then connects to the Orange (A0 and A1) and Tan (A2 and A3) locations on the acquisition card. The second P6434/P6860 plugs onto the Group C connector on the PMC64 and then connects to the Gray (C0 and C1) and White (C2 and C3) locations on the acquisition card. Table 2 shows the 32-bit wiring and Channel Grouping for the 102/136-channel TLA600/700 NEX-PMC64 connection.

Group Name	Signal Name	PMC Pin #	TLA600/700 input	Group Name	Signal Name	PMC Pin #	TLA600/700 input
AD_Hi (Hex)	AD[63]	Jn3-11	D3:7	AD_Lo (Hex)	AD[31]	Jn1-20	A3:7
	AD[62]	Jn3-12	D3:6		AD[30]	Jn2-19	A3:6
	AD[61]	Jn3-13	D3:5		AD[29]	Jn2-20	A3:5
	AD[60]	Jn3-16	D3:4		AD[28]	Jn1-21	A3:4
	AD[59]	Jn3-17	D3:3		AD[27]	Jn1-22	A3:3
	AD[58]	Jn3-18	D3:2		AD[26]	Jn2-22	A3:2
	AD[57]	Jn3-19	D3:1		AD[25]	Jn1-23	A3:1
	AD[56]	Jn3-22	D3:0		AD[24]	Jn2-23	A3:0
	AD[55]	Jn3-23	D2:7		AD[23]	Jn2-26	A2:7
	AD[54]	Jn3-24	D2:6		AD[22]	Jn1-27	A2:6
	AD[53]	Jn3-25	D2:5		AD[21]	Jn1-28	A2:5
	AD[52]	Jn3-28	D2:4		AD[20]	Jn2-28	A2:4
	AD[51]	Jn3-29	D2:3		AD[19]	Jn1-29	A2:3
	AD[50]	Jn3-30	D2:2		AD[18]	Jn2-29	A2:2
	AD[49]	Jn3-31	D2:1		AD[17]	Jn1-32	A2:1
	AD[48]	Jn3-34	D2:0		AD[16]	Jn2-31	A2:0
	AD[47]	Jn3-35	D1:7		AD[15]	Jn1-46	A1:7
	AD[46]	Jn3-36	D1:6		AD[14]	Jn2-45	A1:6
	AD[45]	Jn3-37	D1:5		AD[13]	Jn2-46	A1:5
	AD[44]	Jn3-40	D1:4		AD[12]	Jn1-47	A1:4
	AD[43]	Jn3-41	D1:3		AD[11]	Jn1-48	A1:3
	AD[42]	Jn3-42	D1:2		AD[10]	Jn2-48	A1:2
	AD[41]	Jn3-43	D1:1		AD[9]	Jn1-49	A1:1
	AD[40]	Jn3-46	D1:0		AD[8]	Jn2-49	A1:0
	AD[39]	Jn3-47	D0:7		AD[7]	Jn2-51	A0:7
	AD[38]	Jn3-48	D0:6		AD[6]	Jn1-53	A0:6
	AD[37]	Jn3-49	D0:5		AD[5]	Jn1-54	A0:5
	AD[36]	Jn3-52	D0:4		AD[4]	Jn1-55	A0:4
	AD[35]	Jn3-53	D0:3		AD[3]	Jn1-58	A0:3
	AD[34]	Jn3-54	D0:2		AD[2]	Jn1-59	A0:2
	AD[33]	Jn3-55	D0:1		AD[1]	Jn1-60	A0:1
	AD[32]	Jn3-58	D0:0		AD[0]	Jn1-61	A0:0

Table 1- NEX-PMC64 TLA600/700 (102/136-channel) Wiring

Note: All signals listed above are required for proper disassembly

Group Name	Signal Name	PMC Pin #	TLA600/700 input	Group Name	Signal Name	PMC Pin #	TLA600/700 input
Control (Sym)	RST#	Jn2-13	+ C3:5	Intrpt (Off)	INTD#	Jn1-9	C0:3
	REQ64#	Jn1-64	+ C1:0		INTC#	Jn1-6	C0:2
	ACK64#	Jn2-61	+ C1:1		INTB#	Jn1-5	C0:1
	FRAME#	Jn1-33	+ C2:0		INTA#	Jn1-4	C0:0
	DEVSEL#	Jn1-37	+ C3:0	Misc (Off)	REQ#	Jn1-17	C0:5
	STOP#	Jn2-38	+ C2:3		GNT#	Jn1-16	C0:6
	IRDY#	Jn1-36	+ C2:1		LOCK#	Jn1-40	C3:4
	TRDY#	Jn2-35	+ C2:2		IDSEL	Jn2-25	C0:4
	C/BE#[7]	Jn3-4	+ C1:7		PERR#	Jn2-39	C3:3
	C/BE#[6]	Jn3-5	+ C1:6		PAR	Jn1-43	C3:2
	C/BE#[5]	Jn3-6	+ C1:5	SERR#	Jn2-42	C3:1	
	C/BE#[4]	Jn3-7	+ C1:4	CLK	Jn1-13	C3:7	
	C/BE#[3]	Jn1-26	+ C2:7	Ungrouped	SDONE	Jn1-41	C3:6
	C/BE#[2]	Jn2-32	+ C2:6		SBO#	Jn1-42	C1:3
	C/BE#[1]	Jn2-43	+ C2:5		M66EN		C0:7
	Busmode	C/BE#[0]	Jn1-52	+ C2:4	Clock:0		
Busmode1#		Jn1-7	CLK:0	Clock:1	DEVSEL# =	Jn1-37	+
Busmode2#		Jn2-11	Qual:1	Clock:2			
Busmode3#		Jn2-14	Qual:0	Clock:3	CLK =	Jn1-13	+
Busmode4#	Jn2-16	CLK:2					

Table 1 - NEX-PMC64 TLA600/700 (102/136-channel) Wiring (cont'd.)

Note: Signals with a '+' are required for proper clocking / disassembly

Group Name	Signal Name	PMC Pin #	TLA600/700 input	Group Name	Signal Name	PMC Pin #	TLA600/700 input
Addr_Dat (Hex)	AD[31]	Jn1-20	+ A3:7	Control (Sym)	RST#	Jn2-13	+ C3:5
	AD[30]	Jn2-19	+ A3:6		FRAME#	Jn1-33	+ C2:0
	AD[29]	Jn2-20	+ A3:5		DEVSEL#	Jn1-37	+ C3:0
	AD[28]	Jn1-21	+ A3:4		STOP#	Jn2-38	+ C2:3
	AD[27]	Jn1-22	+ A3:3		IRDY#	Jn1-36	+ C2:1
	AD[26]	Jn2-22	+ A3:2		TRDY#	Jn2-35	+ C2:2
	AD[25]	Jn1-23	+ A3:1		C/BE#[3]	Jn1-26	+ C2:7
	AD[24]	Jn2-23	+ A3:0		C/BE#[2]	Jn2-32	+ C2:6
	AD[23]	Jn2-26	+ A2:7		C/BE#[1]	Jn2-43	+ C2:5
	AD[22]	Jn1-27	+ A2:6	C/BE#[0]	Jn1-52	+ C2:4	
	AD[21]	Jn1-28	+ A2:5	Intrpt (Off)	INTD#	Jn1-9	C0:3
	AD[20]	Jn2-28	+ A2:4		INTC#	Jn1-6	C0:2
	AD[19]	Jn1-29	+ A2:3		INTB#	Jn1-5	C0:1
	AD[18]	Jn2-29	+ A2:2		INTA#	Jn1-4	C0:0
	AD[17]	Jn1-32	+ A2:1	Misc (Off)	REQ#	Jn1-17	C0:5
	AD[16]	Jn2-31	+ A2:0		GNT#	Jn1-16	C0:6
	AD[15]	Jn1-46	+ A1:7		LOCK#	Jn1-40	C3:4
	AD[14]	Jn2-45	+ A1:6		IDSEL	Jn2-25	C0:4
	AD[13]	Jn2-46	+ A1:5		PERR#	Jn2-39	C3:3
	AD[12]	Jn1-47	+ A1:4		PAR	Jn1-43	C3:2
	AD[11]	Jn1-48	+ A1:3		SERR#	Jn2-42	C3:1
AD[10]	Jn2-48	+ A1:2	CLK	Jn1-13	C3:7		
AD[9]	Jn1-49	+ A1:1	Ungrouped	SDONE	Jn1-41	C3:6	
AD[8]	Jn2-49	+ A1:0		SBO#	Jn1-42	C1:3	
AD[7]	Jn2-51	+ A0:7		ACQ64#	Jn2-61	C1:1	
AD[6]	Jn1-53	+ A0:6		REQ64#	Jn1-64	C1:0	
AD[5]	Jn1-54	+ A0:5		M66EN		C0:7	
AD[4]	Jn1-55	+ A0:4	Clock:0 Clock:1 Clock:2 Clock:3				
AD[3]	Jn1-58	+ A0:3		DEVSEL#=	Jn1-37	+	
AD[2]	Jn1-59	+ A0:2		CLK=	Jn1-13	+	
AD[1]	Jn1-60	+ A0:1					
AD[0]	Jn1-61	+ A0:0					
Busmode	Busmode1#	Jn1-7		CLK:0			
	Busmode2#	Jn2-11		Qual:1			
	Busmode3#	Jn2-14	Qual:0				
	Busmode4#	Jn2-16	CLK:2				

Table 2- NEX-PMC64 32-bit TLA600/700 (102/136-channel) Wiring

Note: Signals with a '+' are required for proper clocking / disassembly

5.0 CLOCK SELECTION

5.1 General Information

There are three clocking options available when using either the NEX-PMC64 or NEX-PMC32 support package. Each selection is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.2 Clocking Options - Explanation

Bus Cycle Acquisition - This is the default clocking selection. In this mode only one address cycle is expected. All Wait and Idle states are ignored. In this clocking mode the High Address cycle of a Dual Address cycle will *not* be acquired as it will be considered a Wait state. The Low Address portion of the cycle will be properly acquired and displayed, as will all data associated with the cycle. This clocking selection offers the best use of your acquisition memory by ignoring all Wait and Idle states. Data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for bus cycle acquisitions to be made properly.

Dual Address Capable (32-bit only) - In this mode, both the Low Address and High Address parts of a Dual Address Cycle will be acquired. However, because of the clocking algorithm used, a Wait state immediately following a valid Address cycle will be acquired as well. The disassembly software will properly distinguish between a Wait cycle and the High Address portion of a Dual Address cycle, and will label each appropriately. As with Bus Cycle Acquisition, data is acquired on the rising edge of CLK, with DEVSEL#, FRAME#, IRDY#, and TRDY# used as qualifiers to determine when valid information is present. These signals must be present for this mode to properly acquire data.

Every CLK Rising Edge - In this mode, data will be acquired on every rising edge of the PCI CLK signal. The disassembly will filter and display these cycles accordingly, incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows *all* bus cycles, including Wait and Idle states. Since no clocking qualification is done only the CLK signal is required.

6.0 VIEWING DATA

6.1 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: PMC64 and PMC64-MagniVu (or PMC32 and PMC32-MagniVu when using 32-bit support). The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, PMC64-MagniVu (or PMC32-MagniVu), will show all of the channels in 2GHz/8GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

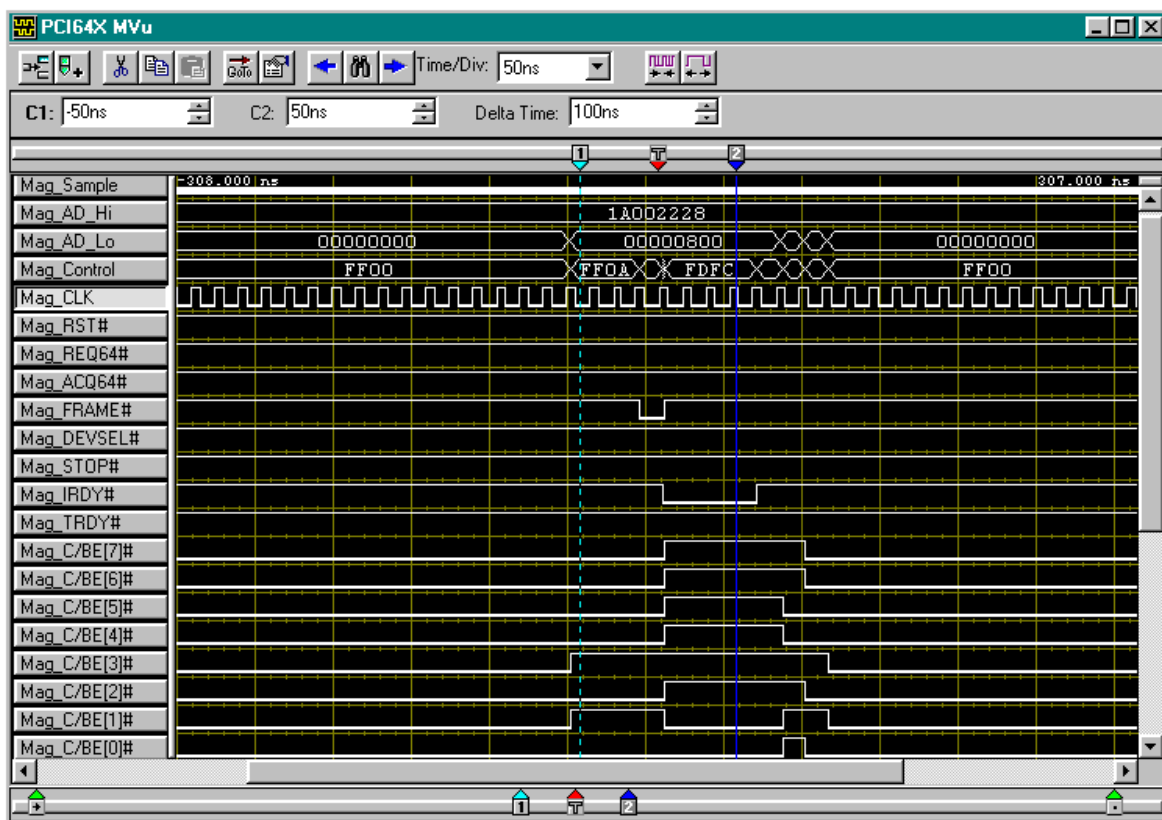


Figure 1- PMC64 MagniVu Display on TLA600/700

Pattern	TLA600/700 Symbols	Meaning
0xxxxxxxxxxxx	RESET	Reset
101111xxxx0000	INTERRUPT ACK	Interrupt Acknowledge
101111xxxx0001	SPECIAL CYCLE	Special Cycle
101111xxxx0010	I/O READ ADDRESS	I/O Read
101111xxxx0011	I/O WRITE ADDRESS	I/O Write
101111xxxx010x	RESERVED	Reserved
101111xxxx0110	MEMORY READ ADDRESS	Memory Read
101111xxxx0111	MEMORY WRITE ADDRESS	Memory Write
101111xxxx100x	RESERVED	Reserved
101111xxxx1010	CONFIG READ ADDRESS	Configuration Read
101111xxxx1011	CONFIG WRITE ADDRESS	Configuration Write
101111xxxx1100	MEMORY READ MULTIPLE	Memory Read Multiple
101111xxxx1101	DUAL ADDRESS	Dual Address Cycle
101111xxxx1110	MEMORY READ LINE	Memory Read Line
101111xxxx1111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
111101xxxxxxxx	WAIT/MASTER ABORT	Wait or Master Abort
111001xxxxxxxx	TARGET ABORT	Target Abort
110001xxxxxxxx	RETRY	Retry Cycle
1x0x0011111110	BYTE 0	Byte 0 valid (D0-7)
1x0x0011111101	BYTE 1	Byte 1 valid (D8-15)
1x0x0011111011	BYTE 2	Byte 2 valid (D16-23)
1x0x0011110111	BYTE 3	Byte 3 valid (D24-31)
1x0x0011101111	BYTE 4	Byte 4 valid (D32-39)
1x0x0011011111	BYTE 5	Byte 5 valid (D40-47)
1x0x0010111111	BYTE 6	Byte 6 valid (D48-55)
1x0x0001111111	BYTE 7	Byte 7 valid (D56-63)
1x0x0011111100	BYTES 0,1	Bytes 0 & 1 valid (D0-15)
1x0x0011110011	BYTES 2,3	Bytes 2 & 3 valid (D16-31)
1x0x0011001111	BYTES 4,5	Bytes 4 & 5 valid (D32-47)
1x0x0000111111	BYTES 6,7	Bytes 6 & 7 valid (D48-63)
1x0x0011110000	BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x0000001111	BYTES 4-7	Bytes 4-7 valid (D32-63)
1x0x0000000000	BYTES 0-7	Bytes 0-3 valid (D0-63)
1x0x0011111111	INVALID DATA	Invalid Data
11xxxxxxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxxxxxx	FRAME LO	Frame Lo

Table 3- PMC64_Ctrl Contol Symbol Table

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#, C/BE#[7], C/BE#[6], C/BE#[5], C/BE#[4], C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

Pattern	TLA600/700 Symbols	Meaning
0xxxxxxxxx	RESET	Reset
1011110000	INTERRUPT ACK	Interrupt Acknowledge
1011110001	SPECIAL CYCLE	Special Cycle
1011110010	I/O READ ADDRESS	I/O Read
1011110011	I/O WRITE ADDRESS	I/O Write
101111010x	RESERVED	Reserved
1011110110	MEMORY READ ADDRESS	Memory Read
1011110111	MEMORY WRITE ADDRESS	Memory Write
101111100x	RESERVED	Reserved
1011111010	CONFIG READ ADDRESS	Configuration Read
1011111011	CONFIG WRITE ADDRESS	Configuration Write
1011111100	MEMORY READ MULTIPLE	Memory Read Multiple
1011111101	DUAL ADDRESS	Dual Address Cycle
1011111110	MEMORY READ LINE	Memory Read Line
1011111111	MEMORY WRITE & INVALIDATE	Memory Write & Invalidate
111101xxxx	WAIT/MASTER ABORT	Wait or Master Abort
111001xxxx	TARGET ABORT	Target Abort
110001xxxx	RETRY	Retry Cycle
1x0x001110	DATA - BYTE 0	Byte 0 valid (D0-7)
1x0x001101	DATA - BYTE 1	Byte 1 valid (D8-15)
1x0x001011	DATA - BYTE 2	Byte 2 valid (D16-23)
1x0x000111	DATA - BYTE 3	Byte 3 valid (D24-31)
1x0x001100	DATA - BYTES 0 & 1	Bytes 0 & 1 valid (D0-15)
1x0x000011	DATA - BYTES 2 & 3	Bytes 2 & 3 valid (D16-31)
1x0x000000	DATA - BYTES 0-3	Bytes 0-3 valid (D0-31)
1x0x001111	INVALID DATA	Invalid Data
11xxxxxxxx	FRAME HI	Frame Hi
10xxxxxxxx	FRAME LO	Frame Lo

Table 4- PMC32_Ctrl Control Symbol Table

Signals, from left to right: RST#, FRAME#, STOP#, DEVSEL#, IRDY#, TRDY#,
C/BE#[3], C/BE#[2], C/BE#[1], C/BE#[0]

7.0 USING the DISASSEMBLY SOFTWARE

7.1 General

The PMC64 and PMC32 support software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler (see Figure 2). All PCI Cycle types are identified and Config Cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text. Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE Disk, Video controller, network interface, etc.) is being accessed. The C/BE bus signals are also monitored to determine which data bytes are valid for any given transaction. Invalid bytes are indicated by dashes in the display, making it much easier for the designer to determine what data is actually present on the bus at any given time.

It is also possible to filter the data display to show only those cycle types of interest (Figure 3). The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest.

Another feature of the PMC64 and PMC32 software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the PMC64 / PMC32 software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes, the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or rising clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 125ps/500ps in the TLA600/700 permits precise measurements of bus throughput during burst read transactions, etc. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Using the TLA600/700

The TLA600/700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window

Sample	PCI64X AD_Hi	PCI64X AD_Lo	PCI64X Mnemonics	Timestamp
	-----	FFFE0000	Memory Not Prefetchable	
	-----	FFFE0000	Decoder for 128KB Memory Space	
438	-----	04000010	CONFIG WRITE ADDRESS	6.904,570,000 ms
	-----	04000010	Type 0 Register 4 Function 0	
439	-----	00000000	CONFIG WRITE DATA	6.904,600,000 ms
	-----	00000000	Write to Base Address Register 0	
440	-----	04000008	CONFIG READ ADDRESS	6.908,491,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
441	-----	03000002	CONFIG READ DATA	6.908,536,500 ms
	-----	03000002	Class 0x03 - Display controller	
	-----	03000002	Sub-Class 0x00	
	-----	03000002	Prog. I/F 0x00 - VGA compatible	
	-----	03000002	Revision ID 2	
442	-----	04000010	CONFIG READ ADDRESS	6.937,764,500 ms
	-----	04000010	Type 0 Register 4 Function 0	
443	-----	-----00	CONFIG READ DATA	6.937,809,000 ms
	-----	-----00	Invalid Base Address data	
	-----	-----00	Base Address Register 0	
	-----	-----00	Memory Address Register	
	-----	-----00	Locate anywhere in 32-bit space	
	-----	-----00	Memory Not Prefetchable	
	-----	-----00	Decoder for 16 bytes Memory Space	
444	-----	04000008	CONFIG READ ADDRESS	6.941,296,500 ms
	-----	04000008	Type 0 Register 2 Function 0	
445	-----	03000002	CONFIG READ DATA	6.941,341,500 ms

Figure 2- PMC64 Disassembly

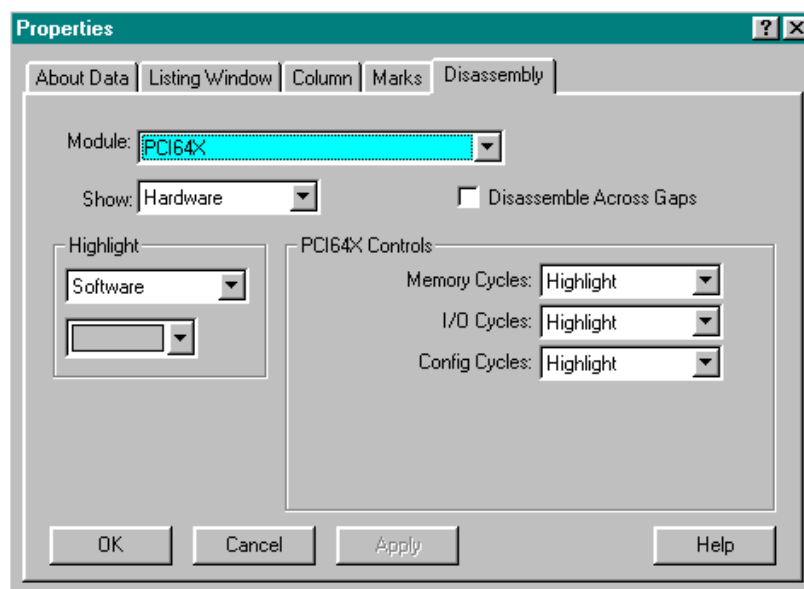


Figure 3- PMC64 Cycle Filter Window

contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark (disabled in PMC64)

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

The other column of interest is the Mnemonics column, where the PMC64 / PMC32 disassembly information is displayed. As mentioned previously, it is possible to choose which PCI cycles are displayed. This is done via selections made in the Disassembly tab of the Properties window. By default the display is in Hardware mode, and Memory, I/O, and Config cycles are set to Highlight. By choosing something other than Hardware in the Show select field, any cycle type set to Normal (instead of Highlight) will not be displayed. It is possible, for instance, to display only Config Cycles by setting Memory and I/O Cycles to Normal, leaving Config Cycles set to Highlight, and setting the Show select field to Software. All of the data still exists, some has just been suppressed from view. To return all of the data to visibility, set all Cycle selections to Highlight.

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

APPENDIX A - Necessary Signals for Clocking

To properly acquire PCI bus activity, the following signals must be provided: CLK, DEVSEL#, FRAME#, IRDY#, and TRDY#. The rising edge of CLK is used as the only active clocking edge; all other signals are used to properly qualify the acquisition of data.

APPENDIX B - Considerations

The NEX-PMC64 is an extender card that is also designed to permit monitoring the PMC/PCI bus signals. This permits the user to see exactly what is happening at the target. It is important to note that using the card as an extender will increase the stub length. Every effort has been taken to keep trace length as short as possible. To enhance signal integrity, stub resistors have been added to every trace routed to mictor connector pins to minimize the effect of the stub. It is entirely possible, however, that placing a target card onto the NEX-PMC64 extender will result in improper operation of the target card.

APPENDIX C - PMC Bus Pinout

Pin #	Pn1/Jn1	Pin#	Pn1/Jn1	Pin#	Pn2/Jn2	Pin#	Pn2/Jn2
1	TCK	33	FRAME#	1	+12V	33	GND
2	-12V	34	GND	2	TRST#	34	PMC-RSVD
3	GND	35	GND	3	TMS	35	TRDY#
4	INTA#	36	IRDY#	4	TDO	36	+3.3V
5	INTB#	37	DEVSEL#	5	TDI	37	GND
6	INTC#	38	+5V	6	GND	38	STOP#
7	BUSMODE1#	39	GND	7	GND	39	PERR#
8	+5V	40	LOCK#	8	PCI-RSVD	40	GND
9	INTD#	41	SDONE#	9	PCI-RSVD	41	+3.3V
10	PCI-RSVD	42	SBO#	10	PCI-RSVD	42	SERR#
11	GND	43	PAR	11	BUSMODE2#	43	C/BE[1]#
12	PCI-RSVD	44	GND	12	+3.3V	44	GND
13	CLK	45	V(I/O)	13	RST#	45	AD[14]
14	GND	46	AD[15]	14	BUSMODE3#	46	AD[13]
15	GND	47	AD[12]	15	3.3V	47	GND
16	GNT#	48	AD[11]	16	BUSMODE4#	48	AD[10]
17	REQ#	49	AD[09]	17	PCI-RSVD	49	AD[08]
18	+5V	50	+5V	18	GND	50	+3.3V
19	V(I/O)	51	GND	19	AD[30]	51	AD[07]
20	AD[31]	52	C/BE[0]#	20	AD[29]	52	PMC-RSVD
21	AD[28]	53	AD[06]	21	GND	53	+3.3V
22	AD[27]	54	AD[05]	22	AD[26]	54	PMC-RSVD
23	AD[25]	55	AD[04]	23	AD[24]	55	PMC-RSVD
24	GND	56	GND	24	+3.3V	56	GND
25	GND	57	V(I/O)	25	IDSEL	57	PMC-RSVD
26	C/BE[3]#	58	AD[03]	26	AD[23]	58	PMC-RSVD
27	AD[22]	59	AD[02]	27	+3.3V	59	GND
28	AD[21]	60	AD[01]	28	AD[20]	60	PMC-RSVD
29	AD[19]	61	AD[00]	29	AD[18]	61	ACK64#
30	+5V	62	+5V	30	GND	62	+3.3V
31	V(I/O)	63	GND	31	AD[16]	63	GND
32	AD[17]	64	REQ64#	32	C/BE[2]#	64	PMC-RSVD

Pin #	Pn3/Jn3	Pin#	Pn3/Jn3	Pin#	Pn4/Jn4	Pin#	Pn4/Jn4
1	PCI-RSVD	33	GND	1	I/O	33	I/O
2	GND	34	AD[48]	2	I/O	34	I/O
3	GND	35	AD[47]	3	I/O	35	I/O
4	C/BE[7]#	36	AD[46]	4	I/O	36	I/O
5	C/BE[6]#	37	AD[45]	5	I/O	37	I/O
6	C/BE[5]#	38	GND	6	I/O	38	I/O
7	C/BE[4]#	39	V(I/O)	7	I/O	39	I/O
8	GND	40	AD[44]	8	I/O	40	I/O
9	V(I/O)	41	AD[43]	9	I/O	41	I/O
10	PAR64	42	AD[42]	10	I/O	42	I/O
11	AD[63]	43	AD[41]	11	I/O	43	I/O
12	AD[62]	44	GND	12	I/O	44	I/O
13	AD[61]	45	GND	13	I/O	45	I/O
14	GND	46	AD[40]	14	I/O	46	I/O
15	GND	47	AD[39]	15	I/O	47	I/O
16	AD[60]	48	AD[38]	16	I/O	48	I/O
17	AD[59]	49	AD[37]	17	I/O	49	I/O
18	AD[58]	50	GND	18	I/O	50	I/O
19	AD[57]	51	GND	19	I/O	51	I/O
20	GND	52	AD[36]	20	I/O	52	I/O
21	V(I/O)	53	AD[35]	21	I/O	53	I/O
22	AD[56]	54	AD[34]	22	I/O	54	I/O
23	AD[55]	55	AD[33]	23	I/O	55	I/O
24	AD[54]	56	GND	24	I/O	56	I/O
25	AD[53]	57	V(I/O)	25	I/O	57	I/O
26	GND	58	AD[32]	26	I/O	58	I/O
27	GND	59	PCI-RSVD	27	I/O	59	I/O
28	AD[52]	60	PCI-RSVD	28	I/O	60	I/O
29	AD[51]	61	PCI-RSVD	29	I/O	61	I/O
30	AD[50]	62	GND	30	I/O	62	I/O
31	AD[49]	63	GND	31	I/O	63	I/O
32	GND	64	PCI-RSVD	32	I/O	64	I/O

APPENDIX E - NEX-PMC64 Mictor Pinout

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 / 92A96 Channel	PMC Signal Name	PMC Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 / 92A96 Channel	PMC Signal Name	PMC Pin #
3	5	CLK:0	BUSMODE1#	Jn1-7	36	6	CLK:1 ¹	DEVSEL#	Jn1-37
4	7	A3:7	AD[31]	Jn1-20	35	8	A1:7	AD[15]	Jn1-46
5	9	A3:6	AD[30]	Jn2-19	34	10	A1:6	AD[14]	Jn2-45
6	11	A3:5	AD[29]	Jn2-20	33	12	A1:5	AD[13]	Jn2-46
7	13	A3:4	AD[28]	Jn1-21	32	14	A1:4	AD[12]	Jn1-47
8	15	A3:3	AD[27]	Jn1-22	31	16	A1:3	AD[11]	Jn1-48
9	17	A3:2	AD[26]	Jn2-22	30	18	A1:2	AD[10]	Jn2-48
10	19	A3:1	AD[25]	Jn1-23	29	20	A1:1	AD[9]	Jn1-49
11	21	A3:0	AD[24]	Jn2-23	28	22	A1:0	AD[8]	Jn2-49
12	23	A2:7	AD[23]	Jn2-26	27	24	A0:7	AD[7]	Jn2-51
13	25	A2:6	AD[22]	Jn1-27	26	26	A0:6	AD[6]	Jn1-53
14	27	A2:5	AD[21]	Jn1-28	25	28	A0:5	AD[5]	Jn1-54
15	29	A2:4	AD[20]	Jn2-28	24	30	A0:4	AD[4]	Jn1-55
16	31	A2:3	AD[19]	Jn1-29	23	32	A0:3	AD[3]	Jn1-58
17	33	A2:2	AD[18]	Jn2-29	22	34	A0:2	AD[2]	Jn1-59
18	35	A2:1	AD[17]	Jn1-32	21	36	A0:1	AD[1]	Jn1-60
19	37	A2:0	AD[16]	Jn2-31	20	38	A0:0	AD[0]	Jn1-61

Group A Mictor

Notes:

1. DEVSEL# is also connected to C3:0

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 / 92A96 Channel	PMC Signal Name	PMC Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 / 92A96 Channel	PMC Signal Name	PMC Pin #
3	5	CLK:3 ¹	CLK	Jn1-13	36	6	QUAL:1	BUSMODE2#	Jn2-11
4	7	C3:7	CLK	Jn1-13	35	8	C1:7 ³	C/BE[7]#	Jn3-4
5	9	C3:6	SDONE	Jn1-41	34	10	C1:6 ³	C/BE[6]#	Jn3-5
6	11	C3:5 ²	RST#	Jn2-13	33	12	C1:5 ³	C/BE[5]#	Jn3-6
7	13	C3:4	LOCK#	Jn1-40	32	14	C1:4 ³	C/BE[4]#	Jn3-7
8	15	C3:3	PERR#	Jn2-39	31	16	C1:3	SBO#	Jn1-42
9	17	C3:2	PAR	Jn1-43	30	18	C1:2	PAR64	Jn3-10
10	19	C3:1	SERR#	Jn2-42	29	20	C1:1 ³	ACQ64#	Jn2-61
11	21	C3:0 ²	DEVSEL#	Jn1-37	28	22	C1:0 ³	REQ64#	Jn1-64
12	23	C2:7 ²	C/BE[3]#	Jn1-26	27	24	C0:7	M66EN	
13	25	C2:6 ²	C/BE[2]#	Jn2-32	26	26	C0:6	GNT#	Jn1-16
14	27	C2:5 ²	C/BE[1]#	Jn2-43	25	28	C0:5	REQ#	Jn1-17
15	29	C2:4 ²	C/BE[0]#	Jn1-52	24	30	C0:4	IDSEL	Jn2-25
16	31	C2:3 ²	STOP#	Jn2-38	23	32	C0:3	INTD#	Jn1-9
17	33	C2:2 ²	TRDY#	Jn2-35	22	34	C0:2	INTC#	Jn1-6
18	35	C2:1 ²	IRDY#	Jn1-36	21	36	C0:1	INTB#	Jn1-5
19	37	C2:0 ²	FRAME#	Jn1-33	20	38	C0:0	INTA#	Jn1-4

Group C Mictor

Notes:

1. CLK is also connected to C3:7
2. These signals are required for proper 32- or 64-bit disassembly
3. These signals are required for proper 64-bit disassembly

Tek Mictor Pin #	AMP Mictor Pin #	TLA700 / 92A96 Channel	PMC Signal Name	PMC Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA700 / 92A96 Channel	PMC Signal Name	PMC Pin #
3	5	QUAL:0	BUSMODE3#	Jn2-14	36	6	CLK:2	BUSMODE4#	Jn2-16
4	7	D3:7	AD[63]	Jn3-11	35	8	D1:7	AD[47]	Jn3-35
5	9	D3:6	AD[62]	Jn3-12	34	10	D1:6	AD[46]	Jn3-36
6	11	D3:5	AD[61]	Jn3-13	33	12	D1:5	AD[45]	Jn3-37
7	13	D3:4	AD[60]	Jn3-16	32	14	D1:4	AD[44]	Jn3-40
8	15	D3:3	AD[59]	Jn3-17	31	16	D1:3	AD[43]	Jn3-41
9	17	D3:2	AD[58]	Jn3-18	30	18	D1:2	AD[42]	Jn3-42
10	19	D3:1	AD[57]	Jn3-19	29	20	D1:1	AD[41]	Jn3-43
11	21	D3:0	AD[56]	Jn3-22	28	22	D1:0	AD[40]	Jn3-46
12	23	D2:7	AD[55]	Jn3-23	27	24	D0:7	AD[39]	Jn3-47
13	25	D2:6	AD[54]	Jn3-24	26	26	D0:6	AD[38]	Jn3-48
14	27	D2:5	AD[53]	Jn3-25	25	28	D0:5	AD[37]	Jn3-49
15	29	D2:4	AD[52]	Jn3-28	24	30	D0:4	AD[36]	Jn3-52
16	31	D2:3	AD[51]	Jn3-29	23	32	D0:3	AD[35]	Jn3-53
17	33	D2:2	AD[50]	Jn3-30	22	34	D0:2	AD[34]	Jn3-54
18	35	D2:1	AD[49]	Jn3-31	21	36	D0:1	AD[33]	Jn3-55
19	37	D2:0	AD[48]	Jn3-34	20	38	D0:0	AD[32]	Jn3-58

Group D Mictor

APPENDIX F - NEX-PMC64 P6960 D-Max Pinout

For further information on the P6960 probes please refer to the “P69xx Series High-Density Logic Analyzer Probes with D-Max Probing Technology Instruction Manual”, Tektronix part number 071-1528-02.

Connect NEX-M2P69X adapter to NEX-PMC64 Mictor connection “GROUP A”							
Pad	TLA Channel	PMC Signal Name	PMC Pin #	Pad	TLA Channel	PMC Signal Name	PMC Pin #
B20	Q0-	GND	-----	A8	CK0-	GND	-----
B21	Q0+	DEVSEL#	Jn1-37	A7	CK0+	BUSMODE1#	Jn1-7
B14	D3:7	AD[15]	Jn1-46	A14	A3:7	AD[31]	Jn1-20
B15	D3:6	AD[14]	Jn2-45	A13	A3:6	AD[30]	Jn2-19
A16	D3:5	AD[13]	Jn2-46	B12	A3:5	AD[29]	Jn2-20
A17	D3:4	AD[12]	Jn1-47	B11	A3:4	AD[28]	Jn1-21
B17	D3:3	AD[11]	Jn1-48	A11	A3:3	AD[27]	Jn1-22
B18	D3:2	AD[10]	Jn2-48	A10	A3:2	AD[26]	Jn2-22
A19	D3:1	AD[09]	Jn1-49	B9	A3:1	AD[25]	Jn1-23
A20	D3:0	AD[08]	Jn2-49	B8	A3:0	AD[24]	Jn2-23
A22	D2:7	AD[07]	Jn2-51	B6	A2:7	AD[23]	Jn2-26
A23	D2:6	AD[06]	Jn1-53	B5	A2:6	AD[22]	Jn1-27
B23	D2:5	AD[05]	Jn1-54	A5	A2:5	AD[21]	Jn1-28
B24	D2:4	AD[04]	Jn1-55	A4	A2:4	AD[20]	Jn2-28
A25	D2:3	AD[03]	Jn1-58	B3	A2:3	AD[19]	Jn1-29
A26	D2:2	AD[02]	Jn1-59	B2	A2:2	AD[18]	Jn2-29
B26	D2:1	AD[01]	Jn1-60	A2	A2:1	AD[17]	Jn1-32
B27	D2:0	AD[00]	Jn1-61	A1	A2:0	AD[16]	Jn2-31

Probe Connection D2/D3

Probe Connection A2/A3

Connect NEX-M2P69X adapter to NEX-PMC64 Mictor connection "GROUP C"							
Pad	TLA Channel	PMC Signal Name	PMC Pin #	Pad	TLA Channel	PMC Signal Name	PMC Pin #
B20	Q1-	GND	-----	A1	CK3-	GND	-----
B21	Q1+	BUSMODE2#	Jn2-11	A7	CK3+	CLK	Jn1-13
B14	C1:7	C/BE[7]#	Jn3-4	A14	C3:7	CLK	Jn1-13
B15	C1:6	C/BE[6]#	Jn3-5	A13	C3:6	SDONE	Jn1-41
A16	C1:5	C/BE[5]#	Jn3-6	B12	C3:5	RST#	Jn2-13
A17	C1:4	C/BE[4]#	Jn3-7	B11	C3:4	LOCK#	Jn1-40
B17	C1:3	SBO#	Jn1-42	A11	C3:3	PERR#	Jn2-39
B18	C1:2	PAR64	Jn3-10	A10	C3:2	PAR	Jn1-43
A19	C1:1	ACQ64#	Jn2-61	B9	C3:1	SERR#	Jn2-42
A20	C1:0	REQ64#	Jn1-64	B8	C3:0	DEVSEL#	Jn1-37
A22	C0:7	M66EN		B6	C2:7	C/BE[3]#	Jn1-26
A23	C0:6	GNT#	Jn1-16	B5	C2:6	C/BE[2]#	Jn2-32
B23	C0:5	REQ#	Jn1-17	A5	C2:5	C/BE[1]#	Jn2-43
B24	C0:4	IDSEL	Jn2-25	A4	C2:4	C/BE[0]#	Jn1-52
A25	C0:3	INTD#	Jn1-9	B3	C2:3	STOP#	Jn2-38
A26	C0:2	INTC#	Jn1-6	A1	C2:2	TRDY#	Jn2-35
B26	C0:1	INTB#	Jn1-5	A7	C2:1	IRDY#	Jn1-36
B27	C0:0	INTA#	Jn1-4	A14	C2:0	FRAME#	Jn1-33

Probe Connection C0/C1

Probe Connection C2/C3

Connect NEX-M2P69X adapter to NEX-PMC64 Mictor connection "GROUP D"							
Pad	TLA Channel	PMC Signal Name	PMC Pin #	Pad	TLA Channel	PMC Signal Name	PMC Pin #
B20	CK2-	GND	-----	A8	CK1-	GND	-----
B21	CK2+	BUSMODE4#	Jn2-16	A7	CK1+	BUSMODE3#	Jn2-14
B14	D1:7	AD[47]	Jn3-35	A14	A1:7	AD[63]	Jn3-11
B15	D1:6	AD[46]	Jn3-36	A13	A1:6	AD[62]	Jn3-12
A16	D1:5	AD[45]	Jn3-37	B12	A1:5	AD[61]	Jn3-13
A17	D1:4	AD[44]	Jn3-40	B11	A1:4	AD[60]	Jn3-16
B17	D1:3	AD[43]	Jn3-41	A11	A1:3	AD[59]	Jn3-17
B18	D1:2	AD[42]	Jn3-42	A10	A1:2	AD[58]	Jn3-18
A19	D1:1	AD[41]	Jn3-43	B9	A1:1	AD[57]	Jn3-19
A20	D1:0	AD[40]	Jn3-46	B8	A1:0	AD[56]	Jn3-22
A22	D0:7	AD[39]	Jn3-47	B6	A0:7	AD[55]	Jn3-23
A23	D0:6	AD[38]	Jn3-48	B5	A0:6	AD[54]	Jn3-24
B23	D0:5	AD[37]	Jn3-49	A5	A0:5	AD[53]	Jn3-25
B24	D0:4	AD[36]	Jn3-52	A4	A0:4	AD[52]	Jn3-28
A25	D0:3	AD[35]	Jn3-53	B3	A0:3	AD[51]	Jn3-29
A26	D0:2	AD[34]	Jn3-54	B2	A0:2	AD[50]	Jn3-30
B26	D0:1	AD[33]	Jn3-55	A2	A0:1	AD[49]	Jn3-31
B27	D0:0	AD[32]	Jn3-58	A1	A0:0	AD[48]	Jn3-34

Probe Connection D0/D1

Probe Connection A0/A1

APPENDIX G - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

Tektronix P6860 Compression Probe Manual

IEEE P1386.1/Draft2.0 PCI Mezzanine Card

PCI Local Bus Specification

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PO Box 14070

Portland OR 97214

800-433-5177 (U.S.)

503-797-4207 (International)

503-234-6762 (FAX)

PCI System Architecture

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Mindshare, Inc. (Tom Shanley / Don Anderson)

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APPENDIX H - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.