



NEX-SA110
StrongARM Disassembly Software Users Manual
Including these Software Support packages:
SA110

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1.0 OVERVIEW

1.1 General Information

The NEX-SA110 disassembly software provides disassembly of acquired StrongARM SA-110 bus cycles using a TLA600/700 102-channel or 136-channel acquisition module. The NEX-SA110 support is software only. Please see Section 3.0 “Connecting to a SA-110 Target” for information on probing.

The NEX-SA110 provides full instruction decoding of ARM, through Architecture v4. Thumb instructions are not supported at this time.

This manual assumes that the user is familiar with the SA-110 processor specification and the Tektronix TLA600/700 Logic Analyzer. It is also expected that the user is familiar with Windows 95. The TLA600/700 Application must also be at V1.1 or later for the NEX-SA110 support to work properly.

2.0 SOFTWARE INSTALLATION

One 3½” diskette has been included with the NEX-SA110 disassembly product, and it contains the software support for the Logic Analyzer. The NEX-SA110 software is loaded in the same method as other Win95 programs. Place the NEX-SA110 Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the SA110 support in its proper place on the hard disk.

To load SA110 support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose SA110 and click on **Okay**.

3.0 CONNECTING TO AN SA-110 TARGET

3.1 General

When possible it is recommended that the user add Mictor connectors to their target for the interface to the TLA600/700 using Tektronix P6434 high-density probes. Table 1 shows the wiring and Channel Grouping required for NEX-SA110 support.

IMPORTANT: Specific wiring must be followed when routing the SA110 signals to Mictor connectors if the NEX-SA110 support is going to be used. Appendix A “NEX-SA110 Mictor Pinout” and Appendix B “NEX-SA110 P6860 Compression Pinouts” provides this information.

Group Name	Signal Name	SA-110 Pin #	TLA700 input	Group Name	Signal Name	SA- Pin #	TLA700 input
Address (Hex)	A[31]	120	A3:7	Data (Hex)	D[31]	47	D3:7
	A[30]	119	A3:6		D[30]	46	D3:6
	A[29]	118	A3:5		D[29]	45	D3:5
	A[28]	117	A3:4		D[28]	44	D3:4
	A[27]	116	A3:3		D[27]	41	D3:3
	A[26]	115	A3:2		D[26]	40	D3:2
	A[25]	112	A3:1		D[25]	39	D3:1
	A[24]	111	A3:0		D[24]	38	D3:0
	A[23]	110	A2:7		D[23]	37	D2:7
	A[22]	109	A2:6		D[22]	35	D2:6
	A[21]	108	A2:5		D[21]	34	D2:5
	A[20]	107	A2:4		D[20]	33	D2:4
	A[19]	106	A2:3		D[19]	28	D2:3
	A[18]	101	A2:2		D[18]	27	D2:2
	A[17]	100	A2:1		D[17]	26	D2:1
	A[16]	99	A2:0		D[16]	25	D2:0
	A[15]	98	A1:7		D[15]	24	D1:7
	A[14]	97	A1:6		D[14]	23	D1:6
	A[13]	96	A1:5		D[13]	22	D1:5
	A[12]	95	A1:4		D[12]	21	D1:4
	A[11]	94	A1:3		D[11]	16	D1:3
	A[10]	89	A1:2		D[10]	15	D1:2
	A[9]	88	A1:1		D[9]	14	D1:1
	A[8]	87	A1:0		D[8]	13	D1:0
	A[7]	86	A0:7		D[7]	12	D0:7
	A[6]	85	A0:6		D[6]	11	D0:6
	A[5]	84	A0:5		D[5]	10	D0:5
	A[4]	83	A0:4		D[4]	9	D0:4
	A[3]	82	A0:3		D[3]	4	D0:3
	A[2]	77	A0:2		D[2]	3	D0:2
	A[1]	76	A0:1		D[1]	2	D0:1
	A[0]	75	A0:0		D[0]	1	D0:0
Control (Sym)	MAS1	74	C2:7	Misc.	MCLK	123	Clock0
	MAS0	73	C2:6		APE	121	Clock1
	ABORT	122	C2:3		DBE	36	C3:2
	nRW	62	C2:4		ABE	72	C3:1
	CLF	60	C2:1		CONFIG	57	C2:5
	nMREQ	58	C2:2		nPWRS�	140	C3:6
Intrpts	nFIQ	143	C3:4	LOCK	61	C3:3	
	nIRQ	144	C3:5	nWAIT	127	C2:0	
				Ungrouped	nRESET	141	Clock3

Table 1- SA-110 TLA600/700 Wiring

3.2 Clips for connecting to the SA-110

If a clip is needed to connect the TLA logic analyzer to the SA-110 pins please contact Nexus Technology for a list of recommended adapter vendors. You can also get a list of recommended vendors from our web site <http://www.busboards.com>.

4.0 CLOCK SELECTION

4.1 General Information

There are two clocking options available when using the NEX-SA110 support package. Each is explained in detail below.

The clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

NOTE: Depending upon the speed of the SA-110 micro and the design of the target it may be necessary to adjust the Setup & Hold times for some of the NEX-SA110 data groups to ensure proper data acquisition. Please refer to Appendix C - Clocking Considerations for further details.

4.2 Clocking Options - Explanation

Bus Cycle Clocking - This is the default clocking selection. In this mode the software monitors MCLK, nWAIT, and nMREQ to permit the acquisition of StrongARM bus cycles only. All Wait and idle states will be ignored, offering the best use of your acquisition memory. Refer to Appendix B for more information on how bus cycle data is acquired.

Every Edge of MCLK - In this mode, data will be acquired on every edge of the MCLK signal. The disassembly software will try to filter and display these cycles accordingly, but incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows all bus cycles, including any Wait or idle states. Since no clocking qualification is done only the MCLK signal is needed.

5.0 VIEWING DATA

5.1 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: SA110 and SA110-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except

in Timing format. The second selection, SA110-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

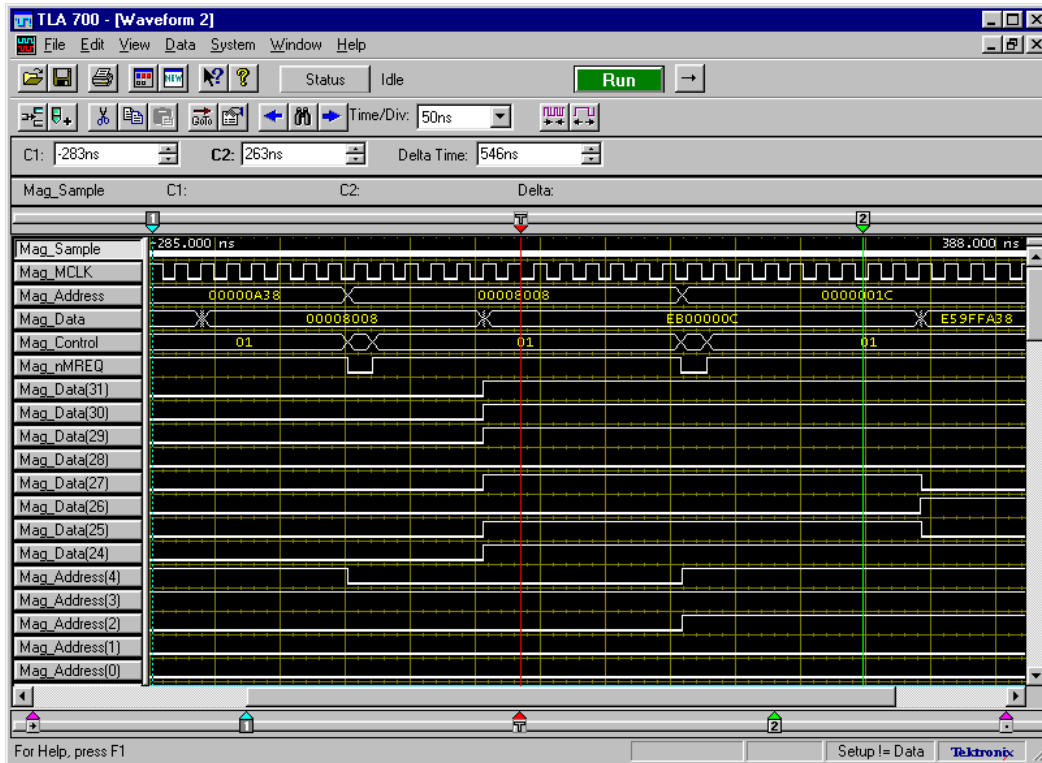


Figure 1- SA110 MagniVu Display on TLA600/700

6.0 USING THE DISASSEMBLY SOFTWARE

6.1 General

The NEX-SA110 support software acquires and decodes StrongARM SA-110 bus activity and displays the information as assembly language mnemonics (machine code) - see Figure 2. This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types of interest to the software engineer (Figure 3). The user can choose to display the acquired data in Hardware, Software, Control Flow, or Subroutine modes.

A major feature of the NEX-SA110 software is its ability to intelligently acquire bus cycle information. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the SA110 software is able to acquire only the valid SA-110 bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more microprocessor bus cycles. For debug purposes, the user also has the ability to override this

function and acquire data on every MCLK edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps in the TLA600/700 series, permits precise measurements of microprocessor bus activity. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

6.2 Disassembly Using the TLA600/700

The TLA600/700, since it is a Win95 program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

Sample	SA1X0 Address	SA1X0 Data	SA1X0 Mnemonics	Intrpts	Timestamp
3989	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-76.235,000 us
3990	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-75.268,500 us
3992	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-73.848,000 us
3994	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-71.914,000 us
3995	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-70.947,500 us
3997	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-69.527,500 us
3999	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-67.593,500 us
4000	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-66.626,500 us
4002	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-65.206,500 us
4004	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-63.272,500 us
4005	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-62.306,000 us
4007	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-60.885,500 us
4009	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-58.952,000 us
4010	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-57.985,000 us
4012	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-56.565,000 us
4014	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-54.631,000 us
4015	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-53.664,000 us
4017	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-52.244,000 us
4019	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-50.310,000 us
4020	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-49.343,500 us
4022	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-47.923,000 us
4024	80000CCC	E5D01000	LDRB R1, [R0], #+000(0xF000FF7)	01	-45.989,500 us
4025	80000CD0	E3110001	TSTS R0, R1, #01 >> 0	01	-45.022,500 us
4027	80000CD4	0AFFFFF0	BEQ 0x80000CCC	01	-43.602,500 us
4028	80000CD8	E9F01E0	LDR R0, [R15], #+1E0(0x80000EC0)	01	-42.635,500 us
4029	80000CDC	E5D00000	LDRB R0, [R0], #+000(0xF000FE3)	01	-41.668,500 us
4031	80000CE0	E1A0100E	MOV R1, R0, R14	01	-39.774,500 us
4033	80000CE4	E1A0F001	MOV R15, R0, R1	01	-38.354,000 us
4035	800083A0	E1A04000	MOV R4, R0, R0	01	-36.420,500 us
4036	800083A4	E3A06C0A	MOV R6, R0, #0A >> 24	01	-35.453,500 us
4037	800083A8	E59600DC	LDR R0, [R6], #+0DC(0x0000ADC)	01	-34.487,500 us
4038	800083AC	E3300000	TEQS R0, R0, #00 >> 0	01	-33.520,500 us
4040	800083B0	1A000009	BNE 0x800083DC	01	-32.395,500 us
4041	800083B4	E5D610D9	LDRB R1, [R6], #+0D9(0x0000ADB)	01	-31.428,500 us
4042	800083B8	E3110002	TSTS R0, R1, #02 >> 0	01	-30.462,500 us
4044	800083BC	E5C600D9	STRB R0, [R6], #+0D9	01	-29.338,000 us
4045	800083C0	18BD8000	LDMNEIA R13!, R15(0x0000AEO)+	01	-28.370,500 us

Figure 2- SA110 Disassembly

The other column of interest is the Mnemonics column, where the SA-110 disassembly information is displayed. As mentioned previously, it is possible to filter the SA-110 instructions that are displayed. This is done via selections made in the Disassembly tab of the Properties window (see Figure 3). By default the display is in Hardware mode, where all bus cycles are displayed (Memory Reads, Memory Writes, Instructions, etc.). Other choices are: Software (only executed instructions are displayed), Control Flow (display of instructions affecting code flow such as Jumps, Branches, etc.), and Subroutine (only instructions such as Calls, Returns, etc. are displayed).

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

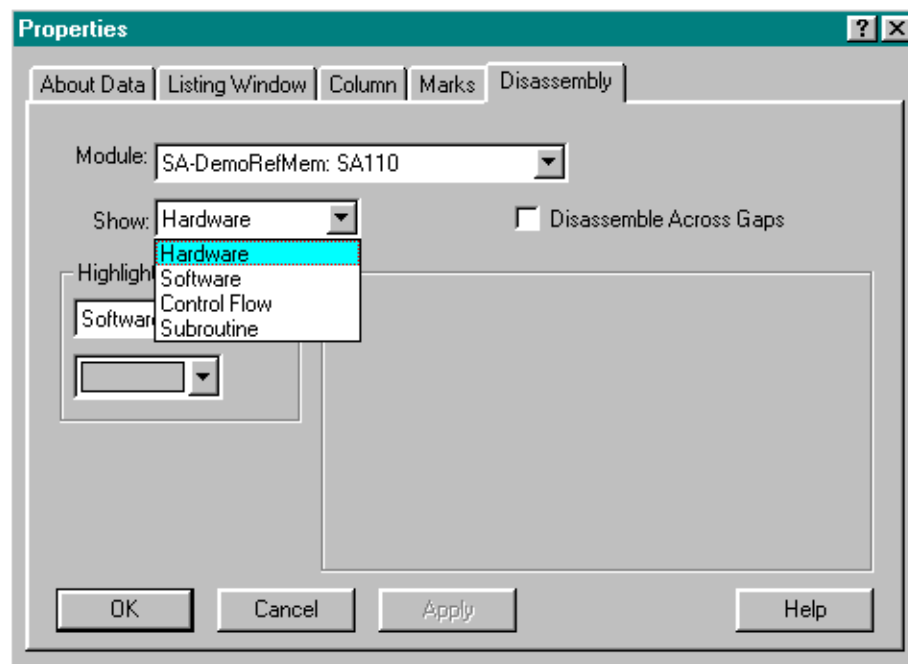


Figure 3- Disassembly Display Filter Window

6.3 Instruction Decoding/Addressing Modes Supported

The following lists the particular StrongARM feature sets that the NEX-SA110 disassembler packages supports.

IMPORTANT: The Thumb instruction set is not supported at this time.

- Architecture v4 Level Instructions and Addressing modes
- Load data read cycle detection
 - LDM and LDC multiple load read cycle detection
 - Branch Prefetch Instruction flush detection
 - Mark-Opcode support

All five addressing modes:

Addressing Mode 1

- Shifter operands
- Immediate
- Register
- Logical shift left by immediate
- Logical shift left by register
- Logical shift right by immediate
- Logical shift right by register
- Arithmetic shift right by immediate
- Arithmetic shift right by register

- Rotate right by immediate
- Rotate right by register
- Rotate right with extend

Addressing Mode 2

- Immediate offset
- Register offset
- Scaled register offset
- Immediate pre-indexed
- Register pre-indexed
- Scaled register pre-indexed
- Immediate post-indexed
- Register post-indexed
- Scaled register post-indexed

Addressing Mode 3

- Immediate offset
- Register offset
- Immediate pre-indexed
- Register pre-indexed
- Immediate post-indexed
- Register post-indexed

Addressing Mode 4

- Increment after
- Increment before
- Decrement after
- Decrement before

Addressing Mode 5

- Immediate offset
- Immediate pre-indexed
- Immediate post-indexed

6.4 SA-110 Instructions Supported

ADC	{<cond>}{S} Rd, Rn, <shifter_operand>	
ADD	{<cond>}{S} Rd, Rn, <shifter_operand>	
AND	{<cond>}{S} Rd, Rn, <shifter_operand>	
B{L}	{<cond>} <target address>	
BIC	{<cond>}{S} Rd, Rn, <shifter_operand>	
BX	{<cond>} Rm	
CDP	{<cond>} p<cp#>, <opcode_1>, CRd, CRn, CRm, <opcode_2>	
CMN	{<cond>} Rn, <shifter_operand>	
CMP	{<cond>} Rn, <shifter_operand>	
EOR	{<cond>}{S} Rd, Rn, <shifter_operand>	
LDC	{<cond>} p<cp_num>, CRd, <addressing_mode>	
LDM	{<cond>} <addressing_mode> Rn{!}, <registers>	LDM(1)
LDM	{<cond>} <addressing_mode> Rn, <registers>^	LDM(2)

LDM	{<cond>} <addressing_mode> Rn{!}, <registers_and_pc>^	
LDM(3)		
LDR	{<cond>} Rd, <addressing_mode>	
LDR	{<cond>}B Rd, <addressing_mode>	
LDR	{<cond>}BT Rd, <post_indexed_addressing_mode>	
LDR	{<cond>}H Rd, <addressing_mode>	
LDR	{<cond>}SB Rd, <addressing_mode>	
LDR	{<cond>}SH Rd, <addressing_mode>	
LDR	{<cond>}T Rd, <post_indexed_addressing_mode>	
MCR	{<cond>} p<cp#>, <opcode_1>, Rd, CRn, CRm, <opcode_2>	
MLA	{<cond>}{<S>} Rd, Rm, Rs, Rn	
MOV	{<cond>}{S} Rd, <shifter_operand>	
MRC	{<cond>} p<cp#>, <opcode_1>, Rd, CRn, CRm, <opcode_2>	
MRS	{<cond>} Rd, CPSR	
MRS	{<cond>} Rd, SPSR	
MSR	{<cond>} Rd, CPSR_f, #32bit immediate	
MSR	{<cond>} Rd, CPSR_<fields>, Rm	
MSR	{<cond>} Rd, SPSR_f, #32bit immediate	
MSR	{<cond>} Rd, SPSR_<fields>, Rm	
MUL	{<cond>}{<S>}Rd, Rm, Rs	
MVN	{<cond>}{<S>} Rd, <shifter_operand>	
ORR	{<cond>}{S} Rd, Rn, <shifter_operand>	
RSB	{<cond>}{S} Rd, Rn, <shifter_operand>	
RSC	{<cond>}{S} Rd, Rn, <shifter_operand>	
SBC	{<cond>}{S} Rd, Rn, <shifter_operand>	
SMLAL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	
SMULL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	
STC	{<cond>} p<cp_num>, CRd, <addressing_mode>	
STM	{<cond>} <addressing_mode> Rn{!}, <registers>	STM(1)
STM	{<cond>} <addressing_mode> Rn{!}, <registers>^	STM(2)
STR	{<cond>} Rd, <addressing_mode>	
STR	{<cond>}B Rd, <addressing_mode>	
STR	{<cond>}BT Rd, <post_indexed_addressing_mode>	
STR	{<cond>}H Rd, <addressing_mode>	
STR	{<cond>}T Rd, <post_indexed_addressing_mode>	
SUB	{<cond>}{<S>} Rd, Rn, <shifter_operand>	
SWI	{<cond>} <24_bit_immediate>	
SWP	{<cond>} Rd, Rm, [Rn]	
SWP	{<cond>}B Rd, Rm, [Rn]	
TEQ	{<cond>} Rn, <shifter_operand>	
TST	{<cond>} Rn, <shifter_operand>	
UMLAL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	
UMULL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	

7.0 THE NEX-SA110 CONTROL GROUP SYMBOL TABLE

The use of Symbol Tables when displaying state data and defining a trigger enables the user to quickly determine the type of bus cycle that occurred or is desired. A symbol table for the Control group (SA110_Ctrl, Table 2) has been provided to quickly show the type of bus transaction acquired when viewing data in Listing display. This same symbol table can be used in the Trigger area of the TLA to easily define the sort of bus cycle that is to be triggered on.

Pattern	TLA600/700 Symbols	Meaning
xx1xxx	ABORT	CPU Abort Cycle
xx10x1	I/O READ	I/O Read Cycle
xx11x1	I/O WRITE	I/O Write Cycle
xx00x0	MEM READ/FETCH	Memory Read or Fetch Cycle
xx01x0	MEM WRITE	Memory Write Cycle

Table 2- NEX-SA110 Control Symbol Table

Signals, from left to right: MAS1, MAS0, ABORT, nRW, CLF, nMREQ

APPENDIX A - NEX-SA110 Mictor Pinout

The following Mictor wiring must be followed if the NEX-SA110 disassembly software is to be used. Please refer to the Tektronix P6434 Mass Termination Probe Instruction Manual for further information on designing the Mictor connectors into your target. TLA inputs that show dashes ('---') in the SA-110 Pin and Signal columns are unassigned, and may be connected to any target signal desired.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA-110 Pin #	SA-110 Signal	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA-110 Pin #	SA-110 Signal
3	5	CK0	123	MCLK	36	6	CK1	121	APE
4	7	A3:7	120	A31	35	8	A1:7	98	A15
5	9	A3:6	119	A30	34	10	A1:6	97	A14
6	11	A3:5	118	A29	33	12	A1:5	96	A13
7	13	A3:4	117	A28	32	14	A1:4	95	A12
8	15	A3:3	116	A27	31	16	A1:3	94	A11
9	17	A3:2	115	A26	30	18	A1:2	89	A10
10	19	A3:1	112	A25	29	20	A1:1	88	A9
11	21	A3:0	111	A24	28	22	A1:0	87	A8
12	23	A2:7	110	A23	27	24	A0:7	86	A7
13	25	A2:6	109	A22	26	26	A0:6	85	A6
14	27	A2:5	108	A21	25	28	A0:5	84	A5
15	29	A2:4	107	A20	24	30	A0:4	83	A4
16	31	A2:3	106	A19	23	32	A0:3	82	A3
17	33	A2:2	101	A18	22	34	A0:2	77	A2
18	35	A2:1	100	A17	21	36	A0:1	76	A1
19	37	A2:0	99	A16	20	38	A0:0	75	A0

Mictor Group A

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA-110 Pin #	SA-110 Signal	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA-110 Pin #	SA-110 Signal
3	5	CK3	141	nRESET	36	6	Q1	---	---
4	7	C3:7	---	---	35	8	C1:7	---	---
5	9	C3:6	140	nPWRSLP	34	10	C1:6	---	---
6	11	C3:5	144	nIRQ	33	12	C1:5	---	---
7	13	C3:4	143	nFIQ	32	14	C1:4	---	---
8	15	C3:3	61	LOCK	31	16	C1:3	---	---
9	17	C3:2	36	DBE	30	18	C1:2	---	---
10	19	C3:1	72	ABE	29	20	C1:1	---	---
11	21	C3:0	---	---	28	22	C1:0	---	---
12	23	C2:7	74	MAS1	27	24	C0:7	---	---
13	25	C2:6	73	MAS0	26	26	C0:6	---	---
14	27	C2:5	57	CONFIG	25	28	C0:5	---	---
15	29	C2:4	62	nRW	24	30	C0:4	---	---
16	31	C2:3	122	ABORT	23	32	C0:3	---	---
17	33	C2:2	58	nMREQ	22	34	C0:2	---	---
18	35	C2:1	60	CLF	21	36	C0:1	---	---
19	37	C2:0	127	nWAIT	20	38	C0:0	---	---

Mictor Group C

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA-110 Pin #	SA-110 Signal	Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA-110 Pin #	SA-110 Signal
3	5	Q0	---	---	36	6	CK2	---	---
4	7	D3:7	47	D31	35	8	D1:7	24	D15
5	9	D3:6	46	D30	34	10	D1:6	23	D14
6	11	D3:5	45	D29	33	12	D1:5	22	D13
7	13	D3:4	44	D28	32	14	D1:4	21	D12
8	15	D3:3	41	D27	31	16	D1:3	16	D11
9	17	D3:2	40	D26	30	18	D1:2	15	D10
10	19	D3:1	39	D25	29	20	D1:1	14	D9
11	21	D3:0	38	D24	28	22	D1:0	13	D8
12	23	D2:7	37	D23	27	24	D0:7	12	D7
13	25	D2:6	35	D22	26	26	D0:6	11	D6
14	27	D2:5	34	D21	25	28	D0:5	10	D5
15	29	D2:4	33	D20	24	30	D0:4	9	D4
16	31	D2:3	28	D19	23	32	D0:3	4	D3
17	33	D2:2	27	D18	22	34	D0:2	3	D2
18	35	D2:1	26	D17	21	36	D0:1	2	D1
19	37	D2:0	25	D16	20	38	D0:0	1	D0

Mictor Group D

APPENDIX B - NEX-SA110 P6860 Compression Pinouts

For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

Pad #	TLA Channel	SA-110 Pin #	SA-110 Signal Name
A15	CK1-	Gnd	Gnd
A13	CK1+	121	APE
B12	A1:7	98	A15
B10	A1:6	97	A14
A12	A1:5	96	A13
A10	A1:4	95	A12
B9	A1:3	94	A11
B7	A1:2	89	A10
A9	A1:1	88	A9
A7	A1:0	87	A8
B6	A0:7	86	A7
B4	A0:6	85	A6
A6	A0:5	84	A5
A4	A0:4	83	A4
B3	A0:3	82	A3
B1	A0:2	77	A2
A3	A0:1	76	A1
A1	A0:0	75	A0

Probe Connection A0/A1

Pad #	TLA Channel	SA-110 Pin #	SA-110 Signal Name
A15	CK0-	Gnd	Gnd
A13	CK0+	123	MCLK
B12	A3:7	120	A31
B10	A3:6	119	A30
A12	A3:5	118	A29
A10	A3:4	117	A28
B9	A3:3	116	A27
B7	A3:2	115	A26
A9	A3:1	112	A25
A7	A3:0	111	A24
B6	A2:7	110	A23
B4	A2:6	109	A22
A6	A2:5	108	A21
A4	A2:4	107	A20
B3	A2:3	106	A19
B1	A2:2	101	A18
A3	A2:1	100	A17
A1	A2:0	99	A16

Probe Connection A2/A3

Pad #	TLA Channel	SA110 Pin #	SA110 Signal Name
A15	Q1-	Gnd	Gnd
A13	Q1+	---	---
B12	C1:7	---	---
B10	C1:6	---	---
A12	C1:5	---	---
A10	C1:4	---	---
B9	C1:3	---	---
B7	C1:2	---	---
A9	C1:1	---	---
A7	C1:0	---	---
B6	C0:7	---	---
B4	C0:6	---	---
A6	C0:5	---	---
A4	C0:4	---	---
B3	C0:3	---	---
B1	C0:2	---	---
A3	C0:1	---	---
A1	C0:0	---	---

Probe Connection C0/C1

Pad #	TLA Channel	SA110 Pin #	SA110 Signal Name
A15	CK3-	Gnd	Gnd
A13	CK3+	141	nRESET
B12	C3:7	---	---
B10	C3:6	140	nPWRSLP
A12	C3:5	144	nIRQ
A10	C3:4	143	nFIQ
B9	C3:3	61	LOCK
B7	C3:2	36	DBE
A9	C3:1	72	ABE
A7	C3:0	---	---
B6	C2:7	74	MAS1
B4	C2:6	73	MAS0
A6	C2:5	57	CONFIG
A4	C2:4	62	nRW
B3	C2:3	122	ABORT
B1	C2:2	58	nMREQ
A3	C2:1	60	CLF
A1	C2:0	127	nWAIT

Probe Connection C2/C3

Pad #	TLA Channel	SA110 Pin #	SA110 Signal Name
A15	CK2-		
A13	CK2+	---	---
B12	D1:7	24	D15
B10	D1:6	23	D14
A12	D1:5	22	D13
A10	D1:4	21	D12
B9	D1:3	16	D11
B7	D1:2	15	D10
A9	D1:1	14	D9
A7	D1:0	13	D8
B6	D0:7	12	D7
B4	D0:6	11	D6
A6	D0:5	10	D5
A4	D0:4	9	D4
B3	D0:3	4	D3
B1	D0:2	3	D2
A3	D0:1	2	D1
A1	D0:0	1	D0

Probe Connection D0/D1

Pad #	TLA Channel	SA110 Pin #	SA110 Signal Name
A15	Q0-		
A13	Q0+	---	---
B12	D3:7	47	D31
B10	D3:6	46	D30
A12	D3:5	45	D29
A10	D3:4	44	D28
B9	D3:3	41	D27
B7	D3:2	40	D26
A9	D3:1	39	D25
A7	D3:0	38	D24
B6	D2:7	37	D23
B4	D2:6	35	D22
A6	D2:5	34	D21
A4	D2:4	33	D20
B3	D2:3	28	D19
B1	D2:2	27	D18
A3	D2:1	26	D17
A1	D2:0	25	D16

Probe Connection D2/D3

APPENDIX C - Necessary Signals for Clocking

To properly acquire SA-110 bus activity in Bus Cycle Clocking mode (see Section 4.0 for further information on this mode), the following signals must be provided: MCLK, APE, nRESET, nWAIT, CLF, and ABORT. If Bus Cycle Clocking does not work, move to the Activity Indicator window of the TLA and observe the following:

MCLK - Should be toggling

APE - Should be steady-state, high or low

nRESET - Should be high for normal operation; low for RESET

nWAIT - May toggle depend on target design; should be high for normal operation

CLF - May toggle depending on target design

ABORT - Should be low for normal operation

When using the NEX-SA110 support in Every Edge of MCLK mode, the only signal that is required is MCLK, and this signal must show activity in the Activity Indicator window of the TLA.

APPENDIX D - Clocking Considerations

Because of timing differences between versions of StrongARM SA-110 micros, and also due to design of the target, it may be necessary to adjust the sample point of some of the acquisition groups for ensure proper data acquisition. The TLA600/700 Logic Analyzer cards require a 2ns stable data window to guarantee data acquisition, and by default this window is defined as 2ns Setup / 0ns Hold relative to the MCLK clock edge. However, this Setup and Hold value can be adjusted on a group-by-group basis to meet the target's timing requirements. This is done by moving to the LA card's Setup window and clicking on the **More** button next to the right of the Clocking field. A window similar to that shown in Figure 4 will appear. In this example the Address, Intrpts, and Misc groups have been left at the Support Package Defaults selection, which is defined as 2ns Setup / 0ns Hold. The Data group has been adjusted to 0ns Setup / 2ns Hold, and the Control group has been adjusted to 1ns Setup / 1ns Hold. When using a TLA running V2.0 software these adjustments are made by left-clicking on the Setup/Hold Window field and then choosing the desired Setup value from the menu field. The process may be slightly different when using V1.1 TLA software.

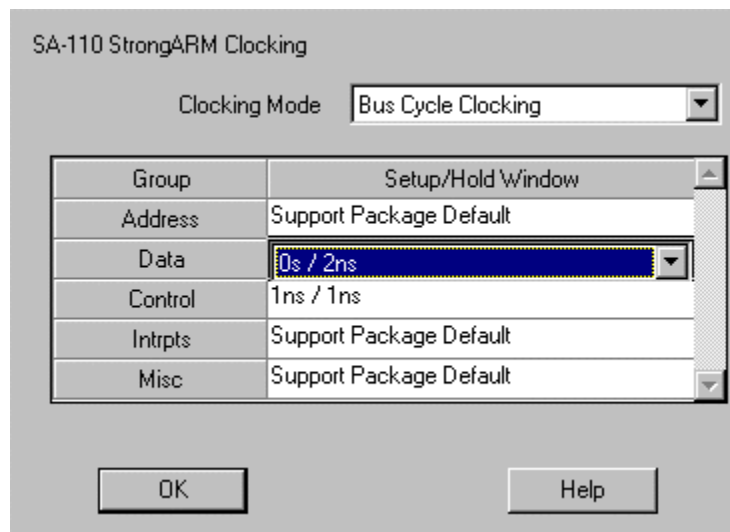


Figure 4- Setup & Hold Adjustment

APPENDIX E - StrongARM SA-110 Pinout

SA110 Pin#	SA110 Signal	SA110 Pin#	SA110 Signal	SA110 Pin#	SA110 Signal	SA110 Pin#	SA110 Signal
1	D[0]	37	D[23]	73	MAS[0]	109	A[22]
2	D[1]	38	D[24]	74	MAS[1]	110	A[23]
3	D[2]	39	D[25]	75	A[0]	111	A[24]
4	D[3]	40	D[26]	76	A[1]	112	A[25]
5	VDD	41	D[27]	77	A[2]	113	VSS
6	VSS	42	VSS	78	VDDX2	114	VDDX2
7	VSS	43	VDDX1	79	VSS	115	A[26]
8	VDDX1	44	D[28]	80	VSS	116	A[27]
9	D[4]	45	D[29]	81	VDD	117	A[28]
10	D[5]	46	D[30]	82	A[3]	118	A[29]
11	D[6]	47	D[31]	83	A[4]	119	A[30]
12	D[7]	48	TDO	84	A[5]	120	A[31]
13	D[8]	49	TDI	85	A[6]	121	APE
14	D[9]	50	nTRST	86	A[7]	122	ABORT
15	D[10]	51	TMS	87	A[8]	123	MCLK
16	D[11]	52	TCK	88	A[9]	124	nMCLK
17	VDDX1	53	n/c	89	A[10]	125	VSS
18	VSS	54	VSS	90	VDD	126	VDDX2
19	VSS	55	VDD	91	VSS	127	nWAIT
20	VDD	56	MSE	92	VSS	128	CLK
21	D[12]	57	CONFIG	93	VDDX2	129	VDD
22	D[13]	58	nMREQ	94	A[11]	130	TCK_BYP
23	D[14]	59	SEQ	95	A[12]	131	TESTCLK
24	D[15]	60	CLF	96	A[13]	132	VSS
25	D[16]	61	LOCK	97	A[14]	133	VDD
26	D[17]	62	nRW	98	A[15]	134	n/c
27	D[18]	63	VSS	99	A[16]	135	n/c
28	D[19]	64	VDDX1	100	A[17]	136	n/c
29	VDDX1	65	SPDF	101	A[18]	137	n/c
30	VSS	66	MCCFG[0]	102	VDDX2	138	CCCFG[1]
31	VSS	67	MCCFG[1]	103	VSS	139	CCCFG[0]
32	VDD	68	MCCFG[2]	104	VSS	140	nPWRSLP
33	D[20]	69	CCCFG[2]	105	VDD	141	nRESET
34	D[21]	70	CCCFG[3]	106	A[19]	142	SnA
35	D[22]	71	nRESET_OUT	107	A[20]	143	nFIQ
36	DBE	72	ABE	108	A[21]	144	nIRQ

APPENDIX F - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX G - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

“Advanced RISC Machines Architectural Reference Manual”

Edited by Dave Jaggard

Document Number ARM DD1 01008

ISBN 0-13-736299-4

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Prentice Hall, New York, NY

Digital Semiconductor SA-110 Microprocessor Technical Reference Manual

Revision C

Document #EC-QPWLC-TE