



NEX-SA11XX

StrongARM Disassembly Software Users Manual

Including these Software Support packages:

BRUTUS SA1100 SA1110

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1.0 OVERVIEW

1.1 General Information

The NEX-SA11XX disassembly software support provides disassembly of acquired StrongARM SA-1100 or SA-1110 bus cycles using a TLA600/700-series logic analyzer. For SA-1100 support a 136-channel acquisition module is required; for SA-1110 support a 102-channel acquisition system is required. In both cases a 100MHz TLA acquisition card is sufficient unless the core clock frequency is expected to approach or exceed 200MHz. The NEX-SA11XX support is software only. Please see Section 3.0 “Connecting to an SA-11XX Target” for information on probing.

The NEX-SA11XX provides full instruction decoding of ARM, though Architecture v4. Thumb instructions are not supported at this time. Note that three different supports are included. One, NEX-SA1100, is to be used with generic SA-1100 designs. A second, NEX-SA1110, is for use with an SA-1110 target. The third, NEX-BRUTUS, is to be used with the Intel SA-1100 Evaluation Board (code-named Brutus). All versions shall be referred to as NEX-SA11XX support except when particular distinctions need to be pointed out.

In practice, the only differences between the NEX-SA1100 support and the NEX-SA1110 support is that the NEX-SA1100 and NEX-Brutus supports work with DRAM memory and the NEX-SA1110 support works with SDRAM memory.

This manual assumes that the user is familiar with the SA-1100/1110 processor specification and the Tektronix TLA600/700 Logic Analyzer. It is also expected that the user is familiar with Windows 95 and/or Windows 98. The TLA600/700 Application must also be at V1.1 or later for the NEX-SA11XX support to work properly.

2.0 SOFTWARE INSTALLATION

Three 3½” diskettes have been included with the NEX-SA11XX disassembly product - one for generic SA-1100 support, another for SA-1110 support, and the third specifically developed for the Intel Brutus (SA-1100) development board. The NEX-SA11XX software is loaded in the same method as other Windows programs. Place the desired Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the Selected support in its proper place on the hard disk.

To load the support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose SA1100, SA1110, or Brutus and click on **Okay**.

3.0 CONNECTING TO AN SA-11XX TARGET

3.1 General Information

It is recommended that the user add Mictor connectors to their target for the interface to the TLA600/700 using Tektronix P6434 high-density probes as we are unaware of a clip to permit acquiring the signals directly from the micro. Table 1 shows the wiring and Channel Grouping required for NEX-SA1100 support; Table 2 shows the same information but for NEX-SA1110 support.

IMPORTANT: Specific wiring must be followed when routing the microprocessor signals to Mictor connectors if NEX-SA1100 or NEX-SA1110 support is going to be used. Appendix A “SA1100 to Mictor Connector Wiring” shows the connections required for the SA1100; Appendix B “SA1110 to Mictor Connector Wiring” shows the wiring required for the SA1110.

3.2 SA-1100 and GP26

The SA-1100 microprocessor does not offer, by default, a clock signal that can be used by a Logic Analyzer to acquire bus information synchronously which makes disassembly support difficult if not impossible. However, there is an option to use one of the General Purpose I/O pins, GP26, to provide a clock that runs at ½ the core clock speed. The SA1100 and Brutus supports **require** that this clock signal be enabled. Sample code to enable this signal and disable the internal data and instruction caches, is provided in Appendix C “Sample Source Code”.

3.3 Intel Brutus Evaluation Board

The Intel Brutus evaluation board has Mictor connectors placed on it for easy access to the SA-1100 signals. However, in order for our Brutus support package to function properly several signals must be moved by using a Nexus Technology NEX-HDSWIZ adapter for the C Group Mictor.

The HD-SWIZ must be modified as follows. The Target end of the HD-SWIZ is considered to be the connector that plugs into the Mictor on the Brutus target. The TLA end of the HD-SWIZ is the connector and latch housing, mounted on the larger PC board, that receives the P6434 probe from the TLA:

Cut the PC board traces for Pins 3, 18, 19, and 36

Connect the following:

Target pin 7 to TLA pin 19

Target pin 9 to TLA pin 3

Target pin 11 to TLA pin 36

Target pin 6 to TLA pin 18

Then the TLA P6434s should be connected to the Brutus board as follows:

A Group Mictor to J11

E Group Mictor to J12

C Group Mictor to J13 (using the HD-SWIZ)

Group Name	Signal Name	SA1100 Pin #	TLA700 input	Group Name	Signal Name	SA1100 Pin #	TLA700 input
Address (Hex)	A25	137	A3:1	Data (Hex)	D31	46	E3:7
	A24	138	A3:0		D30	42	E3:6
	A23	139	A2:7		D29	36	E3:5
	A22	140	A2:6		D28	32	E3:4
	A21	143	A2:5		D27	24	E3:3
	A20	144	A2:4		D26	20	E3:2
	A19	145	A2:3		D25	14	E3:1
	A18	146	A2:2		D24	10	E3:0
	A17	147	A2:1		D23	45	E2:7
	A16	148	A2:0		D22	41	E2:6
	A15	149	A1:7		D21	35	E2:5
	A14	150	A1:6		D20	31	E2:4
	A13	155	A1:5		D19	23	E2:3
	A12	156	A1:4		D18	19	E2:2
	A11	157	A1:3		D17	13	E2:1
	A10	158	A1:2		D16	9	E2:0
	A9	159	A1:1		D15	44	E1:7
	A8	160	A1:0		D14	40	E1:6
	A7	163	A0:7		D13	34	E1:5
	A6	164	A0:6		D12	30	E1:4
A5	165	A0:5	D11	22	E1:3		
A4	166	A0:4	D10	18	E1:2		
A3	167	A0:3	D9	12	E1:1		
A2	168	A0:2	D8	8	E1:0		
A1	169	A0:1	D7	43	E0:7		
A0	170	A0:0	D6	39	E0:6		
DRAMAddr	CASAddr10	---	D2:4	D5	33	E0:5	
	CASAddr9	---	D2:3	D4	29	E0:4	
	CASAddr8	---	D2:2	D3	21	E0:3	
	A21	---	A2:5	D2	17	E0:2	
	A20	---	A2:4	D1	11	E0:1	
	A19	---	A2:3	D0	7	E0:0	
	A18	---	A2:2	Control (Sym)	nOE	118	C2:3
	A17	---	A2:1		nWE	117	C2:2
	A16	---	A2:0	RASLines	nRAS3	121	CK3
	A15	---	A1:7		nRAS2	122	CK2
	A14	---	A1:6		nRAS1	123	C2:1
	A13	---	A1:5		nRAS0	124	C2:0
	A12	---	A1:4	CASLines	nCAS3	125	Q3
	A11	---	A1:3		nCAS2	126	Q2
	A10	---	A1:2		nCAS1	127	Q1
	CASAddr7	---	D2:1		nCAS0	128	Q0
	CASAddr6	---	D2:0	Selects	nCS3	133	C2:7
	CASAddr5	---	D1:7		nCS2	134	C2:6
	CASAddr4	---	D1:6		nCS1	135	C2:5
	CASAddr3	---	D1:5		nCS0	136	C2:4
CASAddr2	---	D1:4	Misc	RCLK_OUT	52	CK1	
CASAddr1	---	D1:3		nRESET_OUT	192	CK0	
CASAddr0	---	D1:2					
DRAM_A1	ground		D1:1				
DRAM_A0	ground		D1:0				

Table 1- SA-1100 TLA600/700 Channel Grouping

Group Name	Signal Name	SA1110 BGA Pad #	TLA700 input	Group Name	Signal Name	SA1110 BGA Pin #	TLA700 input	
Address (Hex)	A25	F16	A3:1	Data (Hex)	D31	M1	D3:7	
	A24	G13	A3:0		D30	L2	D3:6	
	A23	F13	A2:7		D29	K3	D3:5	
	A22	F15	A2:6		D28	J3	D3:4	
	A21	E16	A2:5		D27	H4	D3:3	
	A20	F14	A2:4		D26	G3	D3:2	
	A19	E15	A2:3		D25	F3	D3:1	
	A18	D16	A2:2		D24	E3	D3:0	
	A17	E14	A2:1		D23	M2	D2:7	
	A16	D15	A2:0		D22	L3	D2:6	
	A15	C16	A1:7		D21	K2	D2:5	
	A14	E13	A1:6		D20	J2	D2:4	
	A13	D13	A1:5		D19	G1	D2:3	
	A12	B16	A1:4		D18	G4	D2:2	
	A11	C14	A1:3		D17	E1	D2:1	
	A10	B14	A1:2		D16	D1	D2:0	
	A9	B15	A1:1		D15	L4	D1:7	
	A8	A16	A1:0		D14	K4	D1:6	
	A7	A15	A0:7		D13	J1	D1:5	
	A6	A14	A0:6		D12	J6	D1:4	
	A5	B13	A0:5		D11	H6	D1:3	
	A4	C13	A0:4		D10	F1	D1:2	
	A3	A13	A0:3		D9	E2	D1:1	
	A2	B12	A0:2		D8	D2	D1:0	
	A1	C12	A0:1		D7	L1	D0:7	
	A0	D12	A0:0		D6	K1	D0:6	
DRAMAddr	A24	G13	A3:0		D5	J4	D0:5	
	A23	F13	A2:7		D4	H1	D0:4	
	A22	F15	A2:6		D3	G2	D0:3	
	A21	E16	A2:5		D2	F2	D0:2	
	A20	F14	A2:4		D1	F4	D0:1	
	A19	E15	A2:3		D0	E4	D0:0	
	A18	D16	A2:2		Control (Sym)	nSDRAS	M14	C2:0
	A17	E14	A2:1			nSDCAS	L16	C2:1
	A16	D15	A2:0			nOE	M15	C2:3
	A15	C16	A1:7			nWE	M13	C2:2
	A14	E13	A1:6		Misc (Bin)	SDCLK0	P1	CK3
	A13	D13	A1:5			nRESET_OUT	C7	CK1
	A12	B16	A1:4		SDRAM_CS (Bin)	nSDCS3		C3:3
	A11	C14	A1:3			nSDCS2		C3:2
	A10	B14	A1:2			nSDCS1		C3:1
						nSDCS0		C3:0

Table 2- SA-1110 TLA600/700 Channel Grouping

Group Name	Signal Name	TLA600/700 input	Group Name	Signal Name	TLA600/700 input	
Address (Hex)	A25	A3:1	Data (Hex)	D31	E3:7	
	A24	A3:0		D30	E3:6	
	A23	A2:7		D29	E3:5	
	A22	A2:6		D28	E3:4	
	A21	A2:5		D27	E3:3	
	A20	A2:4		D26	E3:2	
	A19	A2:3		D25	E3:1	
	A18	A2:2		D24	E3:0	
	A17	A2:1		D23	E2:7	
	A16	A2:0		D22	E2:6	
	A15	A1:7		D21	E2:5	
	A14	A1:6		D20	E2:4	
	A13	A1:5		D19	E2:3	
	A12	A1:4		D18	E2:2	
	A11	A1:3		D17	E2:1	
	A10	A1:2		D16	E2:0	
	A9	A1:1		D15	E1:7	
	A8	A1:0		D14	E1:6	
	A7	A0:7		D13	E1:5	
	A6	A0:6		D12	E1:4	
	A5	A0:5		D11	E1:3	
	A4	A0:4		D10	E1:2	
	A3	A0:3		D9	E1:1	
	A2	A0:2		D8	E1:0	
	A1	A0:1		D7	E0:7	
	A0	A0:0		D6	E0:6	
	DRAMAddr	CASAddr9		D2:3	D5	E0:5
		CASAddr8		D2:2	D4	E0:4
A19		A2:3	D3	E0:3		
A18		A2:2	D2	E0:2		
A17		A2:1	D1	E0:1		
A16		A2:0	D0	E0:0		
A15		A1:7	Control (Sym)	LA_OE#	C2:3	
A14		A1:6		LA_WE#	C2:2	
A13		A1:5	RASlines	LA_RAS3#	C3:7	
A12		A1:4		LA_RAS2#	C3:6	
A11		A1:3		LA_RAS1#	C2:1	
A10		A1:2		LA_RAS0#	C2:0	
CASAddr7		D2:1	CASlines	LA_CAS3#	C3:3	
CASAddr6		D2:0		LA_CAS2#	CK3	
CASAddr5		D1:7		LA_CAS1#	C3:1	
CASAddr4		D1:6		LA_CAS0#	Q1	
CASAddr3		D1:5	Selects	LA_CS3#	C2:7	
CASAddr2		D1:4		LA_CS2#	C2:6	
CASAddr1		D1:3		LA_CS1#	C2:5	
CASAddr0		D1:2		LA_CS0#	C2:4	
DRAM_A1	D1:1	Misc	RCLK_OUT	CK1		
DRAM_A0	D1:0					

Table 3- Brutus TLA600/700 Channel Grouping

4.0 CONFIGURING THE SUPPORT

The SA-1100 microprocessor supports the use of DRAM for code execution memory. However, because DRAM is accessed by Row and Column address cycles it becomes more difficult to translate those two cycles into a physical address equivalent which is necessary for tracking the flow of program code. The DRAMAddr group for Brutus support is already configured to properly reconstruct the physical address from Row and Column information. The DRAMAddr group in the SA-1100 support is configured by default for the largest memory configuration possible (16Mb). Some of the bits presently in this group may need to be deleted to reflect a given target. Refer to Section 10.3 (Dynamic Interface Operation) of the *SA-1100 Microprocessor Technical Reference Manual* for information on how the DRAMAddr group should be configured for a specific target.

Note: During testing it appeared as if the complete proper physical address is placed on the Address bus during the Row Address cycle. However, the SA-1100 documentation doesn't appear to mention this, and there was concern that this functionality may not be present in later versions of the micro, so it was decided ignore this and instead create the DRAMAddr group to handle physical memory addresses.

5.0 CLOCK SELECTION

5.1 SA-1100 and Brutus

5.1.1 General Information

There is one clocking option available when using the NEX-SA1100 and NEX-Brutus support packages. The selections for this option are explained in detail below. As previously mentioned these supports are designed to work with DRAM targets only. Please use the NEX-SA1110 support for SDRAM targets.

The clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

NOTE: Depending upon the speed of the SA-1100 micro and the design of the target it may be necessary to adjust the Setup & Hold times for some of the NEX-SA1100 data groups to ensure proper data acquisition. Please refer to Appendix C "Clocking Considerations" for further details.

5.1.2 Clocking Options - Explanation

Clocking Mode - Bus Cycle Clocking is the default clocking selection. In this mode the software monitors the RCLK_OUT, nRAS0-3, and nCAS0-3 signals to permit the acquisition of SA-1100 bus cycles only. All Wait and Idle states will be ignored, offering the best use of your acquisition memory. Refer to Appendix B for more information on how bus cycle data is acquired. **With Every Edge of RCLK** data will be acquired on every edge of the RCLK_OUT signal. The disassembly software will try to filter and display these cycles accordingly, but incorrect decoding may occur because of the

numerous duplicated cycles. This clocking mode shows all bus cycles, including any Wait or idle states. Since no clocking qualification is done only the RCLK signal is needed.

5.2 SA-1110

5.2.1 General Information

There are three clocking select fields available when using the NEX-SA1110 support package. Each is explained in detail below. As previously mentioned the NEX-SA1110 support is designed to work with SDRAM targets only. Please use the NEX-SA1100 support for DRAM targets.

The necessary clocking mode selections are made by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in each Clocking Select field.

NOTE: Depending upon the speed of the SA-1110 micro and the design of the target it may be necessary to adjust the Setup & Hold times for some of the NEX-SA1110 data groups to ensure proper data acquisition. Please refer to Appendix C “Clocking Considerations” for further details.

5.2.2 Clocking Options - Explanation

Clocking Mode - This is set to *Bus Cycle Clocking* by default. In this mode the software monitors the SDCLK0, nRAS, nCAS, and nWE signals to permit the acquisition of valid SA-1110 bus cycles only. All Wait and Idle states will be ignored, offering the best use of your acquisition memory. Refer to Appendix C for more information on how bus cycle data is acquired. Selecting *Rising Edge of SDCLK0* will acquire data on every rising edge of the SDCLK0 signal. The disassembly software will try to filter and display these cycles accordingly, but incorrect decoding may occur because of the numerous duplicated cycles. This clocking mode shows all bus cycles, including any Wait or idle states. Since no clocking qualification is done only the SDCLK0 signal is needed.

CAS Latency – This field should be set to the proper value of the CAS latency for Read cycles. Valid selections are **2** (default), **3**, or **4 SDCLK** cycles. Selecting the incorrect value will result in invalid data acquisition during Read or Fetch cycles.

Read Burst Length – This field must be set to the length of Burst Read Cycles that the target is using. Valid values are **1** (default), **4**, or **8** cycles. The proper value must be set or improper Read and Fetch data acquisition will result.

6.0 VIEWING DATA

6.1 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Disassembly mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the Window pull-down, selecting New Data Window, clicking on Waveform Window Type, then choosing the Data Source. Two choices are presented: SA1100 and SA1100-MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Disassembly window, except in Timing format. The second selection, SA1100-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

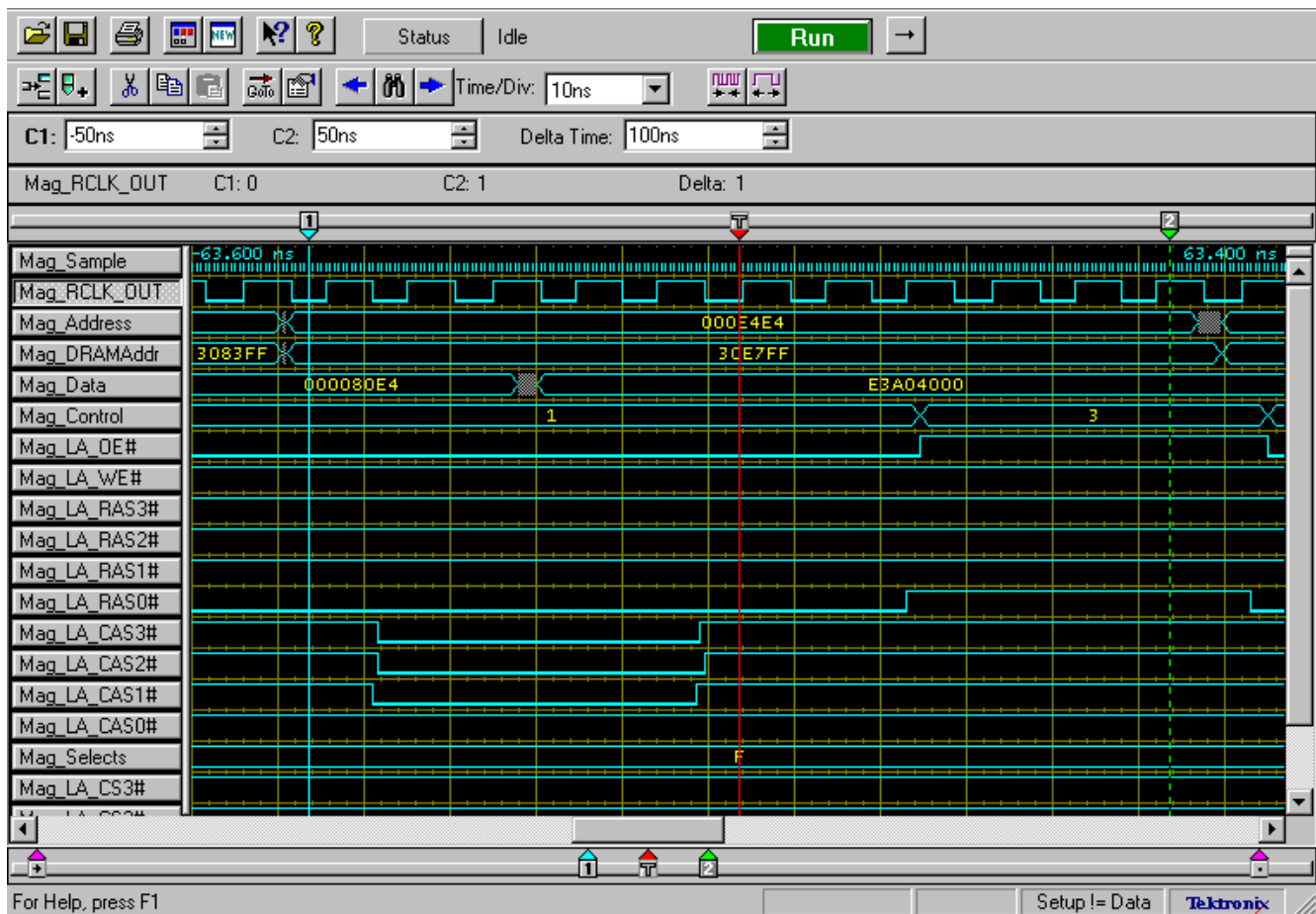


Figure 1- SA1100 MagniVu Display on TLA600/700

7.0 USING THE DISASSEMBLY SOFTWARE

7.1 General Information

The NEX-SA1100 support software acquires and decodes StrongARM SA-1100 bus activity and displays the information as assembly language mnemonics (machine code) - see Figure 2. This permits the tracing of code execution for debug purposes. It is possible to filter the data display cycle types of interest to the software engineer (Figure 3). The user can choose to display the acquired data in Hardware, Software, Control Flow, or Subroutine modes.

A major feature of the NEX-SA1100 software is its ability to intelligently acquire bus cycle information. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the SA1100 software is able to acquire only the valid SA-1100 bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more microprocessor bus cycles. For debug purposes, the user also has the ability to override this function and acquire data on every RCLK edge to permit the user to see all of the bus traffic including the Idle and Wait states. (See Section 5.2 Clocking Options for further information.)

Every stored cycle (bus or clock edge, depending upon clocking selection) has a timestamp value stored with it. This time information, accurate to 500ps in the TLA600/700 series, permits precise measurements of microprocessor bus activity. Because of the design of Tektronix Logic Analyzers there is no need to worry about trading off acquisition memory depth when making these measurements, as the timestamp memory is separate from the acquisition memory.

7.2 Disassembly Using the TLA600/700

The TLA600/700, since it is a Windows program, has the same type of user interface as other Windows-based applications. In the Disassembly Listing window, a tool bar at the top of the window contains buttons that allow the user to modify the display. These buttons, from left to right, perform the following functions:

- Add Column - Adds a column to the display
- Add Mark - Adds a user mark to the display
- Cut - (may be grayed out) - Cuts the selection to the Clipboard
- Copy - (may be grayed out) - Copies the selection to the Clipboard
- Paste - (may be grayed out) - Inserts the contents of the Clipboard
- Go To - Moves the display to the item of interest
- Properties - Edits the current Listing Display properties
- Smaller Font - Decreases the displayed font size
- Larger Font - Increases the displayed font size
- Search Backward - Moves to a previous data match
- Define Search - Define data to be matched
- Search Forward - Moves to the next data match
- Mark Opcode - Permits placing an opcode mark

The format (or display properties) of each displayed column can be changed by putting the mouse cursor on the heading of the column, clicking the left mouse button to select that column, clicking the right mouse button to bring up the editing dialog, then selecting Properties. The column to be modified can also be selected by clicking on the Column tab, selecting the column of interest in the Column field, then making any desired modifications to that display column. The modification or selections possible will vary from column to column.

Two display columns of particular interest are the Timestamp and Mnemonics columns. Timestamp shows a time value associated with the acquisition. By default, Timestamp shows the time from System Trigger. Clicking on the From window in the Timestamp Reference field shows all available selections: Absolute (from when the Logic Analyzer was started), Previous (the time from the present sequence to the previous displayed one), and three selections that permit time to be displayed from different reference points: System Trigger, Cursor 1 Current Position, and Cursor 2 Current Position. Selecting the desired mode with the mouse, and then clicking the left mouse button, will make the selection the present Timestamp display mode.

Sample	Brutus DRAMAddr	Brutus Data	Brutus Mnemonics	Timestamp	Address
0	0080E4	E3A04000	MOV R4, R0, #00 >> 0	0 ps	00080
1	0080E8	EB000F2F	BL 0x0000BDAC	125.500 ns	00080
2	0080EC	E1A01000	MOV R1, R0, RO[FLUSH]	251.000 ns	00080
3	00BDAC	E59FC01C	LDR R12, [R15], #+01C(0x0000BDD0)	376.500 ns	0008D
4	00BDB0	E89C0003	LDMIA R12, R1,RO(0x0000C124)+	502.500 ns	0008D
5	00BDD0	0000C124	(DATA READ)	628.500 ns	0008D
6	00BDB4	E11100A1	TSTS R0, R1, R1, LSR 1	754.500 ns	0008D
7	00C124	55555555	(DATA READ)	880.500 ns	000C1
8	00BDB8	E1B02060	MOVS R2, RO, RO, RRX	1.007,000 us	0008D
9	00C128	55555555	(DATA READ)	1.133,000 us	000C1
10	00BDBC	E0A11001	ADC R1, R1, R1	1.259,500 us	0008D
11	00BDC0	E0222600	EOR R2, R2, RO, LSL 12	1.385,000 us	0008D
12	00BDC4	E0220A22	EOR RO, R2, R2, LSR 20	1.511,000 us	0008D
13	00BDC8	E88C0003	STMIA R12, R1,RO	1.636,500 us	0008D
14	00BDCC	E1A0F00E	MOV R15, RO, R14	1.762,000 us	0008D
15	00C124	FFFFFF55	(WRITE)	1.888,000 us	000C1
16	00BDD0	0000C124	ANDEQ R12, RO, R4, LSR 2[FLUSH]	1.994,500 us	0008D
17	00C128	AAAAAAAB	(WRITE)	2.121,000 us	000C1
18	0080EC	E1A01000	MOV R1, RO, RO	2.227,500 us	00080
19	0080F0	E28F0F05	ADD RO, R15, #05 >> 30	2.353,500 us	00080
20	0080F4	EB00003C	BL 0x000081EC	2.479,500 us	00080
21	0080F8	E2844001	ADD R4, R4, #01 >> 0[FLUSH]	2.605,500 us	00080
22	0081EC	E1A0C00D	MOV R12, RO, R13	2.731,500 us	00081
23	0081F0	E92D000F	STMDB R13!, R3,R2,R1,RO	2.857,500 us	00081
24	0081F4	E92DD800	STMDB R13!, R15,R14,R12,R11	2.983,500 us	00081
25	0081F8	E24CB014	SUB R11, R12, #14 >> 0	3.321,500 us	00081
26	0081FC	E15D000A	CMP R0, R13, R10	3.875,000 us	00081
27	008200	4BFFFFDD	BLMI 0x0000817C	4.107,500 us	00082
28	008204	E24DD03C	SUB R13, R13, #3C >> 0	4.339,000 us	00082
29	008208	E28B0008	ADD RO, R11, #08 >> 0	4.464,000 us	00082
30	00820C	F58D0038	STR RO, [R13], #+038	4.589,500 us	00082

Figure 2- SA1100 Disassembly

The other column of interest is the Mnemonics column, where the SA-1100 disassembly information is displayed. As mentioned previously, it is possible to filter the SA-1100 instructions that are displayed. This is done via selections made in the Disassembly tab of the Properties window (see Figure 3). By default the display is in Hardware mode, where all bus cycles are displayed (Memory Reads, Memory Writes, Instructions, etc.). Other choices are: Software (only executed instructions are displayed), Control Flow (display of instructions affecting code flow such as Jumps, Branches, etc.), and Subroutine (only instructions such as Calls, Returns, etc. are displayed).

Note that when data is suppressed in this fashion that Timestamp information (in Previous form) will be updated to show the time between displayed cycles.

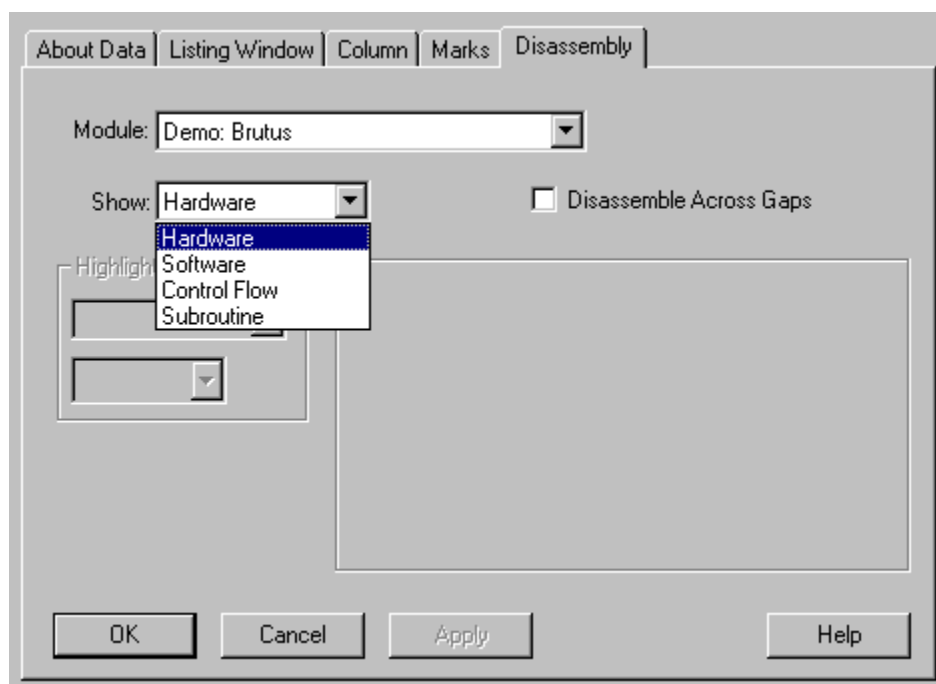


Figure 3- Disassembly Display Filter Window

7.3 Help! The Disassembler's Confused (or: Using Mark Opcode)

Because the SA-1100 does not have a signal to denote an opcode fetch, it is difficult to distinguish between a Read cycle and an Opcode Fetch. The disassembly software does the best it can to figure this out, but it assumes that every Read from contiguous memory cycles is a Fetch, and this may not always be the case. When this happens the user can Mark an Opcode (a Sample or Cycle in the List display) to help the disassembler re-synchronize. To do this, the user first moves the mouse cursor to the cycle that is to be marked. Click on the right mouse button to bring up the menu selections, then click on Mark Opcode. Another window will appear (see Figure 4) which permits selecting the type of cycle that is to be marked (Opcode Fetch, Memory Read, etc.). Select the desired cycle and then click on Okay. To remove an existing Mark, select Undo Mark and then click on OK.

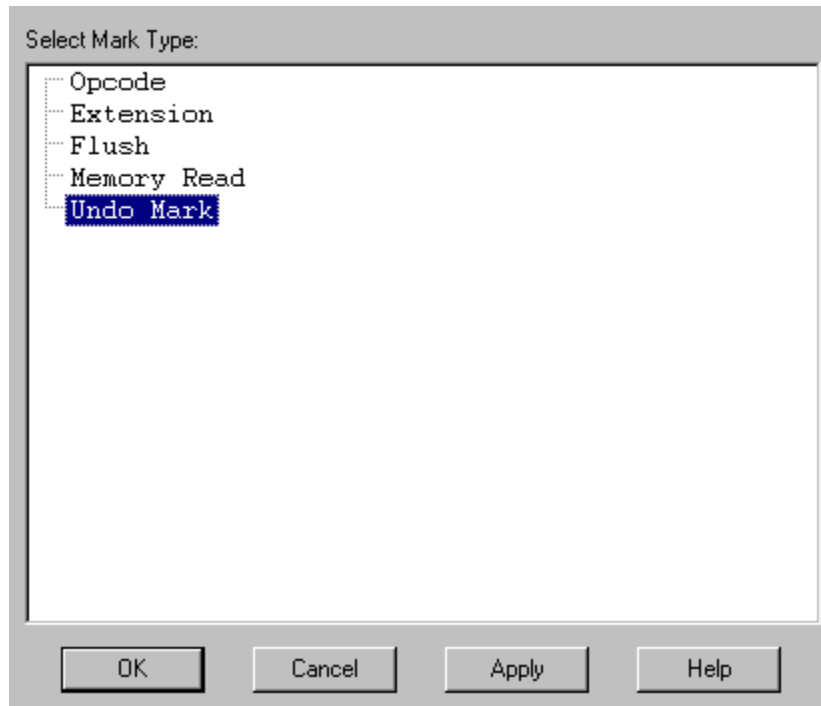


Figure 4- Mark Opcode Window

7.4 Instruction Decoding/Addressing Modes Supported

The following lists the particular StrongARM feature sets that the NEX-SA1100 disassembler packages supports.

IMPORTANT: The Thumb instruction set is not supported at this time.

Architecture v4 Level Instructions and Addressing modes

- Load data read cycle detection
- LDM and LDC multiple load read cycle detection
- Branch Prefetch Instruction flush detection
- Mark-Opcode support

All five addressing modes:

Addressing Mode 1

- Shifter operands
- Immediate
- Register
- Logical shift left by immediate
- Logical shift left by register
- Logical shift right by immediate
- Logical shift right by register
- Arithmetic shift right by immediate
- Arithmetic shift right by register

- Rotate right by immediate
- Rotate right by register
- Rotate right with extend

Addressing Mode 2

- Immediate offset
- Register offset
- Scaled register offset
- Immediate pre-indexed
- Register pre-indexed
- Scaled register pre-indexed
- Immediate post-indexed
- Register post-indexed
- Scaled register post-indexed

Addressing Mode 3

- Immediate offset
- Register offset
- Immediate pre-indexed
- Register pre-indexed
- Immediate post-indexed
- Register post-indexed

Addressing Mode 4

- Increment after
- Increment before
- Decrement after
- Decrement before

Addressing Mode 5

- Immediate offset
- Immediate pre-indexed
- Immediate post-indexed

7.5 SA-1100 Instructions Supported

ADC	{<cond>}{S} Rd, Rn, <shifter_operand>	
ADD	{<cond>}{S} Rd, Rn, <shifter_operand>	
AND	{<cond>}{S} Rd, Rn, <shifter_operand>	
B{L}	{<cond>} <target address>	
BIC	{<cond>}{S} Rd, Rn, <shifter_operand>	
BX	{<cond>} Rm	
CDP	{<cond>} p<cp#>, <opcode_1>, CRd, CRn, CRm, <opcode_2>	
CMN	{<cond>} Rn, <shifter_operand>	
CMP	{<cond>} Rn, <shifter_operand>	
EOR	{<cond>}{S} Rd, Rn, <shifter_operand>	
LDC	{<cond>} p<cp_num>, CRd, <addressing_mode>	
LDM	{<cond>} <addressing_mode> Rn{!}, <registers>	LDM(1)
LDM	{<cond>} <addressing_mode> Rn, <registers>^	LDM(2)

LDM	{<cond>} <addressing_mode> Rn{!}, <registers_and_pc>^	
LDM(3)		
LDR	{<cond>} Rd, <addressing_mode>	
LDR	{<cond>}B Rd, <addressing_mode>	
LDR	{<cond>}BT Rd, <post_indexed_addressing_mode>	
LDR	{<cond>}H Rd, <addressing_mode>	
LDR	{<cond>}SB Rd, <addressing_mode>	
LDR	{<cond>}SH Rd, <addressing_mode>	
LDR	{<cond>}T Rd, <post_indexed_addressing_mode>	
MCR	{<cond>} p<cp#>, <opcode_1>, Rd, CRn, CRm, <opcode_2>	
MLA	{<cond>}{<S>} Rd, Rm, Rs, Rn	
MOV	{<cond>}{S} Rd, <shifter_operand>	
MRC	{<cond>} p<cp#>, <opcode_1>, Rd, CRn, CRm, <opcode_2>	
MRS	{<cond>} Rd, CPSR	
MRS	{<cond>} Rd, SPSR	
MSR	{<cond>} Rd, CPSR_f, #32bit immediate	
MSR	{<cond>} Rd, CPSR_<fields>, Rm	
MSR	{<cond>} Rd, SPSR_f, #32bit immediate	
MSR	{<cond>} Rd, SPSR_<fields>, Rm	
MUL	{<cond>}{<S>}Rd, Rm, Rs	
MVN	{<cond>}{<S>} Rd, <shifter_operand>	
ORR	{<cond>}{S} Rd, Rn, <shifter_operand>	
RSB	{<cond>}{S} Rd, Rn, <shifter_operand>	
RSC	{<cond>}{S} Rd, Rn, <shifter_operand>	
SBC	{<cond>}{S} Rd, Rn, <shifter_operand>	
SMLAL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	
SMULL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	
STC	{<cond>} p<cp_num>, CRd, <addressing_mode>	
STM	{<cond>} <addressing_mode> Rn{!}, <registers>	STM(1)
STM	{<cond>} <addressing_mode> Rn{!}, <registers>^	STM(2)
STR	{<cond>} Rd, <addressing_mode>	
STR	{<cond>}B Rd, <addressing_mode>	
STR	{<cond>}BT Rd, <post_indexed_addressing_mode>	
STR	{<cond>}H Rd, <addressing_mode>	
STR	{<cond>}T Rd, <post_indexed_addressing_mode>	
SUB	{<cond>}{<S>} Rd, Rn, <shifter_operand>	
SWI	{<cond>} <24_bit_immediate>	
SWP	{<cond>} Rd, Rm, [Rn]	
SWP	{<cond>}B Rd, Rm, [Rn]	
TEQ	{<cond>} Rn, <shifter_operand>	
TST	{<cond>} Rn, <shifter_operand>	
UMLAL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	
UMULL	{<cond>}{<S>} RdLo, RdHi, Rm, Rs	

8.0 CONTROL GROUP SYMBOL TABLES

The use of Symbol Tables when displaying state data and defining a trigger enables the user to quickly determine the type of bus cycle that occurred or is desired. Symbol tables for the Control group (SA1100_Ctrl / NEX-Brutus Table 4 and SA1110_Ctrl Table 5) have been provided to quickly show the type of bus transaction acquired when viewing data in Listing display. This same symbol table can be used in the Trigger area of the TLA to easily define the sort of bus cycle that is to be triggered on.

Pattern	TLA600/700 Symbols	Meaning
01	READ/FETCH	Read or Fetch Cycle
10	WRITE	Write Cycle

Table 4- NEX-SA1100 / NEX-Brutus Control Symbol Table

Signals, from left to right: nOE, nWE

Pattern	TLA600/700 Symbols	Meaning
1xx1	READ/FETCH	Read or Fetch Cycle
1xx0	WRITE	Write Cycle
01xx	RAS_CYCLE	RAS Address Cycle
10xx	CAS_CYCLE	CAS Address Cycle
00xx	REFRESH	Memory Refresh Cycle

Table 5- NEX-SA1110 Control Symbol Table

Signals, from left to right: nSDRAS, nSDCAS, nOE, nWE

APPENDIX A - NEX-SA1100 Mictor Wiring

NOTES: The pin numbers are identical for the 208-pin Quad Flat Pack and 256-pin Mini-Ball Grid Array packages. Blank entries in the SA1100 Pin # and Signal columns denote unused TLA inputs that can be wired to any user signal. Please refer to the manual from Tektronix for the P6434 High Density probes for important information on designing the necessary connectors into a target system.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #
3	5	CK0	nRESET_OUT	192	36	6	CK1	GP26	52
4	7	A3:7			35	8	A1:7	A15	149
5	9	A3:6			34	10	A1:6	A14	150
6	11	A3:5			33	12	A1:5	A13	155
7	13	A3:4			32	14	A1:4	A12	156
8	15	A3:3			31	16	A1:3	A11	157
9	17	A3:2			30	18	A1:2	A10	158
10	19	A3:1	A25	137	29	20	A1:1	A9	159
11	21	A3:0	A24	138	28	22	A1:0	A8	160
12	23	A2:7	A23	139	27	24	A0:7	A7	163
13	25	A2:6	A22	140	26	26	A0:6	A6	164
14	27	A2:5	A21	143	25	28	A0:5	A5	165
15	29	A2:4	A20	144	24	30	A0:4	A4	166
16	31	A2:3	A19	145	23	32	A0:3	A3	167
17	33	A2:2	A18	146	22	34	A0:2	A2	168
18	35	A2:1	A17	147	21	36	A0:1	A1	169
19	37	A2:0	A16	148	20	38	A0:0	A0	170

Mictor Group A

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #
3	5	CK3	nRAS3	121	36	6	Q1	nCAS1	127
4	7	C3:7			35	8	C1:7		
5	9	C3:6			34	10	C1:6		
6	11	C3:5			33	12	C1:5		
7	13	C3:4			32	14	C1:4		
8	15	C3:3			31	16	C1:3		
9	17	C3:2			30	18	C1:2		
10	19	C3:1			29	20	C1:1		
11	21	C3:0			28	22	C1:0		
12	23	C2:7	nCS3	133	27	24	C0:7		
13	25	C2:6	nCS2	134	26	26	C0:6		
14	27	C2:5	nCS1	135	25	28	C0:5		
15	29	C2:4	nCS0	136	24	30	C0:4		
16	31	C2:3	nOE	118	23	32	C0:3		
17	33	C2:2	nWE	117	22	34	C0:2		
18	35	C2:1	nRAS1	123	21	36	C0:1		
19	37	C2:0	nRAS0	124	20	38	C0:0		

Mictor Group C

APPENDIX A - NEX-SA1100 Mictor Wiring (cont'd)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #
3	5	Q0	nCAS0	128	36	6	CK2	nRAS2	122
4	7	D3:7			35	8	D1:7	Do Not Use	DNU
5	9	D3:6			34	10	D1:6	Do Not Use	DNU
6	11	D3:5			33	12	D1:5	Do Not Use	DNU
7	13	D3:4			32	14	D1:4	Do Not Use	DNU
8	15	D3:3			31	16	D1:3	Do Not Use	DNU
9	17	D3:2			30	18	D1:2	Do Not Use	DNU
10	19	D3:1			29	20	D1:1	Do Not Use	DNU
11	21	D3:0			28	22	D1:0	Do Not Use	DNU
12	23	D2:7	Do Not Use	DNU	27	24	D0:7		
13	25	D2:6	Do Not Use	DNU	26	26	D0:6		
14	27	D2:5	Do Not Use	DNU	25	28	D0:5		
15	29	D2:4	Do Not Use	DNU	24	30	D0:4		
16	31	D2:3	Do Not Use	DNU	23	32	D0:3		
17	33	D2:2	Do Not Use	DNU	22	34	D0:2		
18	35	D2:1	Do Not Use	DNU	21	36	D0:1		
19	37	D2:0	Do Not Use	DNU	20	38	D0:0		

Mictor Group D

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1100 Signal	SA1100 Pin #
3	5	Q3	nCAS3	125	36	6	Q2	nCAS2	126
4	7	E3:7	D31	46	35	8	E1:7	D15	44
5	9	E3:6	D30	42	34	10	E1:6	D14	40
6	11	E3:5	D29	36	33	12	E1:5	D13	34
7	13	E3:4	D28	32	32	14	E1:4	D12	30
8	15	E3:3	D27	24	31	16	E1:3	D11	22
9	17	E3:2	D26	20	30	18	E1:2	D10	18
10	19	E3:1	D25	14	29	20	E1:1	D9	12
11	21	E3:0	D24	10	28	22	E1:0	D8	8
12	23	E2:7	D23	45	27	24	E0:7	D7	43
13	25	E2:6	D22	41	26	26	E0:6	D6	39
14	27	E2:5	D21	35	25	28	E0:5	D5	33
15	29	E2:4	D20	31	24	30	E0:4	D4	29
16	31	E2:3	D19	23	23	32	E0:3	D3	21
17	33	E2:2	D18	19	22	34	E0:2	D2	17
18	35	E2:1	D17	13	21	36	E0:1	D1	11
19	37	E2:0	D16	9	20	38	E0:0	D0	7

Mictor Group E

APPENDIX B - NEX-SA1100 P6860 Compression Pinout

NOTES: The pin numbers are identical for the 208-pin Quad Flat Pack and 256-pin Mini-Ball Grid Array packages. Blank entries in the SA1100 Pin # and Signal columns denote unused TLA inputs that can be wired to any user signal. For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	CK1-	Gnd	Gnd
A13	CK1+	GP26	52
B12	A1:7	A15	149
B10	A1:6	A14	150
A12	A1:5	A13	155
A10	A1:4	A12	156
B9	A1:3	A11	157
B7	A1:2	A10	158
A9	A1:1	A9	159
A7	A1:0	A8	160
B6	A0:7	A7	163
B4	A0:6	A6	164
A6	A0:5	A5	165
A4	A0:4	A4	166
B3	A0:3	A3	167
B1	A0:2	A2	168
A3	A0:1	A1	169
A1	A0:0	A0	170

Probe Connection A0/A1

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	CK0-	Gnd	Gnd
A13	CK0+	nRESET_OUT	192
B12	A3:7		
B10	A3:6		
A12	A3:5		
A10	A3:4		
B9	A3:3		
B7	A3:2		
A9	A3:1	A25	137
A7	A3:0	A24	138
B6	A2:7	A23	139
B4	A2:6	A22	140
A6	A2:5	A21	143
A4	A2:4	A20	144
B3	A2:3	A19	145
B1	A2:2	A18	146
A3	A2:1	A17	147
A1	A2:0	A16	148

Probe Connection A2/A3

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	Q1-	Gnd	Gnd
A13	Q1+	nCAS1	127
B12	C1:7		
B10	C1:6		
A12	C1:5		
A10	C1:4		
B9	C1:3		
B7	C1:2		
A9	C1:1		
A7	C1:0		
B6	C0:7		
B4	C0:6		
A6	C0:5		
A4	C0:4		
B3	C0:3		
B1	C0:2		
A3	C0:1		
A1	C0:0		

Probe Connection C0/C1

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	nRAS3	121
B12	C3:7		
B10	C3:6		
A12	C3:5		
A10	C3:4		
B9	C3:3		
B7	C3:2		
A9	C3:1		
A7	C3:0		
B6	C2:7	nCS3	133
B4	C2:6	nCS2	134
A6	C2:5	nCS1	135
A4	C2:4	nCS0	136
B3	C2:3	nOE	118
B1	C2:2	nWE	117
A3	C2:1	nRAS1	123
A1	C2:0	nRAS0	124

Probe Connection C2/C3

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	CK2-	Gnd	Gnd
A13	CK2+	nRAS2	122
B12	D1:7	Do Not Use	DNU
B10	D1:6	Do Not Use	DNU
A12	D1:5	Do Not Use	DNU
A10	D1:4	Do Not Use	DNU
B9	D1:3	Do Not Use	DNU
B7	D1:2	Do Not Use	DNU
A9	D1:1	Do Not Use	DNU
A7	D1:0	Do Not Use	DNU
B6	D0:7		
B4	D0:6		
A6	D0:5		
A4	D0:4		
B3	D0:3		
B1	D0:2		
A3	D0:1		
A1	D0:0		

Probe Connection D0/D1

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	Q0-	Gnd	Gnd
A13	Q0+	nCAS0	128
B12	D3:7		
B10	D3:6		
A12	D3:5		
A10	D3:4		
B9	D3:3		
B7	D3:2		
A9	D3:1		
A7	D3:0		
B6	D2:7	Do Not Use	DNU
B4	D2:6	Do Not Use	DNU
A6	D2:5	Do Not Use	DNU
A4	D2:4	Do Not Use	DNU
B3	D2:3	Do Not Use	DNU
B1	D2:2	Do Not Use	DNU
A3	D2:1	Do Not Use	DNU
A1	D2:0	Do Not Use	DNU

Probe Connection D2/D3

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	Q2-	Gnd	Gnd
A13	Q2+	nCAS2	126
B12	E1:7	D15	44
B10	E1:6	D14	40
A12	E1:5	D13	34
A10	E1:4	D12	30
B9	E1:3	D11	22
B7	E1:2	D10	18
A9	E1:1	D9	12
A7	E1:0	D8	8
B6	E0:7	D7	43
B4	E0:6	D6	39
A6	E0:5	D5	33
A4	E0:4	D4	29
B3	E0:3	D3	21
B1	E0:2	D2	17
A3	E0:1	D1	11
A1	E0:0	D0	7

Probe Connection E0/E1

Pad #	TLA Channel	SA1100 Signal Name	SA1100 Pin #
A15	Q3-	Gnd	Gnd
A13	Q3+	nCAS3	125
B12	E3:7	D31	46
B10	E3:6	D30	42
A12	E3:5	D29	36
A10	E3:4	D28	32
B9	E3:3	D27	24
B7	E3:2	D26	20
A9	E3:1	D25	14
A7	E3:0	D24	10
B6	E2:7	D23	45
B4	E2:6	D22	41
A6	E2:5	D21	35
A4	E2:4	D20	31
B3	E2:3	D19	23
B1	E2:2	D18	19
A3	E2:1	D17	13
A1	E2:0	D16	9

Probe Connection E2/E3

APPENDIX C - NEX-SA1110 Mictor Wiring

NOTES: The pin numbers are for the 256-pin Mini-Ball Grid Array packages. Blank entries in the SA1110 Pin # and Signal columns denote unused TLA inputs that can be wired to any user signal. Please refer to the manual from Tektronix for the P6434 High Density probes for important information on designing the necessary connectors into a target system.

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1110 Signal	SA1110 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1110 Signal	SA1110 Pin #
3	5	CK0			36	6	CK1	nRESET_OUT	C7
4	7	A3:7			35	8	A1:7	A15	C16
5	9	A3:6			34	10	A1:6	A14	E13
6	11	A3:5			33	12	A1:5	A13	D13
7	13	A3:4			32	14	A1:4	A12	B16
8	15	A3:3			31	16	A1:3	A11	C14
9	17	A3:2			30	18	A1:2	A10	B14
10	19	A3:1	A25	F16	29	20	A1:1	A9	B15
11	21	A3:0	A24	G13	28	22	A1:0	A8	A16
12	23	A2:7	A23	F13	27	24	A0:7	A7	A15
13	25	A2:6	A22	F15	26	26	A0:6	A6	A14
14	27	A2:5	A21	E16	25	28	A0:5	A5	B13
15	29	A2:4	A20	F14	24	30	A0:4	A4	C13
16	31	A2:3	A19	E15	23	32	A0:3	A3	A13
17	33	A2:2	A18	D16	22	34	A0:2	A2	B12
18	35	A2:1	A17	E14	21	36	A0:1	A1	C12
19	37	A2:0	A16	D15	20	38	A0:0	A0	D12

Mictor Group A

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1110 Signal	SA1110 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1110 Signal	SA1110 Pin #
3	5	CK3	SDCLK0	P1	36	6	Q1		
4	7	C3:7	DQM3	K13	35	8	C1:7		
5	9	C3:6	DQM2	K15	34	10	C1:6		
6	11	C3:5	DQM1	J15	33	12	C1:5		
7	13	C3:4	DQM0	J14	32	14	C1:4		
8	15	C3:3	nSDCS3	L15	31	16	C1:3		
9	17	C3:2	nSDCS2	L14	30	18	C1:2		
10	19	C3:1	nSDCS1	L13	29	20	C1:1		
11	21	C3:0	nSDCS0	K16	28	22	C1:0		
12	23	C2:7			27	24	C0:7		
13	25	C2:6			26	26	C0:6		
14	27	C2:5			25	28	C0:5		
15	29	C2:4			24	30	C0:4		
16	31	C2:3	nOE	M15	23	32	C0:3		
17	33	C2:2	nWE	M13	22	34	C0:2		
18	35	C2:1	nSDCAS	L16	21	36	C0:1		
19	37	C2:0	nSDRAS	M14	20	38	C0:0		

Mictor Group C

APPENDIX C - NEX-SA1110 Mictor Wiring (cont'd)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1110 Signal	SA1110 Pin #	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SA1110 Signal	SA1110 Pin #
3	5	Q0			36	6	CK2		
4	7	D3:7	D31	M1	35	8	D1:7	D15	L4
5	9	D3:6	D30	L2	34	10	D1:6	D14	K4
6	11	D3:5	D29	K3	33	12	D1:5	D13	J1
7	13	D3:4	D28	J3	32	14	D1:4	D12	J6
8	15	D3:3	D27	H4	31	16	D1:3	D11	H6
9	17	D3:2	D26	G3	30	18	D1:2	D10	F1
10	19	D3:1	D25	F3	29	20	D1:1	D9	E2
11	21	D3:0	D24	E3	28	22	D1:0	D8	D2
12	23	D2:7	D23	M2	27	24	D0:7	D7	L1
13	25	D2:6	D22	L3	26	26	D0:6	D6	K1
14	27	D2:5	D21	K2	25	28	D0:5	D5	J4
15	29	D2:4	D20	J2	24	30	D0:4	D4	H1
16	31	D2:3	D19	G1	23	32	D0:3	D3	G2
17	33	D2:2	D18	G4	22	34	D0:2	D2	F2
18	35	D2:1	D17	E1	21	36	D0:1	D1	F4
19	37	D2:0	D16	D1	20	38	D0:0	D0	E4

Mictor Group D

APPENDIX D - NEX-SA1110 P6860 Compression Pinout

NOTES: The pin numbers are for the 256-pin Mini-Ball Grid Array packages. Blank entries in the SA1110 Pin # and Signal columns denote unused TLA inputs that can be wired to any user signal. For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

Pad #	TLA Channel	SA1110 Signal Name	SA1110 Pin #
A15	CK1-	Gnd	Gnd
A13	CK1+	nRESET_OUT	C7
B12	A1:7	A15	C16
B10	A1:6	A14	E13
A12	A1:5	A13	D13
A10	A1:4	A12	B16
B9	A1:3	A11	C14
B7	A1:2	A10	B14
A9	A1:1	A9	B15
A7	A1:0	A8	A16
B6	A0:7	A7	A15
B4	A0:6	A6	A14
A6	A0:5	A5	B13
A4	A0:4	A4	C13
B3	A0:3	A3	A13
B1	A0:2	A2	B12
A3	A0:1	A1	C12
A1	A0:0	A0	D12

Probe Connection A0/A1

Pad #	TLA Channel	SA1110 Signal Name	SA1110 Pin #
A15	CK0-	Gnd	Gnd
A13	CK0+		
B12	A3:7		
B10	A3:6		
A12	A3:5		
A10	A3:4		
B9	A3:3		
B7	A3:2		
A9	A3:1	A25	F16
A7	A3:0	A24	G13
B6	A2:7	A23	F13
B4	A2:6	A22	F15
A6	A2:5	A21	E16
A4	A2:4	A20	F14
B3	A2:3	A19	E15
B1	A2:2	A18	D16
A3	A2:1	A17	E14
A1	A2:0	A16	D15

Probe Connection A2/A3

Pad #	TLA Channel	SA1110 Signal Name	SA1110 Pin #
A15	Q1-	Gnd	Gnd
A13	Q1+		
B12	C1:7		
B10	C1:6		
A12	C1:5		
A10	C1:4		
B9	C1:3		
B7	C1:2		
A9	C1:1		
A7	C1:0		
B6	C0:7		
B4	C0:6		
A6	C0:5		
A4	C0:4		
B3	C0:3		
B1	C0:2		
A3	C0:1		
A1	C0:0		

Probe Connection C0/C1

Pad #	TLA Channel	SA1110 Signal Name	SA1110 Pin #
A15	CK3-	Gnd	Gnd
A13	CK3+	SDCLK0	P1
B12	C3:7	DQM3	K13
B10	C3:6	DQM2	K15
A12	C3:5	DQM1	J15
A10	C3:4	DQM0	J14
B9	C3:3	nSDCS3	L15
B7	C3:2	nSDCS2	L14
A9	C3:1	nSDCS1	L13
A7	C3:0	nSDCS0	K16
B6	C2:7		
B4	C2:6		
A6	C2:5		
A4	C2:4		
B3	C2:3	nOE	M15
B1	C2:2	nWE	M13
A3	C2:1	nSDCAS	L16
A1	C2:0	nSDRAS	M14

Probe Connection C2/C3

Pad #	TLA Channel	SA1110 Signal Name	SA1110 Pin #
A15	CK2-	Gnd	Gnd
A13	CK2+		
B12	D1:7	D15	L4
B10	D1:6	D14	K4
A12	D1:5	D13	J1
A10	D1:4	D12	J6
B9	D1:3	D11	H6
B7	D1:2	D10	F1
A9	D1:1	D9	E2
A7	D1:0	D8	D2
B6	D0:7	D7	L1
B4	D0:6	D6	K1
A6	D0:5	D5	J4
A4	D0:4	D4	H1
B3	D0:3	D3	G2
B1	D0:2	D2	F2
A3	D0:1	D1	F4
A1	D0:0	D0	E4

Probe Connection D0/D1

Pad #	TLA Channel	SA1110 Signal Name	SA1110 Pin #
A15	Q0-	Gnd	Gnd
A13	Q0+		
B12	D3:7	D31	M1
B10	D3:6	D30	L2
A12	D3:5	D29	K3
A10	D3:4	D28	J3
B9	D3:3	D27	H4
B7	D3:2	D26	G3
A9	D3:1	D25	F3
A7	D3:0	D24	E3
B6	D2:7	D23	M2
B4	D2:6	D22	L3
A6	D2:5	D21	K2
A4	D2:4	D20	J2
B3	D2:3	D19	G1
B1	D2:2	D18	G4
A3	D2:1	D17	E1
A1	D2:0	D16	D1

Probe Connection D2/D3

APPENDIX E - Necessary Signals for Clocking

To properly acquire SA-1100 bus activity in Bus Cycle Clocking mode (see Section 5.0 for further information on this mode), the following signals must be provided: RCLK_OUT, nRAS0-3, and nCAS0-3. If Bus Cycle Clocking does not work, move to the Activity Indicator window of the TLA and observe that all of these signals are toggling.

When using the NEX-SA1100 support in Every Edge of RCLK mode, the only signal that is required is RCLK_OUT, and this signal must show activity in the Activity Indicator window of the TLA.

APPENDIX F - SAMPLE SOURCE CODE

As previously mentioned it is necessary to define the GP26 signal as an external clock source for micro data to be acquired synchronously by the Logic Analyzer. It is also strongly recommended that both the instruction and data caches be disabled to permit the Analyzer to better track the flow of the code and we have provided some examples to do this. The code is available on the TLA's hard disk in one of the following folders (depending upon which support was loaded):

```
C:\Program Files\TLA 700\Supports\Brutus
C:\Program Files\TLA 700\Supports\SA1100
```

with the filename **NewWaveInit.s** . The code is also listed below:

```
; turns on external rclk
; disables both icache and dcache
;

GPIODirect EQU 0x90040004
GPIOAltFunc EQU 0x9004001c

RclkMask EQU 0x04000000

TUCRegister EQU 0x90030008

Bit31Mask EQU 0x80000000

EnableDcache EQU 0x4
EnableWB EQU 0x8
EnableIcache EQU 0x1000

FlushCacheOPC2 EQU 0x0
FlushCacheCRm EQU 0x7

SWI_Angel EQU 0x123456
angel_SWIreason_EnterSVC EQU 0x17

AREA |Random$$code|, CODE, READONLY

EXPORT NewWaveInit

NewWaveInit

STMFD sp!, {v1-v3, lr} ; save working registers
MOV v3, sp ; save stack pointer...

; must enter supervisor mode to disable caches
```

```

MOV r0, #angel_SWIreason_EnterSVC ; Enter SVC mode
SWI SWI_Angel           ; Returns EnterUSR routine in r0

MRC p15, 0, r4, c1, c0 ,0 ; read the control register
BIC r4, r4, #EnableIcache ; turn off Icache
BIC r4, r4, #EnableDcache ; turn off Dcache
BIC r4, r4, #EnableWB
MCR p15, 0, r4, c1, c0 ,0 ; write the control register

; now back to user mode
MOV sp, v3      ; restore stack pointer
LDMFD sp!, {v1-v3, lr} ; restore registers

; now we must flush the icache, we flush both
; because nothing of significance to the user has
; happened so far, we want all data reads to show up
; and we just restored all the registers from the stack
; (which may have been cached)
MOV r4, #0
MCR p15, 0, r4, c7, c7, 0

LDR r0, =GPIODirect ; GPDR - GPIO Direction Register
LDR r1, =GPIOAltFunc ; GAFR - GPIO Alternate Function Register
LDR r2, =RclkMask ; GPIO26 (rclk) Mask Bit

; We must set GPIO Direction and GPIO Alternate Function Registers
; Bit 26 on to enable RCLK_OUT
LDR r3, [r0] ; Get current GPDR contents
LDR r4, [r1] ; Get current GAFR contents
ORR r5, r3, r2 ; Set Bit 26 true (1)
STR r5, [r0] ; Write GPDR to set Bit 26 as an Output
ORR r5, r4, r2 ; Set Bit 26 true (1)
STR r5, [r1] ; Write GAFR Bit 26 for RCLK_OUT

; We must also set Bit 31 of TUCR to output clock
LDR r0, =TUCRegister ; TUCR - Test Control Register
LDR r1, =Bit31Mask ; Bit 31 Mask
LDR r3, [r0] ; Get current TUCR contents
ORR r5, r3, r1 ; Set Bit 31 true (1)
STR r5, [r0] ; Write TUCR to set Bit 31

```

END

APPENDIX G - Clocking Considerations

Because of timing differences between versions of StrongARM SA-1100 micro, and also due to design of the target, it may be necessary to adjust the sample point of some of the acquisition groups for ensure proper data acquisition. The TLA600/700 Logic Analyzer cards require a 2ns stable data window to guarantee data acquisition, and by default this window is defined as 2ns Setup / 0ns Hold (for all groups) relative to the RCLK_OUT clock edge. However, this Setup and Hold value can be adjusted on a group-by-group basis to meet the target's timing requirements. This is done by moving to the LA card's Setup window and clicking on the **More** button next to the right of the Clocking field. A window similar to that shown in Figure 4 will appear. In this example the Address, DRAMAddr, Control and RASAddr groups have been left at the Support Package Defaults selection, which is defined as 2ns Setup / 0ns Hold. The Data group has been adjusted to 1ns Setup / 1ns Hold. When using a TLA running V3.0 software these adjustments are made by left-clicking on the Setup/Hold Window field and then choosing the desired Setup value from the menu field. The process may be slightly different when using earlier versions of TLA software.

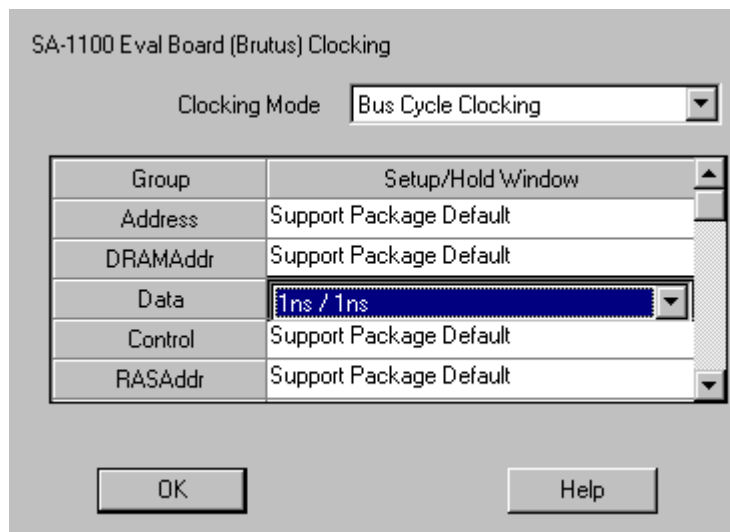


Figure 5- Setup & Hold Adjustment

The same concerns exist for the SA-1110 micro and designs using it. The data groups that may need to be adjusted are the Address, DRAMAddr, Data, and Control groups.

APPENDIX H - StrongARM SA-1100 Pinout

This table shows the pinouts for the 208-pin Quad Flat Pack and 256-pin mini-BGA packages:

QFP Pin #	MBGA Pin #	SA1100 Signal	QFP Pin #	MBGA Pin #	SA1100 Signal	QFP Pin #	MBGA Pin #	SA1100 Signal	QFP Pin #	MBGA Pin #	SA1100 Signal
1	B1	RXD_C	53	R2	GP[25]	105	P14	nPIOR	157	C14	A[11]
2	C2	TXD_C	54	P4	GP[24]	106	P15	nPIOW	158	B14	A[10]
3	J13	VDDX2	55	T2	GP[23]	107	F11	VSSX	159	B15	A[9]
4	A1	VSSX	56	R3	GP[22]	108	L4	VDDX2	160	A16	A[8]
5	C1	VDD	57	D5	VDDX1	109	T16	VSS	161	G10	VSSX
6	D3	VSS	58	F6	VSSX	110	R16	VDD	162	E6	VDDX1
7	D2	D[0]	59	T3	GP[21]	111	P16	PSKTSEL	163	A15	A[7]
8	D1	D[8]	60	R4	GP[20]	112	N15	nIOIS16	164	A14	A[6]
9	F4	D[16]	61	T4	GP[19]	113	N16	nPWAIT	165	B13	A[5]
10	E3	D[24]	62	P5	GP[18]	114	N14	nPREG	166	C13	A[4]
11	E2	D[1]	63	R5	GP[17]	115	M13	nPCE2	167	A13	A[3]
12	E1	D[9]	64	T5	GP[16]	116	M15	nPCE1	168	B12	A[2]
13	F3	D[17]	65	N6	GP[15]	117	M14	nWE	169	C12	A[1]
14	F2	D[25]	66	P6	GP[14]	118	M16	nOE	170	D12	A[0]
15	K5	VDDX2	67	D9	VDDX1	119	G6	VSSX	171	G11	VSSX
16	B2	VSSX	68	F7	VSSX	120	L5	VDDX2	172	E7	VDDX1
17	F1	D[2]	69	R6	GP[13]	121	L15	nRAS[3]	173	A12	UDC-
18	G2	D[10]	70	R7	GP[12]	122	L14	nRAS[2]	174	C11	UDC+
19	G3	D[18]	71	T6	GP[11]	123	L16	nRAS[1]	175	B11	RXD_1
20	H4	D[26]	72	P7	GP[10]	124	K13	nRAS[0]	176	A11	TXD_1
21	G1	D[9]	73	T7	GP[9]	125	K15	nCAS[3]	177	B10	RXD_2
22	H3	D[11]	74	N8	GP[8]	126	K14	nCAS[2]	178	D10	TXD_2
23	H2	D[19]	75	P8	GP[7]	127	K16	nCAS[1]	179	C10	RXD_3
24	J3	D[27]	76	R8	GP[6]	128	J15	nCAS[0]	180	A10	TXD_3
25	H1	VDD	77	K10	VDDX1	129	G7	VSSX	181	H6	VSSX
26	J2	VSS	78	F8	VSSX	130	L12	VDDX2	182	L10	VDDX1
27	D13	VDDX2	79	T8	VDD	131	J16	VSS	183	A9	VSS
28	C3	VSSX	80	R9	VSS	132	J14	VDD	184	B9	TXTAL
29	J1	D[4]	81	P9	GP[5]	133	H14	nCS[3]	185	C9	TEXTAL
30	K4	D[12]	82	T9	GP[4]	134	H13	nCS[2]	186	A8	PEXTAL
31	K3	D[20]	83	N10	GP[3]	135	H16	nCS[1]	187	B8	PXTAL
32	K2	D[28]	84	R10	GP[2]	136	H15	nCS[0]	188	C8	VDDP
33	K1	D[5]	85	P10	GP[1]	137	G14	A[25]	189	D8	VSS
34	L3	D[13]	86	T10	GP[0]	138	G16	A[24]	190	A7	VDD
35	L2	D[21]	87	R11	L_BIAS	139	G15	A[23]	191	B7	nRESET
36	L1	D[29]	88	P11	L_PCLK	140	F15	A[22]	192	C7	nRESET_OUT
37	K12	VDDX2	89	D11	VDDX1	141	G8	VSSX	193	D7	VDDX3
38	D4	VSSX	90	F9	VSSX	142	L13	VDDX2	194	D6	ROMSEL
39	M4	D[6]	91	N12	LDD0	143	F14	A[21]	195	A6	TCK_BYP
40	M3	D[14]	92	T11	LDD1	144	F13	A[20]	196	B6	TESTCLK
41	M2	D[22]	93	R12	LDD2	145	F16	A[19]	197	C6	TMS
42	M1	D[30]	94	P12	LDD3	146	E15	A[18]	198	C5	TCK
43	N3	D[7]	95	P13	LDD4	147	E14	A[17]	199	A5	TDI
44	N2	D[15]	96	T12	LDD5	148	E16	A[16]	200	B5	TDO
45	P3	D[23]	97	R13	LDD6	149	D14	A[15]	201	B4	nTRST
46	P2	D[31]	98	T13	LDD7	150	D15	A[14]	202	A4	BATT_FAULT
47	N1	VDD	99	K11	VDDX1	151	D16	VSS	203	H7	VSSX
48	P1	VSS	100	F10	VSSX	152	C15	VDD	204	E8	VDDX1
49	E4	VDDX2	101	R14	L_LCLK	153	G9	VSSX	205	C4	VDD_FAULT
50	E5	VSSX	102	T14	L_FCLK	154	M5	VDDX2	206	A3	PWR_EN
51	R1	GP[27]	103	R15	nPOE	155	C16	A[13]	207	B3	SFRM_C
52	T1	GP[26]	104	t15	nPWE	156	B16	A[12]	208	A2	SCLK_C

APPENDIX I - StrongARM SA-1110 Pinout

This table shows the pinout for the 256-pin mini-BGA package:

Pin	MBGA PIN#	SA1110 Signal	Pin	MBGA PIN#	SA1110 Signal	Pin	MBGA PIN#	SA1110 Signal	Pin	MBGA PIN#	SA1110 Signal	Pin	MBGA PIN#	SA1110 Signal
1	B1	RXD_C	53	P1	SDCLK[0]	105	T13	LDD6	157	E16	A[21]	209	D7	VDDX3
2	C2	TXD_C	54	M4	SMROM_EN	106	P13	LDD7	158	F14	A[20]	210	D6	ROMSEL
3	E12	VDDX2	55	P3	VDD	107	E7	VDDX1	159	G10	VSSX	211	A6	TCK_BYP
4	A1	VSSX	56	P2	VSS	108	F11	VSSX	160	L5	VDDX2	212	B6	TESTCLK
5	C1	VDD	57	H12	VDDX2	109	R14	L_LCLK	161	E15	A[19]	213	C6	TMS
6	D3	VSS	58	F6	VSSX	110	T14	L_FCLK	162	D16	A[18]	214	C5	TCK
7	E4	D[0]	59	R1	GP[27]	111	R15	nPOE	163	E14	A[17]	215	A5	TDI
8	D2	D[8]	60	T1	GP[26]	112	T15	nPWE	164	D15	A[16]	216	B5	TDO
9	D1	D[16]	61	R2	GP[25]	113	T16	nPIOR	165	C16	A[15]	217	B4	nTRST
10	E3	D[24]	62	P4	GP[24]	114	R16	nPIOW	166	E13	A[14]	218	A4	BATT_FAULT
11	F4	D[1]	63	T2	GP[23]	115	G6	VSSX	167	D14	VSS	219	H10	VSSX
12	E2	D[9]	64	R3	GP[22]	116	J5	VDDX2	168	C15	VDD	220	E11	VDDX1
13	E1	D[17]	65	D5	VDDX1	117	P14	VSS	169	G11	VSSX	221	C4	VDD_FAULT
14	F3	D[25]	66	F7	VSSX	118	P15	VDD	170	L12	VDDX2	222	A3	PWR_EN
15	F12	VDDX2	67	T3	GP[21]	119	P16	PSKTSL	171	D13	A[13]	223	B3	SFRM_C
16	B2	VSSX	68	R4	GP[20]	120	N13	nIOSIS	172	B16	A[12]	224	A2	SCLK_C
17	F2	D[2]	69	T4	GP[19]	121	N16	nPWAIT	173	C14	A[11]		K10	VDDX1
18	F1	D[10]	70	P5	GP[18]	122	N14	nPREG	174	B14	A[10]		K11	VDDX1
19	G4	D[18]	71	R5	GP[17]	123	N15	nPCE2	175	B15	A[9]		L10	VDDX1
20	G3	D[26]	72	T5	GP[16]	124	M16	nPCE1	176	A16	A[8]		L11	VDDX1
21	G2	D[3]	73	N8	GP[15]	125	M13	nWE	177	H7	VSSX		M6	VDDX1
22	H6	D[11]	74	P6	GP[14]	126	M15	nOE	178	E8	VDDX1		M7	VDDX1
23	G1	D[19]	75	D9	VDDX1	127	G7	VSSX	179	A15	A[7]		M8	VDDX1
24	H4	D[27]	76	F8	VSSX	128	J12	VDDX2	180	A14	A[6]		M9	VDDX1
25	H3	VDD	77	R6	GP[13]	129	M14	nSDRAS	181	B13	A[5]		M10	VDDX1
26	H2	VSS	78	R7	GP[12]	130	L16	nSDCAS	182	C13	A[4]		M11	VDDX1
27	G5	VDDX2	79	T6	GP[11]	131	L15	nRAS[3]	183	A13	A[3]		N7	VDDX1
28	C3	VSSX	80	P7	GP[10]	132	L14	nRAS[2]	184	B12	A[2]		N9	VDDX1
29	H1	D[4]	81	T7	GP[9]	133	L13	nRAS[1]	185	C12	A[1]		N11	VDDX1
30	J6	D[12]	82	P8	GP[8]	134	K16	nRAS[0]	186	D12	A[0]		F5	VDDX2
31	J2	D[20]	83	N8	GP[7]	135	K13	nCAS[3]	187	H8	VSSX		M5	VDDX2
32	J3	D[28]	84	R8	GP[6]	136	K15	nCAS[2]	188	E9	VDDX1		M12	VDDX2
33	J4	D[5]	85	D11	VDDX1	137	G8	VSSX	189	A12	UDC-		N4	VDDX2
34	J1	D[13]	86	F9	VSSX	138	K5	VDDX2	190	C11	UDC+		N5	VDDX2
35	K2	D[21]	87	T8	VDD	139	K14	VSS	191	B11	RXD_1		H11	VSSX
36	K3	D[29]	88	R9	VSS	140	J16	VDD	192	A11	TXD_1		J7	VSSX
37	G12	VDDX2	89	P9	GP[5]	141	J15	nCAS[1]	193	B10	RXD_2		J8	VSSX
38	D4	VSSX	90	T9	GP[4]	142	J14	nCAS[0]	194	D10	TXD_2		J9	VSSX
39	K1	D[6]	91	N10	GP[3]	143	J13	RD_nWR	195	C10	RXD_3		J10	VSSX
40	K4	D[14]	92	R10	GP[2]	144	H13	RDY	196	A10	TXD_3		J11	VSSX
41	L3	D[22]	93	P10	GP[1]	145	H16	nCS[5]	197	H9	VSSX		K6	VSSX
42	L2	D[30]	94	T10	GP[0]	146	H15	nCS[4]	198	E10	VDDX1		K7	VSSX
43	L1	D[7]	95	R11	L_BIAS	147	H14	nCS[3]	199	A9	VSS		K8	VSSX
44	L4	D[15]	96	P11	L_PCLK	148	G18	nCS[2]	200	B9	TEXTAL		K9	VSSX
45	M2	D[23]	97	E6	VDDX1	149	G9	VSSX	201	C9	TEXTAL		L6	VSSX
46	M1	D[31]	98	F10	VSSX	150	K12	VDDX2	202	A8	PEXTAL		L7	VSSX
47	H5	VDDX2	99	N12	LDD0	151	G15	nCS[1]	203	B8	PXTAL		L8	VSSX
48	E6	VSSX	100	T11	LDD1	152	G14	nCS[0]	204	C8	VDDP		L9	VSSX
49	M3	SDCLK[2]	101	R12	LDD2	153	F16	A[25]	205	D8	VSS			
50	N2	SDCKE[1]	102	P12	LDD3	154	G13	A[24]	206	A7	VDO			
51	N3	SDCLK[1]	103	T12	LDD4	155	F13	A[23]	207	B7	nRESET			
52	N1	SDCKE[0]	104	R13	LDD5	156	F15	A[22]	208	C7	nRESET_out			

APPENDIX J - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX K - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Module User's Manual

Tektronix P6434 Mass Termination Probe Instruction Manual

“Advanced RISC Machines Architectural Reference Manual”

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Intel SA-1100 Microprocessor Technical Reference Manual

September 1998

Order Number: 278088-001

Intel SA-1110 Advanced Developer's Manual

March 1999