



NEX-SDIMMFLEX168 SDIMM Bus Adapter Users Manual

Including these Software Support packages:
SDIMMFLX

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1.0 OVERVIEW

1.1 General Information

The NEX-SDIMMFLEX168 adapter has been designed to provide quick and easy connections to interface a 136-channel TLA600/700 acquisition module to a 168-pin SDIMM (3.3V Unbuffered Synchronous DRAM Dual Inline Memory Module) socket. Connections are made through P6434 probes which help minimize the size of the adapter board, thus reducing trace length and keeping signal loading to a minimum.

The NEX-SDIMMFLEX168 support package includes software which offers the following capabilities:

- Selections for the Synchronous acquisition of standard SDRAM cycles (default) or the ability to acquire data on every Rising Edge of CK0, CK1, or CK2
- Selections for:
 - 2- or 3-cycle Read Cycle latency
 - Burst Read lengths of 1, 2, 4, 8, or Full Page
 - Burst Write lengths of 1, 2, 4, 8, or Full Page

By acquiring the information synchronously, data is stored as individual and complete cycles, rather than clocking the data asynchronously and forcing the user to determine bus cycle activity by examining the signal relationships.

Note that this manual uses some terms generically. For instance, references to the TLA700 apply to a TLA704, 711, 715 or TLA711, 720, 721 chassis with one or more 7X4 acquisition cards and TLA600.

Appendix D is a silk-screen print of the NEX-SDIMMFLEX168 Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the different 168-pin SDRAM DIMM configurations and the Tektronix TLA600/700. It is also expected that the user is familiar with Windows O.S.

2.0 SOFTWARE INSTALLATION

The NEX-SDIMM168 software is loaded in the same method as other Windows programs. Place the NEX-SDIMM168 Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install, Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the SDIMM168 support in its proper place on the hard disk.

To load SDIMM168 support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose SDIMM168 and click on **Okay**. Note that the Logic Analyzer card must be 136-channels in width.

3.0 CONFIGURING the NEX-SDIMMFLEX168 BUS SUPPORT

Care should be taken to support the weight of the acquisition probes so that the adapter board and/or target socket are not damaged.

The NEX-SDIMM168 support software is designed to support the current maximum 168-pin SDRAM DIMM configuration: 14 RAS Address lines, 11 CAS Address Lines, 64-bits of Data, 2 Bank Address lines, and 4 Chip Enable lines. If fewer than 14 RAS or 11 CAS Address lines are being used then the extra signals should be removed from the pre-defined groups. Refer to the TLA700 Users Manual for information on adding or deleting signals from a group.

The SDIMM168 support acquires, by default, all standard SDRAM cycles. Refer to Section 5.0 for further information on properly setting the different clocking selections available with this support package.

Because of the number of signals possible in some variations of SDRAM DIMM definition, not all signals can be acquired. Refer to Table 1 for information on which signals are acquired.

4.0 CONNECTING to the NEX-SDIMMFLEX168 ADAPTER

4.1 General

The NEX-SDIMMFLEX168 adapter is larger than a standard SDRAM DIMM module, and is designed to function as an extender card while providing easy connections to acquire SDRAM data by the Logic Analyzer. It is entirely possible, that placing a target card onto the NEX-SDIMMFLEX168 adapter may result in improper operation of the target card or system.

Care should be used when removing a DIMM under test from the NEX-SDIMMFLEX168. The extraction tabs will break if excessive force is used.

The flex circuit portion of the adapter should not be repeatedly bent back and forth. Also, the bend radius should not exceed 90 degrees. While most flex designs bend the flex and then hold the bend in a “permanent” position this design intentionally leaves the bending and fixturing of the bend up to the user. This allows for maximum flexibility but also requires the use of extreme care concerning the mechanical wear on the adapter.

The necessary acquisition data sections are A0-A3, D0-D3, C0-C3, and E0-E3. Table 1 shows the wiring and Channel Grouping for the TLA600/700 NEX-SDIMMFLEX168 connection.

Group Name	Signal Name	SDIMM Pin #	TLA700 Input	Group Name	Signal Name	SDIMM Pin #	TLA700 Input
DataHi (Hex)	DQ63	161	A3:7	DataLo (Hex)	DQ31	77	A2:7
	DQ62	160	A3:6		DQ30	76	A2:6
	DQ61	159	A3:5		DQ29	75	A2:5
	DQ60	158	A3:4		DQ28	74	A2:4
	DQ59	156	A3:3		DQ27	72	A2:3
	DQ58	155	A3:2		DQ26	71	A2:2
	DQ57	154	A3:1		DQ25	70	A2:1
	DQ56	153	A3:0		DQ24	69	A2:0
	DQ55	151	A1:7		DQ23	67	A0:7
	DQ54	150	A1:6		DQ22	66	A0:6
	DQ53	149	A1:5		DQ21	65	A0:5
	DQ52	144	A1:4		DQ20	60	A0:4
	DQ51	142	A1:3		DQ19	58	A0:3
	DQ50	141	A1:2		DQ18	57	A0:2
	DQ49	140	A1:1		DQ17	56	A0:1
	DQ48	139	A1:0		DQ16	55	A0:0
	DQ47	104	D3:7		DQ15	20	D2:7
	DQ46	103	D3:6		DQ14	19	D2:6
	DQ45	101	D3:5		DQ13	17	D2:5
	DQ44	100	D3:4		DQ12	16	D2:4
	DQ43	99	D3:3		DQ11	15	D2:3
	DQ42	98	D3:2		DQ10	14	D2:2
	DQ41	97	D3:1		DQ9	13	D2:1
	DQ40	95	D3:0		DQ8	11	D2:0
	DQ39	94	D1:7		DQ7	10	D0:7
	DQ38	93	D1:6		DQ6	9	D0:6
	DQ37	92	D1:5		DQ5	8	D0:5
	DQ36	91	D1:4		DQ4	7	D0:4
	DQ35	89	D1:3		DQ3	5	D0:3
	DQ34	88	D1:2		DQ2	4	D0:2
	DQ33	87	D1:1		DQ1	3	D0:1
	DQ32	86	D1:0		DQ0	2	D0:0

Table 1- SDIMMFLEX168 TLA600/700 Wiring

Group Name	Signal Name	SDIMM Pin #	TLA700 Input	Group Name	Signal Name	SDIMM Pin #	TLA700 Input	
RAS_Addr (Hex)	RA13	132	E3:5	CAS_Addr (Hex)	CA10	38	E1:2	
	RA12	126	E3:4		CA9	121	E1:1	
	RA11	122	E3:3		CA8	37	E1:0	
	RA10/AP	38	E3:2		CA7	120	E0:7	
	RA9	121	E3:1		CA6	36	E0:6	
	RA8	37	E3:0		CA5	119	E0:5	
	RA7	120	E2:7		CA4	35	E0:4	
	RA6	36	E2:6		CA3	118	E0:3	
	RA5	119	E2:5		CA2	34	E0:2	
	RA4	35	E2:4		CA1	117	E0:1	
	RA3	118	E2:3		CA0	33	E0:0	
	RA2	34	E2:2		Control (Sym)	A10/AP	38	E3:2
	RA1	117	E2:1			BA1	39	E3:7
RA0	33	E2:0	BA0	122		E3:6		
Bytes (Hex)	DQMB7	131	C1:7	CKE1		63	CK0	
	DQMB6	130	C1:6	CKE0		128	C2:3	
	DQMB5	113	C1:5	S3~		129	Q1	
	DQMB4	112	C1:4	S2~		45	Q2	
	DQMB3	47	C1:3	S1~		114	Q3	
	DQMB2	46	C1:2	S0~		30	Q0	
	DQMB1	29	C1:1	RAS~		115	C2:0	
ChekBits (Off)	DQMB0	28	C1:0	CAS~		111	C2:1	
	CB7	137	C3:3	WE~		27	C2:2	
	CB6	136	C3:2	Misc (Off)		CK0	42	CK3
	CB5	106	E1:7		CK1	125	CK1	
	CB4	105	E1:6	Not Grouped	SCL	83	C3:4	
	CB3	53	C3:1		SDA	82	C2:4	
	CB2	52	C3:0		SA2	167	C3:7	
	CB1	22	E1:5		SA1	166	C3:6	
	CB0	21	E1:5		SA0	165	C3:5	
	CB15	135	C0:7		CK3	163	C2:7	
CB14	134	C0:6	CK2		79	CK2		
CB13	109	C0:5						
CB12	108	C0:4						
CB11	51	C0:3						
CB10	50	C0:2						
CB9	25	C0:1						
CB8	24	C0:0						

Table 1 (cont'd.) - SDIMMFLEX168 TLA600/700 Wiring

~ Denotes a low true signal

Symbol	Definition
DESL--IGNORE_COMMAND--DATA?	x xx 11 1111 xxx
NOP--NO_OPERATION_(S0~)	x xx 11 xxx0 111
NOP--NO_OPERATION_(S1~)	x xx 11 xx0x 111
NOP--NO_OPERATION_(S2~)	x xx 11 x0xx 111
NOP--NO_OPERATION_(S3~)	x xx 11 0xxx 111
BST--BURST_STOP_(S0~)	x xx 11 xxx0 110
BST--BURST_STOP_(S1~)	x xx 11 xx0x 110
BST--BURST_STOP_(S2~)	x xx 11 x0xx 110
BST--BURST_STOP_(S3~)	x xx 11 0xxx 110
READ--COL_ADDR_READ_(S0~)	0 xx 11 xxx0 101
READ--COL_ADDR_READ_(S1~)	0 xx 11 xx0x 101
READ--COL_ADDR_READ_(S2~)	0 xx 11 x0xx 101
READ--COL_ADDR_READ_(S3~)	0 xx 11 0xxx 101
READA--READ&AUTOPRECHARGE_(S0~)	1 xx 11 xxx0 101
READA--READ&AUTOPRECHARGE_(S1~)	1 xx 11 xx0x 101
READA--READ&AUTOPRECHARGE_(S2~)	1 xx 11 x0xx 101
READA--READ&AUTOPRECHARGE_(S3~)	1 xx 11 0xxx 101
WRITE--COL_ADDR_WRITE_(S0~)	0 xx 11 xxx0 100
WRITE--COL_ADDR_WRITE_(S1~)	0 xx 11 xx0x 100
WRITE--COL_ADDR_WRITE_(S2~)	0 xx 11 x0xx 100
WRITE--COL_ADDR_WRITE_(S3~)	0 xx 11 0xxx 100
WRITEA--WRITE&AUTOPRECHARGE_(S0~)	1 xx 11 xxx0 100
WRITEA--WRITE&AUTOPRECHARGE_(S1~)	1 xx 11 xx0x 100
WRITEA--WRITE&AUTOPRECHARGE_(S2~)	1 xx 11 x0xx 100
WRITEA--WRITE&AUTOPRECHARGE_(S3~)	1 xx 11 0xxx 100
ACTV--ROW_ADDRESS_STROBE_(S0~)	x xx 11 xxx0 011
ACTV--ROW_ADDRESS_STROBE_(S1~)	x xx 11 xx0x 011
ACTV--ROW_ADDRESS_STROBE_(S2~)	x xx 11 x0xx 011
ACTV--ROW_ADDRESS_STROBE_(S3~)	x xx 11 0xxx 011
PRE--PRECHARGE_SELECT_BANK_(S0~)	0 xx 11 xxx0 010
PRE--PRECHARGE_SELECT_BANK_(S1~)	0 xx 11 xx0x 010
PRE--PRECHARGE_SELECT_BANK_(S2~)	0 xx 11 x0xx 010
PRE--PRECHARGE_SELECT_BANK_(S3~)	0 xx 11 0xxx 010
PALL--PRECHARGE_ALL_BANK_(S0~)	1 xx 11 xxx0 010
PALL--PRECHARGE_ALL_BANK_(S1~)	1 xx 11 xx0x 010
PALL--PRECHARGE_ALL_BANK_(S2~)	1 xx 11 x0xx 010
PALL--PRECHARGE_ALL_BANK_(S3~)	1 xx 11 0xxx 010
REF--REFRESH_(S0~)	x xx 11 xxx0 001
REF--REFRESH_(S1~)	x xx 11 xx0x 001
REF--REFRESH_(S2~)	x xx 11 x0xx 001
REF--REFRESH_(S3~)	x xx 11 0xxx 001
MRS--MODE_REGISTER_SET_(S0~)	x xx 11 xxx0 000
MRS--MODE_REGISTER_SET_(S1~)	x xx 11 xx0x 000
MRS--MODE_REGISTER_SET_(S2~)	x xx 11 x0xx 000
MRS--MODE_REGISTER_SET_(S3~)	x xx 11 0xxx 000

Table 2- SDIMMFLEX168 Control Symbol Table

Signals, left-to-right: RA10/AP, BA1, BA0, CKE1, CKE0, S3~, S2~, S1~, S0~, RAS~, CAS~, WE~

5.0 CLOCK SELECTION

5.1 General Information

There are four clocking options available when using the NEX-SDIMMFLEX168 support package. Each is explained in detail below.

The selections are made by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

5.2 Clocking Options - Explanation

Clocking Mode - Valid Cycles Only is the default mode, and will setup the logic analyzer to acquire all but DESL and NOP cycles. An optional selection is Rising Edge of CK0, CK1 or CK2, which will setup the analyzer to acquire and store data on every CK0, CK1 or CK2 rising edge.

Read Cycle Latency - This sets the number of clock cycles to wait before valid Read data is available. The default setting a latency of 3 clock cycles, but this can be set to 2.

Burst Read Length - By default this is set to a burst length of 1. Can be set to 2, 4, 8, or Full Page.

Burst Write Length - By default this is set to a burst length of 1. Can be set to 2, 4, 8, or Full Page.

6.0 VIEWING DATA

6.1 Viewing State Data on the TLA600/700

After making an initial acquisition, the TLA600/700 will display the data in the Listing (State) format. RAS Address, CAS Address, DataHi, DataLo, and Bytes information is displayed in hexadecimal format; Control data is displayed using symbols; the ChekBits and Miscellaneous groups default to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. One symbol table (Table 2) has been provided to show the type of transaction that occurred on the SDIMM168 . This symbol table quickly shows what kind of memory cycles occurred - a Read, Write, Precharge, etc.

It is important to note that changing the group, channel, or wiring of the Control group can result in incorrect symbol information being displayed.

Sample	RAS Addr	CAS Addr	DataHi	DataLo	Control
< 0	42C	21C	15151F58	15151558	WRITEA--WRITE&AUTOPRECHARGE (S0~)
< 1	42C	21C	15151F58	15151558	DESL--IGNORE COMMAND--DATA?
< 2	61E	21C	15151F58	15151558	PALL--PRECHARGE ALL BANK (S0~)
< 3	61E	028	15151F58	15151558	WRITEA--WRITE&AUTOPRECHARGE (S0~)
< 4	61E	028	15151F58	15151558	DESL--IGNORE COMMAND--DATA?
< 5	42A	028	15151F58	15151558	PALL--PRECHARGE ALL BANK (S0~)
< 6	42A	00B	00001E00	00000008	READA--READ&AUTOPRECHARGE (S0~)
< 7	42A	00B	0D0D1FD0	0D0D0D38	DESL--IGNORE COMMAND--DATA?
< 8	408	00B	0C0D1FD0	0D0D0DD8	PALL--PRECHARGE ALL BANK (S0~)
< 9	408	003	00001E00	00000008	READA--READ&AUTOPRECHARGE (S0~)
< 10	408	003	15151F58	15151558	DESL--IGNORE COMMAND--DATA?
< 11	403	003	15151F58	15151558	PALL--PRECHARGE ALL BANK (S0~)
< 12	403	02B	00001E00	00000008	READA--READ&AUTOPRECHARGE (S0~)
< 13	403	02B	63151E00	1563266C	DESL--IGNORE COMMAND--DATA?
< 14	42B	02B	63141E00	1463C66B	PALL--PRECHARGE ALL BANK (S0~)
< 15	42B	02B	15151F58	15151558	WRITEA--WRITE&AUTOPRECHARGE (S0~)
< 16	42B	02B	15151F58	15151558	DESL--IGNORE COMMAND--DATA?
< 17	6FE	02B	15151F58	15151558	PALL--PRECHARGE ALL BANK (S0~)
< 18	6FE	20B	00001E00	00000008	READA--READ&AUTOPRECHARGE (S0~)
< 19	6FE	20B	0D0D1FD0	0D0D0DD8	DESL--IGNORE COMMAND--DATA?
< 20	608	20B	0F0F1FF0	0F4A4AF8	PALL--PRECHARGE ALL BANK (S0~)
< 21	608	207	00001E00	00000008	READA--READ&AUTOPRECHARGE (S0~)

Figure 1- SDIMMFLEX168 State Display on TLA600/700

6.2 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: SDIMM168 and SDIMM168-MagniVu. The first (SDIMM168) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, SDIMM168-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

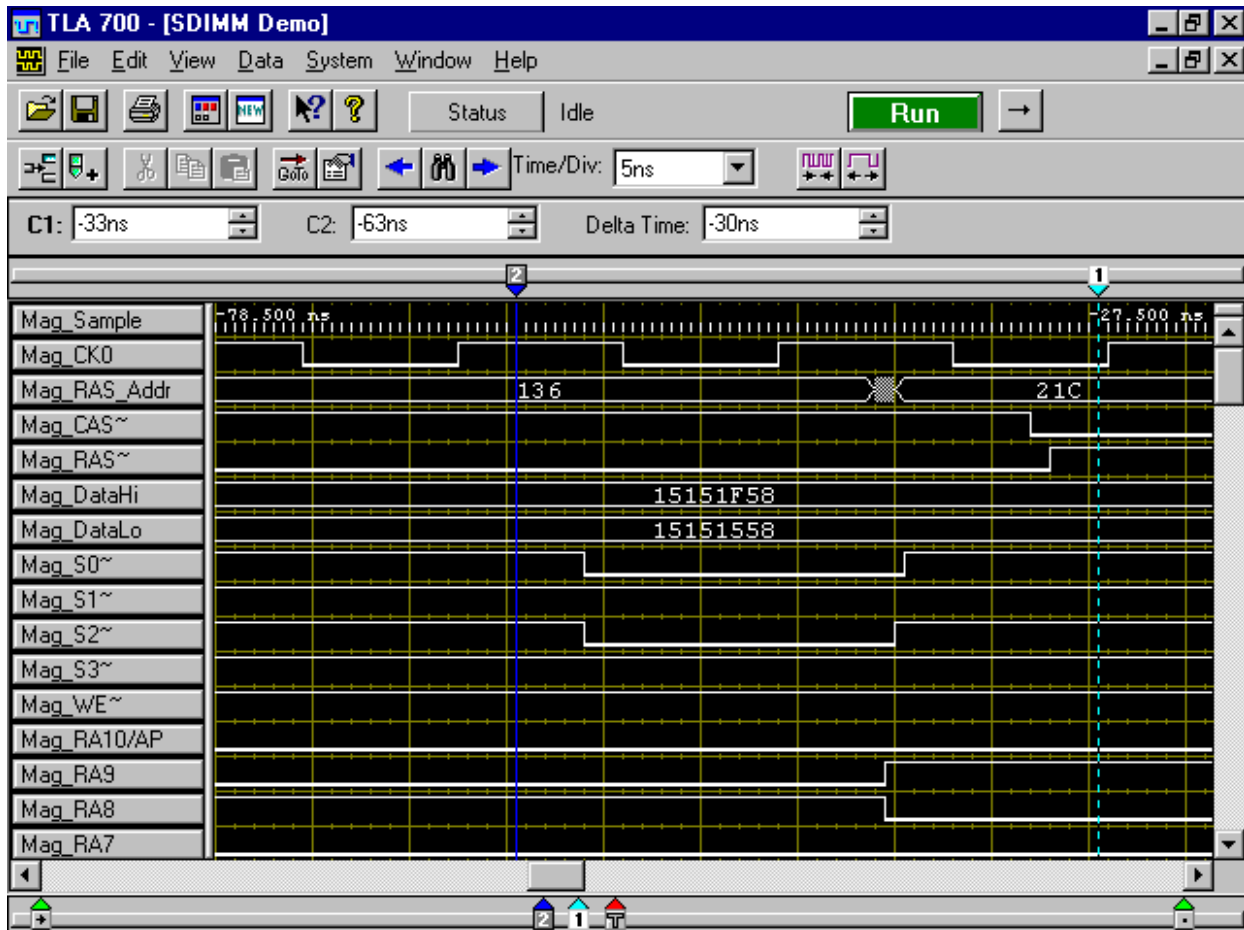


Figure 2- SDIMMFLEX168 MagniVu Display on TLA600/700

APPENDIX A - How SDIMM Data is Clocked

All SDRAM DIMM data is acquired on the rising edge of CK0 with RAS~, CAS~, WE~, CKE0, CKE1, and S0-3~ used as clocking qualifiers. CK1 and CK2 can also be selected.

It is not possible to use merged 102-channel modules for SDIMM support because of the need for the four Qualifier signals (Q0-Q3) available only on the 136-channel card.

APPENDIX B - Considerations

B.1 SDIMM168 Bus Loading

It must be noted that the NEX-SDIMMFLEX168 Bus Adapter does not provide any buffering of the SDRAM memory signals. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-SDIMMFLEX168 adapter, to see the exact timing relationships and signal waveforms from the system.

APPENDIX C - SDRAM SDIMM 168-pin Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	S2~	87	DQ33	129	S3~
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vdd	48	DU	90	Vdd	132	A13
7	DQ4	49	Vdd	91	DQ36	133	Vdd
8	DQ5	50	CB10	92	DQ37	134	CB14
9	DQ6	51	CB11	93	DQ38	135	CB15
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vdd	101	DQ45	143	Vdd
18	Vdd	60	DQ20	102	Vdd	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	CB8	66	DQ22	108	CB12	150	DQ54
25	CB9	67	DQ23	109	CB13	151	DQ55
26	Vdd	68	Vss	110	Vdd	152	Vss
27	WE~	69	DQ24	111	CAS~	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0~	72	DQ27	114	S1~	156	DQ59
31	DU	73	Vdd	115	RAS~	157	Vdd
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	NC	123	A11	165	SA0
40	Vdd	82	SDA	124	Vdd	166	SA1
41	Vdd	83	SCL	125	CK1	167	SA2
42	CK0	84	Vdd	126	A12	168	Vdd

APPENDIX D - NEX-SDIMMFLEX168 Mictor Pinout

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal
3	5	CK0	63	CKE1	36	6	CK1	125	CK1
4	7	A3:7	161	DQ63	35	8	A1:7	151	DQ55
5	9	A3:6	160	DQ62	34	10	A1:6	150	DQ54
6	11	A3:5	159	DQ61	33	12	A1:5	149	DQ53
7	13	A3:4	158	DQ60	32	14	A1:4	144	DQ52
8	15	A3:3	156	DQ59	31	16	A1:3	142	DQ51
9	17	A3:2	155	DQ58	30	18	A1:2	141	DQ50
10	19	A3:1	154	DQ57	29	20	A1:1	140	DQ49
11	21	A3:0	153	DQ56	28	22	A1:0	139	DQ48
12	23	A2:7	77	DQ31	27	24	A0:7	67	DQ23
13	25	A2:6	76	DQ30	26	26	A0:6	66	DQ22
14	27	A2:5	75	DQ29	25	28	A0:5	65	DQ21
15	29	A2:4	74	DQ28	24	30	A0:4	60	DQ20
16	31	A2:3	72	DQ27	23	32	A0:3	58	DQ19
17	33	A2:2	71	DQ26	22	34	A0:2	57	DQ18
18	35	A2:1	70	DQ25	21	36	A0:1	56	DQ17
19	37	A2:0	69	DQ24	20	38	A0:0	55	DQ16

Mictor Group A

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal
3	5	CK3	42	CK0	36	6	Q1	129	S3~
4	7	C3:7	167	SA2	35	8	C1:7	131	DQMB7
5	9	C3:6	166	SA1	34	10	C1:6	130	DQMB6
6	11	C3:5	165	SA0	33	12	C1:5	113	DQMB5
7	13	C3:4	83	SCL	32	14	C1:4	112	DQMB4
8	15	C3:3	137	CB7	31	16	C1:3	47	DQMB3
9	17	C3:2	136	CB6	30	18	C1:2	46	DQMB2
10	19	C3:1	53	CB3	29	20	C1:1	29	DQMB1
11	21	C3:0	52	CB2	28	22	C1:0	28	DQMB0
12	23	C2:7	163	CK3	27	24	C0:7	135	CB15
13	25	C2:6		---	26	26	C0:6	134	CB14
14	27	C2:5		---	25	28	C0:5	109	CB13
15	29	C2:4	82	SDA	24	30	C0:4	108	CB12
16	31	C2:3	128	CKE0	23	32	C0:3	51	CB11
17	33	C2:2	27	WE~	22	34	C0:2	50	CB10
18	35	C2:1	111	CAS~	21	36	C0:1	25	CB9
19	37	C2:0	115	RAS~	20	38	C0:0	24	CB8

Mictor Group C

APPENDIX D - NEX-SDIMM168 Mictor Pinout (cont'd)

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal
3	5	Q0	30	S0~	36	6	CK2	79	CK2
4	7	D3:7	104	DQ47	35	8	D1:7	94	DQ39
5	9	D3:6	103	DQ46	34	10	D1:6	93	DQ38
6	11	D3:5	101	DQ45	33	12	D1:5	92	DQ37
7	13	D3:4	100	DQ44	32	14	D1:4	91	DQ36
8	15	D3:3	99	DQ43	31	16	D1:3	89	DQ35
9	17	D3:2	98	DQ42	30	18	D1:2	88	DQ34
10	19	D3:1	97	DQ41	29	20	D1:1	87	DQ33
11	21	D3:0	95	DQ40	28	22	D1:0	86	DQ32
12	23	D2:7	20	DQ15	27	24	D0:7	10	DQ7
13	25	D2:6	19	DQ14	26	26	D0:6	9	DQ6
14	27	D2:5	17	DQ13	25	28	D0:5	8	DQ5
15	29	D2:4	16	DQ12	24	30	D0:4	7	DQ4
16	31	D2:3	15	DQ11	23	32	D0:3	5	DQ3
17	33	D2:2	14	DQ10	22	34	D0:2	4	DQ2
18	35	D2:1	13	DQ9	21	36	D0:1	3	DQ1
19	37	D2:0	11	DQ8	20	38	D0:0	2	DQ0

Mictor Group D

Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal	Tek Mictor Pin #	AMP Mictor Pin #	TLA Channel	SDIMM Pin #	SDIMM Signal
3	5	Q3	114	S1~	36	6	Q2	45	S2~
4	7	E3:7	39	BA1	35	8	E1:7	106	CB5
5	9	E3:6	122	BA0	34	10	E1:6	105	CB4
6	11	E3:5	132	A13	33	12	E1:5	22	CB1
7	13	E3:4	126	A12	32	14	E1:4	21	CB0
8	15	E3:3	123	A11	31	16	E1:3	---	---
9	17	E3:2	38	A10/AP	30	18	E1:2	---	---
10	19	E3:1	121	A9	29	20	E1:1	---	---
11	21	E3:0	37	A8	28	22	E1:0	---	---
12	23	E2:7	120	A7	27	24	E0:7	---	---
13	25	E2:6	36	A6	26	26	E0:6	---	---
14	27	E2:5	119	A5	25	28	E0:5	---	---
15	29	E2:4	35	A4	24	30	E0:4	---	---
16	31	E2:3	118	A3	23	32	E0:3	---	---
17	33	E2:2	34	A2	22	34	E0:2	---	---
18	35	E2:1	117	A1	21	36	E0:1	---	---
19	37	E2:0	33	A0	20	38	E0:0	---	---

Mictor Group E

APPENDIX E - References

JEDEC Standard No. 21-C “Configurations for Solid State Memories”
Release 7, January 1997

Hitachi HB526C264EN/464EN Series Synchronous Dynamic RAM Module Data Sheet
ADE-203-629 (Z), Preliminary, Rev. 0.0, Aug 20, 1996

Tektronix TLA600/700 System User’s Manual

Tektronix TLA600/700 Logic Analyzer User’s Manual

APPENDIX F - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.