



NEX-SIMM72

Users Manual

Including these Software Support packages:
SIMM72

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1.0 OVERVIEW

1.1 General Information

The NEX-SIMM72 adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA700, a 92A96, or a 92C96 acquisition module to a 72-pin SIMM (Single Inline Memory Module) socket. In addition, the method of connection permits the use of other acquisition cards, pattern generation cards or other measurement devices such as oscilloscopes.

The NEX-SIMM72 adapter includes software which permits the synchronous acquisition of the following DRAM cycles:

- Standard Read and Write
- Fast Page Mode
- EDO (Extended Data Output)
- RAS-only Refresh Cycles
- CAS-before-RAS Refresh Cycles

By acquiring the information synchronously, data is stored as individual and complete cycles, rather than clocking the data asynchronously and forcing the user to determine bus cycle activity by examining the signal relationships.

Note that the status of all active CAS lines may not be acquired properly due to the timing margins present in a design. Proper acquisition of the CAS Address is not affected. This is also true of the RAS lines during a RAS-Only Refresh.

Also note that this manual uses some terms generically. For instance, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA700 apply to a TLA704 or TLA711 chassis with one or more 7L3/4 or 7M3/4 acquisition cards.

Appendix D is a silk-screen print of the NEX-SIMM72 Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the different 72-pin SIMM connector configurations and the Tektronix TLA700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA700, it is expected that the user is familiar with Windows 95.

For information on using a Prism 32GPX/GPD module with this support, or if 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix F for contact information.

2.0 SOFTWARE INSTALLATION

Two 3½" diskettes have been included with the NEX-SIMM72 Bus Adapter. One is for use with the TLA700 series, the other is to be used with a DAS9200 or TLA500.

2.1 TLA700

The NEX-SIMM72 software is loaded in the same method as other Win95 programs. Place the NEX-SIMM72 Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the SIMM72 support in its proper place on the hard disk.

To load SIMM72 support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose SIMM72 and click on **Okay**. Note that the Logic Analyzer card must be at least 102-channels in width.

2.2 DAS9200

The included diskette should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing "SIMM72 Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

3.0 CONFIGURING the NEX-SIMM72 BUS SUPPORT

3.1 Hardware

There are several unused inputs that can be connected to points of interest on the target. Inputs A1:2-6 are acquired on the falling edge of any CAS~ signal and inputs A3:2 and A3:3 are acquired on the falling edge of any RAS~ signal. Feed-throughs are provided next to each one of the unused channels to permit wiring other signals of interest for monitoring.

Care should be taken to support the weight of the acquisition probes so that the adapter board and/or target socket are not damaged.

3.2 Software

The NEX-SIMM72 support software is designed to support the current maximum 72-pin SIMM configuration: 12 RAS/CAS Address lines, 36-bits of Data, and 4 each RAS/CAS enable lines. If fewer Address and/or Data lines exist on the target bus then refer to the instrument-specific instructions below.

3.2.1 TLA700

To load SIMM72 support into the TLA700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose SIMM72 and click on **Okay**. Note that the Logic Analyzer card must be at least 102-channels in width.

The SIMM72 support acquires both Fast Page Mode (FPM) and Extended Data Output (EDO) DRAM cycles. When using a TLA700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired DRAM clocking mode in the Clocking Select field - Include or Exclude Refresh Cycles.

If fewer than 12 RAS/CAS Address lines are being used then the extra signals should be removed from the pre-defined groups. Refer to the TLA700 Users Manual for information on adding or deleting signals from a group.

3.2.2 DAS 9200 / TLA500

Load the desired support from within the 92A96 Config menu. Select "SIMM72 Support", press <RETURN>, and the channel grouping, clocking and symbols will then be loaded. The SIMM72 support acquires both Fast Page Mode (FPM) and Extended Data Output (EDO) DRAM cycles. Move to the Clock menu and choose the desired DRAM clocking mode - Include or Exclude Refresh Cycles.

If fewer than 12 RAS/CAS Address lines are being used then the extra signals should be removed from the pre-defined groups. Refer to the DAS/TLA Users Manual and 92A96/92C96 acquisition card manuals for information on adding or deleting signals from a group.

4.0 CONNECTING to the NEX-SIMM72 ADAPTER

4.1 General

The NEX-SIMM72 adapter is larger than a standard SIMM module, and is designed to function both as signal break-out board and as an extender card.

4.2 TLA700

When using NEX-SIMM72 support with a TLA700 containing a 7L3/4 or 7M3/4 acquisition module, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. Connect the grouped pods (8 podlets to a group) to their appropriate locations by following the silk-screen information printed on the adapter board. Each pod has its proper location denoted (above the connectors) on the silk-screen of the adapter board. When attaching the pods, follow the silk-screen information on the board showing the ground and signal pin locations. When properly connected, the sides of the podlets that have writing on them should face towards the left side of the adapter board.

Connect the four clock leads (CLK0 - CLK3) to their specified locations at J7 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the TLA700 when used with SIMM72 Support.

4.3 92A96 / TLA500

Connect the grouped pods (8 podlets to a group) to their appropriate locations by following the silk-screen information printed on the adapter board. Each pod has its proper location denoted (above the connectors) on the silk-screen of the adapter board. When attaching the pods, follow the silk-screen information on the board showing the ground and signal pin locations. With the 92A96 the colored sides of the pods should face towards the left side of the adapter board.

Connect the four clock leads (CLK0 - CLK3) to their specified locations at J7 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the 92A96 when used with SIMM72 Support.

Group Name	Signal Name	SIMM72 Pin #	TLA700/92A96 input	Group Name	Signal Name	SIMM72 Pin #	TLA700/92A96 input
RASAddr (HEX)	RAS-A11	29	A3:3	HiData (HEX)	DQ35	38	A3:7
	RAS-A10	19	A3:2		DQ34	64	A3:6
	RAS-A9	32	A3:1		DQ33	62	A3:5
	RAS-A8	31	A3:0		DQ32	60	A3:4
	RAS-A7	28	A2:7	Data (HEX)	DQ31	58	D3:7
	RAS-A6	18	A2:6		DQ30	56	D3:6
	RAS-A5	17	A2:5		DQ29	54	D3:5
	RAS-A4	16	A2:4		DQ28	52	D3:4
	RAS-A3	15	A2:3		DQ27	50	D3:3
	RAS-A2	14	A2:2		DQ26	35	D3:2
RAS-A1	13	A2:1	DQ25		27	D3:1	
RAS-A0	12	A2:0	DQ24		25	D3:0	
CASAddr (HEX)	CAS-A11	29	A1:3		DQ23	23	D2:7
	CAS-A10	19	A1:2		DQ22	21	D2:6
	CAS-A9	32	A1:1	DQ21	9	D2:5	
	CAS-A8	31	A1:0	DQ20	7	D2:4	
	CAS-A7	28	A0:7	DQ19	5	D2:3	
	CAS-A6	18	A0:6	DQ18	3	D2:2	
	CAS-A5	17	A0:5	DQ17	37	D2:1	
	CAS-A4	16	A0:4	DQ16	65	D2:0	
	CAS-A3	15	A0:3	DQ15	63	D1:7	
	CAS-A2	14	A0:2	DQ14	61	D1:6	
Control (SYM)	CAS-A1	13	A0:1	DQ13	57	D1:5	
	CAS-A0	12	A0:0	DQ12	55	D1:4	
	RAS3~	33	C3:7	DQ11	53	D1:3	
	RAS2~	34	C3:6	DQ10	51	D1:2	
	RAS1~	45	C3:3	DQ9	49	D1:1	
	RAS0~	44	C3:2	DQ8	36	D1:0	
	CAS3~	42	C3:5	DQ7	26	D0:7	
	CAS2~	41	C3:4	DQ6	24	D0:6	
Misc	CAS1~	43	C3:1	DQ5	22	D0:5	
	CAS0~	40	C3:0	DQ4	20	D0:4	
	WE~	47	C2:0	DQ3	8	D0:3	
	RFSHCLK	*	A1:7	DQ2	6	D0:2	
	RAS_D	*	C2:2	DQ1	4	D0:1	
	CAS_D	*	C2:1	DQ0	2	D0:0	
	PRD4	70	C2:7	Clocks	Clock:0	* RAS_D	
	PRD3	69	C2:6		Clock:1	* CAS_D	
PRD2	68	C2:5	Clock:2		*	RFSHCLK	
PRD1	67	C2:4	Clock:3		*	CAS_STRT	

Table 1- SIMM72 TLA700 / 92A96 Wiring

* Derived signal
~ Denotes a low true signal

Pattern	Symbol	Meaning
0xxx0xxx1	READ	RAS3, CAS3 active; Read
0xxxx0xx1	READ	RAS3, CAS2 active; Read
0xxxxx0x1	READ	RAS3, CAS1 active; Read
0xxxxxx01	READ	RAS3, CAS0 active; Read
0xxx0xxx0	WRITE	RAS3, CAS3 active; Write
0xxxx0xx0	WRITE	RAS3, CAS2 active; Write
0xxxxx0x0	WRITE	RAS3, CAS1 active; Write
0xxxxxx00	WRITE	RAS3, CAS0 active; Write
x0xx0xxx1	READ	RAS2, CAS3 active; Read
x0xxx0xx1	READ	RAS2, CAS2 active; Read
x0xxxx0x1	READ	RAS2, CAS1 active; Read
x0xxxxx01	READ	RAS2, CAS0 active; Read
x0xx0xxx0	WRITE	RAS2, CAS3 active; Write
x0xxx0xx0	WRITE	RAS2, CAS2 active; Write
x0xxxx0x0	WRITE	RAS2, CAS1 active; Write
x0xxxxx00	WRITE	RAS2, CAS0 active; Write
xx0x0xxx1	READ	RAS1, CAS3 active; Read
xx0xx0xx1	READ	RAS1, CAS2 active; Read
xx0xxx0x1	READ	RAS1, CAS1 active; Read
xx0xxxx01	READ	RAS1, CAS0 active; Read
xx0x0xxx0	WRITE	RAS1, CAS3 active; Write
xx0xx0xx0	WRITE	RAS1, CAS2 active; Write
xx0xxx0x0	WRITE	RAS1, CAS1 active; Write
xx0xxxx00	WRITE	RAS1, CAS0 active; Write
xxx00xxx1	READ	RAS0, CAS3 active; Read
xxx0x0xx1	READ	RAS0, CAS2 active; Read
xxx0xx0x1	READ	RAS0, CAS1 active; Read
xxx0xxx01	READ	RAS0, CAS0 active; Read
xxx00xxx0	WRITE	RAS0, CAS3 active; Write
xxx0x0xx0	WRITE	RAS0, CAS2 active; Write
xxx0xx0x0	WRITE	RAS0, CAS1 active; Write
xxx0xxx00	WRITE	RAS0, CAS0 active; Write
0xxx1111x	RAS Refresh	RAS3 Refresh cycle
x0xx1111x	RAS Refresh	RAS2 Refresh cycle
xx0x1111x	RAS Refresh	RAS1 Refresh cycle
xxx01111x	RAS Refresh	RAS0 Refresh cycle
11111111x	RAS Refresh	RAS Refresh cycle
xxxxxxxx1	ANY READ	
xxxxxxxx0	ANY WRITE	

Table 2- SIMM72 Control Symbol Table

Signals, from left to right: RAS3~, RAS2~, RAS1~, RAS0~,CAS3~, CAS2~, CAS1~, CAS0~,WE~

5.0 VIEWING DATA

5.1 Viewing State Data on the TLA700

After making an initial acquisition, the TLA700 will display the data in the Listing (State) format. RAS Address, CAS Address, HiData, and Data information is displayed in hexadecimal format; Control data is displayed using symbols; the Miscellaneous group defaults to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. One symbol table (Table 2) has been provided to show the type of transaction that occurred on the SIMM72. This symbol table quickly shows what kind of memory cycles occurred - a Read, Write, or Refresh.

It is important to note that changing the group, channel, or wiring of the Control group can result in incorrect symbol information being displayed.

The screenshot shows the TLA 700 software interface with a menu bar (File, Edit, View, Data, System, Window, Help) and a toolbar. The main display area shows a table of memory cycles for SIMM72. The table has columns for Sample, RASAddr, CASAddr, HiData, Data, Control, and Timestamp. The data is as follows:

Sample	RASAddr	CASAddr	HiData	Data	Control	Timestamp
46	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.200,500 us
47	055	255	0	00000000	WRITE	62.075,000 us
48	055	255	0	00000000	READ	1.498,500 us
49	055	255	F	FFFFFFFF	WRITE	3.701,500 us
50	055	255	F	FFFFFFFF	READ	1.499,000 us
51	0AA	2AA	0	00000000	WRITE	12.503,000 us
52	0AA	2AA	0	00000000	READ	1.498,500 us
53	0AA	2AA	F	FFFFFFFF	WRITE	3.702,000 us
54	0AA	2AA	F	FFFFFFFF	READ	1.498,000 us
55	0AA	2AA	7	83C1E0F0	WRITE	13.103,000 us
56	0AA	2AA	7	83C1E0F0	READ	1.498,500 us
57	002	203	F	FFFFFFFF	RAS ONLY REFRESH	476.084,500 us
58	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.201,000 us
59	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.200,000 us
60	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.200,500 us
61	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.200,500 us
62	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.200,500 us
63	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.200,000 us
64	002	203	F	FFFFFFFF	RAS ONLY REFRESH	4.200,500 us

Figure 1- SIMM72 State Display on TLA700

5.2 Viewing Timing Data on the TLA700

By default, the TLA700 will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: SIMM72 and SIMM72-MagniVu. The first (SIMM72) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Timing format. The second selection, SIMM72-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA700 System User's Manual for additional information on formatting the Waveform display.

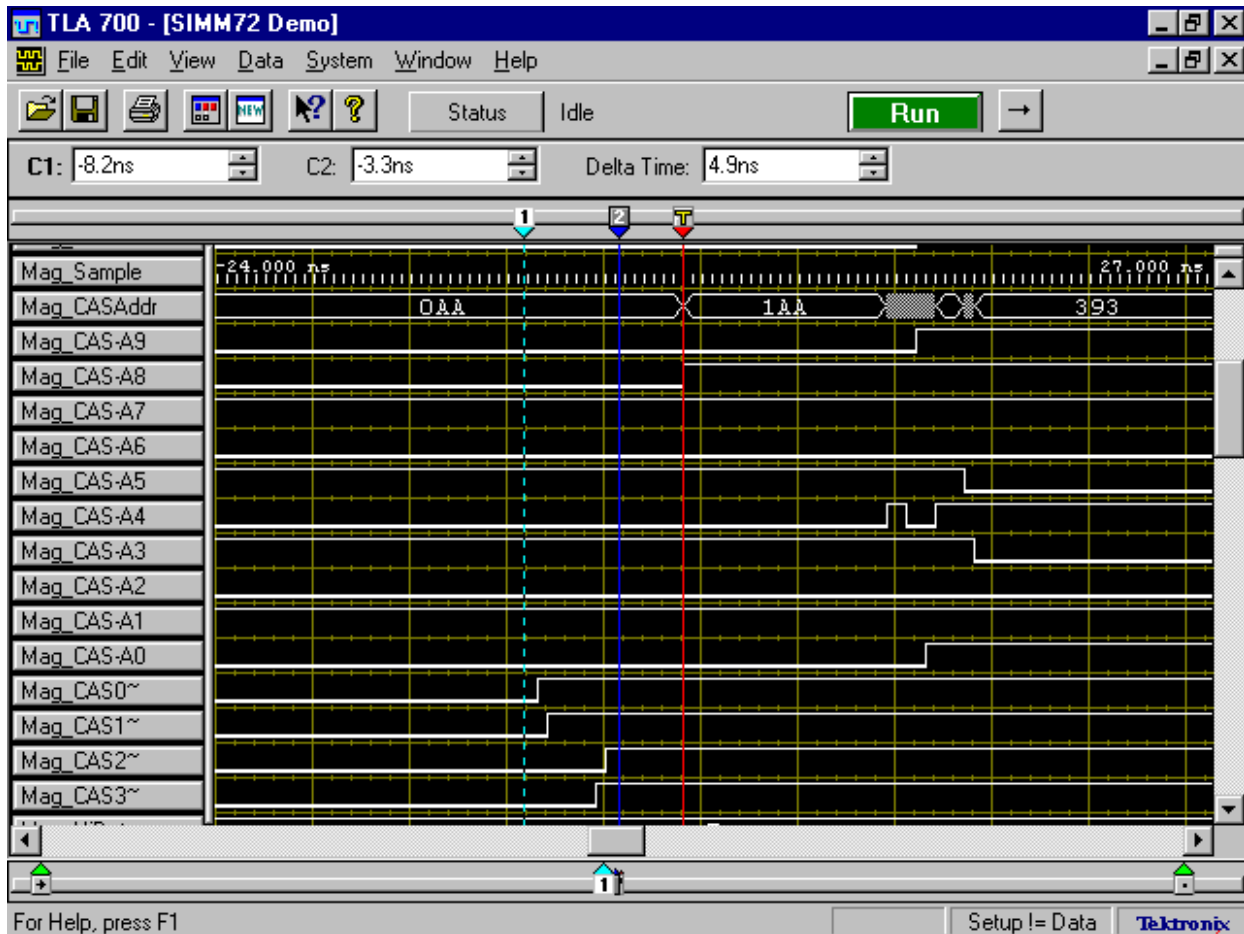


Figure 2- SIMM72 MagniVu Display on TLA700

5.3 Viewing State Data with the DAS / TLA500

After an acquisition is made the DAS 9200 / TLA510 Logic Analyzer will display the data in State Display mode (as a default only). RAS Address, CAS Address, HiData, and Data information is displayed in hexadecimal format; Control data is displayed using symbols; the Miscellaneous group defaults to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. One symbol table (Table 2) has been provided to show the type of transaction that occurred on the SIMM72 bus, and its DAS filename is "SIMM72_Ctrl". This symbol table quickly shows what kind of memory cycles occurred - a Read, Write, or Refresh.

It is important to note that changing the group, channel, or wiring of the Control group can result in incorrect symbol information being displayed.

5.4 Viewing Timing Data with the DAS / TLA

It may be useful to display acquired information using the Timing Diagram display of the DAS / TLA. (Note that, unlike some other logic analyzers, with the 92A96 there is no need to re-acquire SIMM data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the 92A96 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

APPENDIX A - How SIMM Data is Clocked

All SIMM data is usually acquired on the falling edge of any RAS signal and both edges of the CAS signals. The only exception to this is for RAS-Only Refresh cycles when the rising edge of a RAS signal terminates the cycle.

To properly acquire SIMM bus activity, the following signals must be provided: all RAS and CAS lines, and WE~. If any RAS and/or CAS lines are unused they are assumed to be unconnected or tied to their inactive state (to Vcc). However, 10K pullups are provided on these lines to help ensure that this is done.

As mentioned before, it is important to note that the status of all active CAS lines may not be acquired properly due to the timing margins present in a design. Proper acquisition of the CAS Address is not affected. This is also true of the RAS lines during a RAS-Only Refresh.

APPENDIX B - Considerations

B.1 SIMM72 Bus Loading

It must be noted that the NEX-SIMM72 Bus Adapter does not provide any buffering of the SIMM memory signals. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-SIMM72 adapter, to see the exact timing relationships and signal waveforms from the system. It is also much easier to connect pattern generators to the bus since buffer direction is not a concern. It is believed that the signal loading of the TLA700 or 92A96 acquisition cards is low enough so that signal degradation will not occur.

B.2 Pattern Generation

Because there is no buffer circuitry on the NEX-SIMM72 Adapter, it is well suited for use with the 92S16 and 92S32 Pattern Generator modules available for the DAS 9200 and TLA500. By connecting pattern generator probes to the A96 signal connectors on the Adapter, desired bus activity can be simulated. This can be particularly effective when trying to debug interrupt or DMA conflicts.

It should be noted that, because of the pin spacing of the A96 connectors, it is not recommended that the Tektronix P6464 or P6465 pattern generator probes be used without providing adequate cooling for their podlets. These probes use active podlets that can get very warm in use. A better choice would be the P6463 pods which are passive and do not have such cooling requirements.

CAUTION!

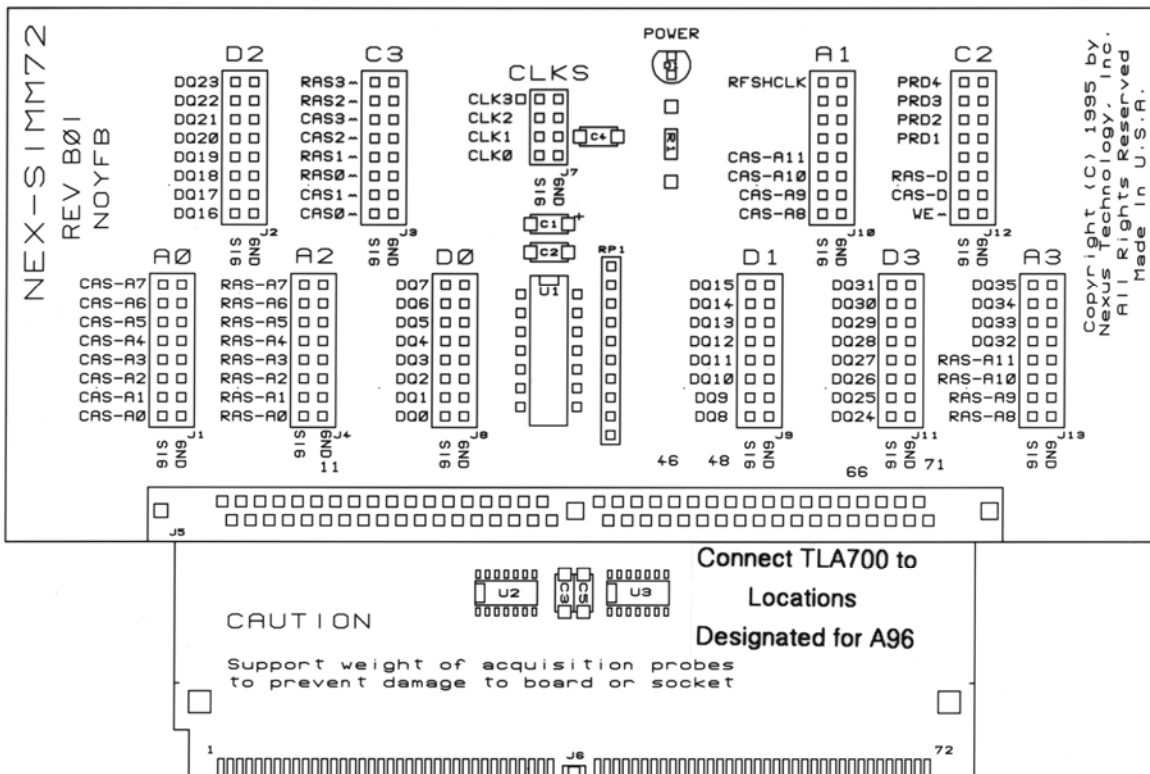
Because of the circuitry on the NEX-SIMM72 adapter, it is suggested that the Pattern Generators not be connected to the RAS_D, CAS_D, and RFSHCLK signals. Damage to the on-board circuitry could result if this caution is not followed.

APPENDIX C - SIMM72 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	CAS0~	58	DQ31
5	DQ19	23	DQ23	41	CAS2~	59	Vcc
6	DQ2	24	DQ6	42	CAS3~	60	DQ32
7	DQ20	25	DQ24	43	CAS1~	61	DQ14
8	DQ3	26	DQ7	44	RAS0~	62	DQ33
9	DQ21	27	DQ25	45	RAS1~	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	A11	47	WE~	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ27	68	PRD2
15	A3	33	RAS1~	51	DQ10	69	PRD3
16	A4	34	RAS0~	52	DQ28	70	PRD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

Table 3- SIMM 72-pin Pinout

APPENDIX D - NEX-SIMM72 Silk Screen



APPENDIX E - References

Hitachi DRAM Modules Data Book (1994; #M11T316)

JEDEC Standard No. 21-C “Configurations for Solid State Memories”
Release 7, January 1997

Micron Technology 1995 DRAM Data Book

Tektronix TLA700 System User’s Manual

Tektronix TLA700 Logic Analyzer User’s Manual

Tektronix DAS 9200 System User's Manual

Tektronix DAS 9200 92A96 User's Manual

APPENDIX F - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

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General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.