



**NEX-SODIMM**  
**Synchronous DRAM SO-DIMM Support Users Manual**  
**Including these Software Support packages:**  
**SODIMM**

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## **1.0 OVERVIEW**

### **1.1 General Information**

The NEX-SODIMM adapter has been designed to provide quick and easy connections to interface a 136-channel TLA600 or TLA700 acquisition module to a 144-pin SODIMM (3.3V Unbuffered or Registered Synchronous DRAM Dual Inline Memory Module) socket. Logic Analyzer connections are made to Mictor connectors on the adapter using P6434 probes or P6860 probes with Tektronix Mictor-on-PCB to Compression adapters. Using the Mictor connectors helps minimize the size of the adapter board, thus reducing trace length and keeping signal loading to a minimum.

The NEX-SODIMM support package includes SODIMM software which offers the following capabilities:

- Selections for the Selective acquisition of standard SDRAM cycles (default) or the ability to acquire data on every Rising Edge of SDRAM CK0 or CK1
- Post-processing display selections for:
  - Burst Read lengths of 1, 2, 4, 8, or Full Page
  - Burst Write lengths of Single (non-bursted) or Same Length as Reads
  - Registered DIMM support

By acquiring the information synchronously, data is stored as individual and complete cycles, rather than clocking the data asynchronously and forcing the user to determine bus cycle activity by examining the signal relationships.

Note that this manual uses some terms generically. For instance, references to the TLA apply to a 136-channel TLA6X4 or TLA7XX chassis with one or more 136-channel acquisition cards. To support data rates in excess of 100MHz the acquisition cards must be configured for 200MHz or greater state acquisition speed.

This manual assumes that the user is familiar with the different 144-pin SDRAM SODIMM configurations and the Tektronix TLA600/700. It is also expected that the user is familiar with the Windows OS on the TLA (Win95, Win98, or Win2000).

## **2.0 SOFTWARE INSTALLATION**

The SODIMM software is loaded in the same manner as other Windows programs. Place the SODIMM Install disk in the floppy drive of the TLA700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the SODIMM support in its proper place on the hard disk.

To load SODIMM support into the TLA, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose SODIMM and click on **Okay**. Note that the Logic Analyzer card must be 136-channels in width.

## **3.0 CONFIGURING the NEX-SODIMM BUS SUPPORT**

Care should be taken to support the weight of the acquisition probes so that the adapter board and/or target socket are not damaged.

The NEX-SODIMM support software is designed to support the current maximum 144-pin SDRAM SODIMM configuration: 14 RAS Address bits, 11 CAS Address bits, 64-bits of Data, 2 Bank Address signals and 4 Chip Enables. If fewer than 14 RAS bits or 11 CAS bits are used by the target then the extra bits should be removed from the RASAddr and CASAddr groups. Refer to the TLA Users Manual for information on adding and deleting signals from a group.

The SODIMM support acquires, by default, all standard SDRAM cycles. Refer to Section 5.0 for further information on properly setting the different clocking selections available with this support package.

## **4.0 CONNECTING to the NEX-SODIMM ADAPTER**

### **4.1 General**

The NEX-SODIMM adapter is designed to function as an extender card while providing easy connections to acquire SDRAM data by the Logic Analyzer. It is entirely possible, that placing a target card onto the NEX-SODIMM adapter may result in improper operation of the target card or system.

Care should be used when inserting and removing a SODIMM under test from the NEX-SODIMM. The flex circuit portion of the adapter should not be bent back and forth or bent beyond 90 degrees.

Table 1 shows the wiring and Channel Grouping for the TLA NEX-SODIMM connection.

Group Name	Signal Name	SODIMM Pin #	TLA700 Input	Group Name	Signal Name	SODIMM Pin #	TLA700 Input
DataHi (Hex)	DQ63	138	D3:3	DataLo (Hex)	DQ31	137	D0:3
	DQ62	136	D2:6		DQ30	135	D1:2
	DQ61	134	D3:4		DQ29	133	D0:4
	DQ60	132	D2:7		DQ28	131	D1:3
	DQ59	128	D3:5		DQ27	127	D0:5
	DQ58	126	D3:0		DQ26	125	D1:4
	DQ57	124	D3:6		DQ25	123	D0:6
	DQ56	122	D3:1		DQ24	121	D1:5
	DQ55	100	C0:4		DQ23	99	C2:7
	DQ54	98	C0:5		DQ22	97	C2:6
	DQ53	96	C0:6		DQ21	95	C3:1
	DQ52	94	C0:7		DQ20	93	C3:0
	DQ51	90	C1:0		DQ19	89	C3:3
	DQ50	88	C1:1		DQ18	87	C3:2
	DQ49	86	C1:2		DQ17	85	C3:5
	DQ48	84	C1:3		DQ16	83	C3:4
	DQ47	54	A3:4		DQ15	53	A1:3
	DQ46	52	A3:3		DQ14	51	A1:4
	DQ45	50	A3:2		DQ13	49	A1:1
	DQ44	48	A3:1		DQ12	47	A1:2
	DQ43	44	A3:0		DQ11	43	A0:7
	DQ42	42	A2:7		DQ10	41	A1:0
	DQ41	40	A2:6		DQ9	39	A0:5
	DQ40	38	A2:5		DQ8	37	A0:6
	DQ39	20	E1:6		DQ7	19	E2:7
	DQ38	18	E0:6		DQ6	17	E3:5
	DQ37	16	E1:5		DQ5	15	E2:6
	DQ36	14	E0:5		DQ4	13	E3:4
	DQ35	10	E1:4		DQ3	9	E2:5
	DQ34	8	E0:4		DQ2	7	E3:3
	DQ33	6	E1:3		DQ1	5	E2:4
	DQ32	4	E1:2		DQ0	3	E3:2

**Table 1- SODIMM TLA Grouping and Wiring**

Group Name	Signal Name	SODIMM Pin #	TLA700 Input	Group Name	Signal Name	SODIMM Pin #	TLA700 Input		
DRAMAddr (Hex)	BA1	110	C0:1	Control (Sym)	A10/AP	111	D1:0		
	BA0	106	C0:2		BA1	110	C0:1		
	A13	72	C1:7		BA0	106	C0:2		
	A12	70	A3:7		CKE1	68	C2:1		
	A11	112	C0:0		CKE0	62	Q3		
	A10/AP	111	D1:0		S1~	71	C2:0		
	A9	109	D1:7		S0~	69	C2:2		
	A8	105	C2:5		RAS~	65	Q1		
	A7	104	C0:3		CAS~	66	Q2		
	A6	103	C2:4		WE~	67	C2:3		
	A5	34	E1:1		Misc (Off)	CK0	61	CK1	
	A4	32	A2:4			CK1	74	CK3	
	Bytes (Hex)	DQMB7 DQMB6 DQMB5 DQMB4 DQMB3 DQMB2 DQMB1 DQMB0	118		D3:7	Not Grouped	RSVD_60	60	A3:6
			116		D3:2		RSVD_58	58	A3:5
26			E1:7	RSVD_57	57		A1:6		
24			E0:7	RSVD_59	59		A1:5		
117			D0:7	RSVD_79	79		C3:7		
115			D1:6	RSVD_77	77		C3:6		
25			E3:0	RSVD_73	73		C1:6		
23			E3:6	RSVD_78	78		C1:5		
				RSVD_80	80		C1:4		
				SDA	141		D1:1		
				SCL	142		CK2		

Table 1 (cont'd.) – SODIMM TLA Grouping and Wiring

~ Denotes a low true signal

## **5.0 CLOCK SELECTION**

### **5.1 General Information**

There are four clocking options available when using the SODIMM support package. Each is explained in detail below.

The selections are made by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

### **5.2 Clocking Options - Explanation**

**Clock Selection** – Permits selection of SDRAM CK0 or CK1 for use as the acquisition clock.

**Clocking Mode** – Allows the user to choose the kind of data acquisition that will be made:

**Selective Clocking** (default) – This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS~ or CAS~ is asserted low along with S0~ or S1~. After every assertion of CAS~ (with either S0~ or S1~) an additional 12 samples (Reads) or up to 9 samples (Writes) are taken on every SODIMM CLK rising edge. If CAS~ and a Chip Select are asserted during these storage cycles the count is reset.

**Rising Edge of Clock** – As the name implies this will cause the acquisition card to store data on every Rising edge of the selected SDRAM clock.

**Burst Read Length** - By default this is set to a burst length of 1/2/4/8. Can be set to Full Page.

**Burst Write Length** - By default this is set to Single (non-Bursted). Can be set to Same Length as Reads.

## 6.0 VIEWING DATA

### 6.1 Viewing State Data on the TLA - General

After making an initial acquisition, the TLA will display the data in the Listing (State) format. A Symbol Table has been included in the support package for the Command data group (see Table 3). The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. The symbol file has been created to permit quickly showing the type of transaction that occurred on the SODIMM Bus - a Read, Write, Precharge, etc. This symbol information can also be used to trigger on a SODIMM cycle of interest.

It is important to note that changing the group, channel, or wiring of the Command group can result in incorrect symbol information being displayed.

Symbol	Definition
DESL--IGNORE_COMMAND--DATA?	x xx 11 11 xxx
NOP--NO_OPERATION_(S0~)	x xx 11 x0 111
NOP--NO_OPERATION_(S1~)	x xx 11 0x 111
BST--BURST_STOP_(S0~)	x xx 11 x0 110
BST--BURST_STOP_(S1~)	x xx 11 0x 110
READ--COL_ADDR_READ_(S0~)	0 xx 11 x0 101
READ--COL_ADDR_READ_(S1~)	0 xx 11 0x 101
READA—	1 xx 11 x0 101
READ&AUTOPRECHARGE_(S0~)	
READA—	1 xx 11 0x 101
READ&AUTOPRECHARGE_(S1~)	
WRITE--COL_ADDR_WRITE_(S0~)	0 xx 11 x0 100
WRITE--COL_ADDR_WRITE_(S1~)	0 xx 11 0x 100
WRITEA--	1 xx 11 x0 100
WRITE&AUTOPRECHARGE_(S0~)	
WRITEA--	1 xx 11 0x 100
WRITE&AUTOPRECHARGE_(S1~)	
ACTV--ROW_ADDRESS_STROBE_(S0~)	x xx 11 x0 011
ACTV--ROW_ADDRESS_STROBE_(S1~)	x xx 11 0x 011
PRE--	0 xx 11 x0 010
PRECHARGE_SELECT_BANK_(S0~)	
PRE--	0 xx 11 0x 010
PRECHARGE_SELECT_BANK_(S1~)	
PALL—PRECHARGE_ALL_BANK_(S0~)	1 xx 11 x0 010
PALL—PRECHARGE_ALL_BANK_(S1~)	1 xx 11 0x 010
REF--REFRESH_(S0~)	x xx 11 x0 001
REF--REFRESH_(S1~)	x xx 11 0x 001
MRS--MODE_REGISTER_SET_(S0~)	x xx 11 x0 000
MRS--MODE_REGISTER_SET_(S1~)	x xx 11 0x 000

Table 2- SODIMM Control Symbol Table

Signals, left-to-right: RA10/AP, BA1, BA0, CKE1, CKE0, S1~, S0~, RAS~, CAS~, WE~

## 6.2 Viewing SODIMM Data

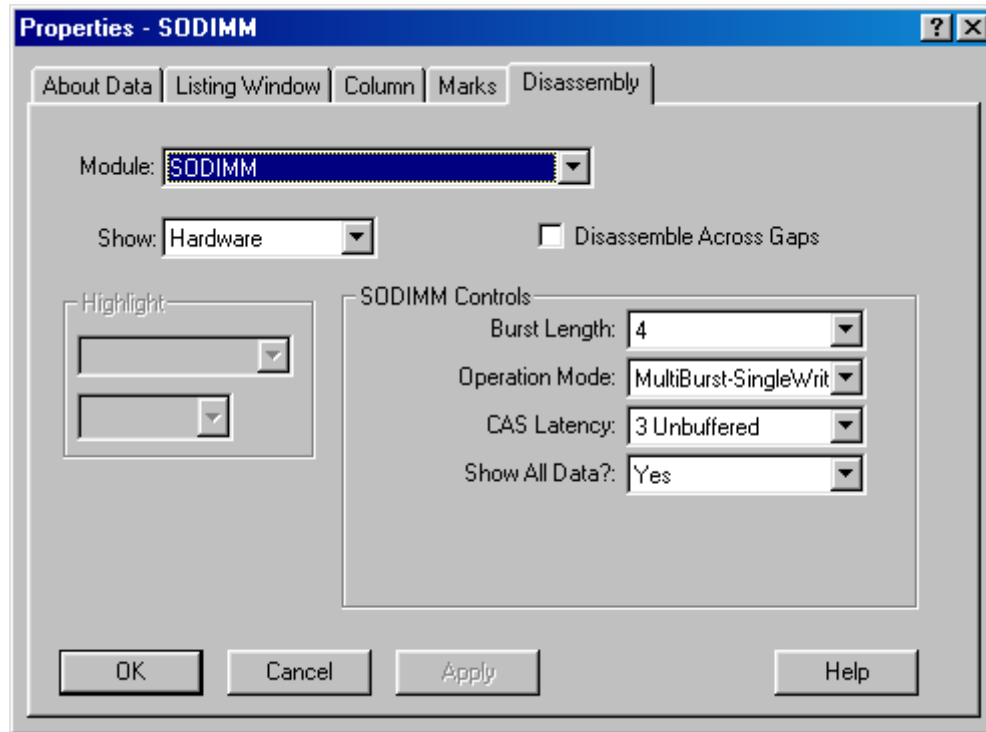
The SODIMM support package displays the Address, DataHi, DataLo, and Bytes group data in hexadecimal format; the Command and Misc groups default to OFF (not automatically displayed).

The Command group is suppressed because its function is replaced with a column labeled “SODIMM Mnemonics”. The SODIMM support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. Figure 1 shows the default display where all SODIMM data is displayed.

Sample	SODIMM DRAMAddr	SODIMM DataHi	SODIMM DataLo	SODIMM Mnemonics	SODIMM Bytes	Timestamp
239	00F0	00000000	00000000	REF - REFRESH (S0~)	FF	9.500 ns
240	00F0	00000000	00000000	REF - REFRESH (S1~)	FF	15.588,500 us
241	00F0	00000000	00000000	REF - REFRESH (S0~)	FF	10.000 ns
242	00F0	00000000	00000000	ACTV - ROW ADDRESS STROBE (S0~)	FF	410.000 ns
243	00F0	00000000	00000000	READ - COL ADDR READ (S0~)	FF	30.000 ns
	00F0	00000000	00000000	[READ LATENCY]	FF	
244	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	00	10.000 ns
	00F0	00000000	00000000	[READ LATENCY]	00	
245	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	00	10.000 ns
	00F0	00000000	00000000	[READ LATENCY]	00	
246	00F0	00000000	55AA55AA	DESL - IGNORE COMMAND--DATA?	00	10.000 ns
	00F0	00000000	55AA55AA	[ READ DATA ]	00	
247	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	00	10.000 ns
	00F0	00000000	00000000	[ READ DATA ]	00	
248	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
	00F0	00000000	00000000	[ READ DATA ]	FF	
249	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
	00F0	00000000	00000000	[ READ DATA ]	FF	
250	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
251	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
252	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
253	00F1	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
254	00F1	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
255	00F1	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
256	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
257	DB06	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
258	DB06	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
259	DB06	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
260	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
261	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
262	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
263	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
264	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
265	00F1	46047468	01234567	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
266	00F1	46047468	01234567	WRITE - COL ADDR WRITE (S0~)	FO	10.000 ns
	00F1	46047468	01234567	[ WRITE DATA ]	FO	
267	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
268	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
269	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
270	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
271	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
272	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns
273	00F0	00000000	00000000	DESL - IGNORE COMMAND--DATA?	FF	10.000 ns

Figure 1- SODIMM State Display - Show All Data? = Yes

To change the display it is necessary to bring up the window’s Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in Figure 2.



**Figure 2- SODIMM Disassembly Properties**

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

**Burst Length** – permits setting the burst length for Read and Write data. Valid choices are 1 (the default), 2, 4, 8, and Full Page. This value must be set properly for all valid Read and Write data to be displayed.

**Operation Mode** – Sets the Write Data mode to Normal (default) which expects the Write Bursts to be the same length as the Read Bursts. Can also be set to MultiBurst-SingleWrite which then will limit the Write Burst length to 1.

**CAS Latency** – sets the delay, in clock cycles, from the Read command until the first Piece of valid Read data is available. Select options exist for Unbuffered or Registered (which adds a clock cycle delay to all data cycle tagging). This value must be set properly for all valid Data to be displayed. Valid choices are 2 Unbuffered (default), 2 Registered, 3 Unbuffered, and 3 Registered.

**Show All Data?** – permits choosing between displaying all SODIMM data (Yes, the default), including Invalid Read / Write and Command data, and showing only valid Data and Command data (No).

When setting **Show All Data?** to No, the display in Figure 1 then becomes the display in Figure

3. This allows the user to see at a glance the valid information on the bus.

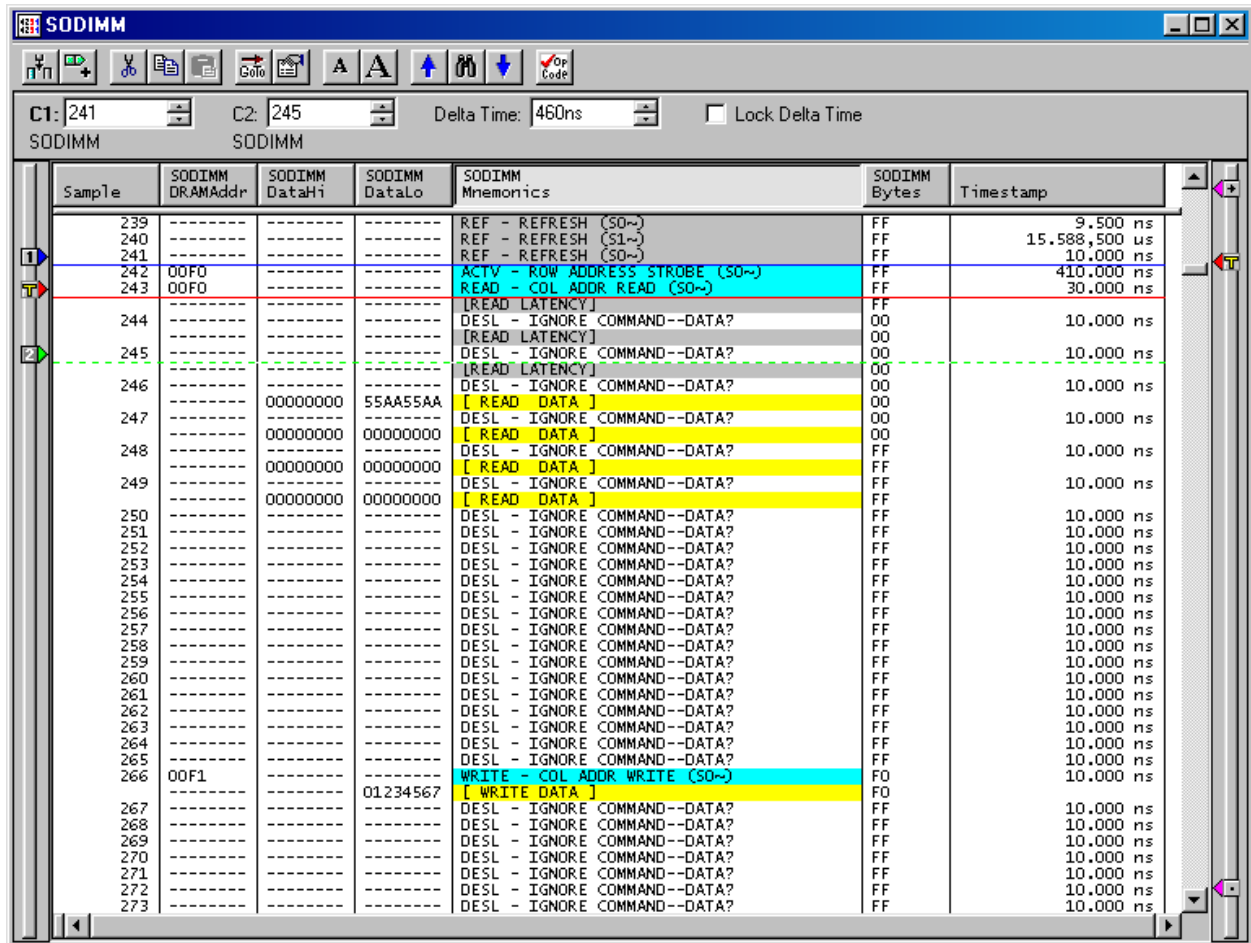


Figure 3- SODIMM State Display - Show All Data? = No

In addition to the Disassembly Properties selections discussed earlier, changing the settings in the **Show** field result in display changes as well:

**Hardware** – displays all acquired cycles

**Software** – suppresses all idle or wait cycles

**Control Flow** – shows Address Command and valid Read / Write data cycles

**Subroutine** – shows valid Read / Write data cycles only

Changing the Show field setting in the display of Figure 3 from Hardware to Control Flow results in the display of Figure 4 where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

Sample	SODIMM DRAMAddr	SODIMM DataHi	SODIMM DataLo	SODIMM Mnemonics	SODIMM Bytes	Timestamp
60	003A	-----	-----	MRS - MODE REGISTER SET (S0~)	FF	0 ps
				Operating Mode:Multiple Burst/Single Wr>	FF	
				Burst Type:Interleaved	FF	
				Burst:4	FF	
				Latency:3	FF	
229	00F0	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	FF	1.541,012,000 ns
230	00F0	-----	-----	WRITE - COL ADDR WRITE (S0~)	F0	30,000 ns
			55AA55AA	[ WRITE DATA ]	F0	
242	00F0	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	FF	64.692,500 us
243	00F0	-----	-----	READ - COL ADDR READ (S0~)	FF	30,000 ns
246	-----	00000000	55AA55AA	[ READ DATA ]	00	30,000 ns
247	-----	00000000	00000000	[ READ DATA ]	00	10,000 ns
248	-----	00000000	00000000	[ READ DATA ]	FF	10,000 ns
249	-----	00000000	00000000	[ READ DATA ]	FF	10,000 ns
266	00F1	-----	-----	WRITE - COL ADDR WRITE (S0~)	F0	170,000 ns
			01234567	[ WRITE DATA ]	F0	
1761	00F0	-----	-----	ACTV - ROW ADDRESS STROBE (S0~)	FF	21.547,500 us
1762	00F0	-----	-----	READ - COL ADDR READ (S0~)	FF	30,000 ns
1765	-----	00000000	55AA55AA	[ READ DATA ]	00	30,000 ns
1766	-----	00000000	01234567	[ READ DATA ]	00	10,000 ns
1767	-----	00000000	00000000	[ READ DATA ]	FF	10,000 ns
1768	-----	00000000	00000000	[ READ DATA ]	FF	10,000 ns

Figure 4- SODIMM State Display - Show Control Flow

### 6.3 SODIMM Mnemonics Description

Table 3 gives a brief description of each of the text lines displayed in the post-processing software display.

<b>Mnemonic</b>	<b>Description</b>
ACTV - ROW ADDRESS STROBE (S0~)	Active command – activate a row in a bank for subsequent access (chip select 0)
ACTV - ROW ADDRESS STROBE (S1~)	Active command – activate a row in a bank for subsequent access (chip select 1)
BST - BURST STOP (S0~)	Burst Terminate command – truncate current Read burst (chip select 0)
BST - BURST STOP (S1~)	Burst Terminate command – truncate current Read burst (chip select 1)
DESL - IGNORE COMMAND	Deselect function – no new command
MRS - MODE REGISTER SET (S0~)	Mode Register Set command – mode register load (chip select 0)
MRS - MODE REGISTER SET (S1~)	Mode Register Set command – mode register load (chip select 1)
NOP - NO OPERATION (S0~)	No Operation command (chip select 0)
NOP - NO OPERATION (S1~)	No Operation command (chip select 1)
PRE - PRECHARGE SELECT BANK (S0~)	Precharge command (chip select 0)
PRE - PRECHARGE SELECT BANK (S1~)	Precharge command (chip select 1)
READ - COL ADDR READ (S0~)	Read command – initiates a burst read access to active row (chip select 0)
READ - COL ADDR READ (S1~)	Read command – initiates a burst read access to active row (chip select 1)
READ DATA	Valid Read data on the bus
REF - REFRESH (S0~)	Self Refresh command (chip select 0)
REF - REFRESH (S1~)	Self Refresh command (chip select 1)
WRITE - COL ADDR WRITE (S0~)	Write command – initiates a burst write access to active row (chip select 0)
WRITE - COL ADDR WRITE (S1~)	Write command – initiates a burst write access to active row (chip select 1)
WRITE DATA	Valid Write data on the bus
READ LATENCY	Read Latency cycle
WRITE LATENCY	Write Latency cycle (Registered DIMMs)

**Table 3- SODIMM Mnemonics Definition**

## 6.4 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: SODIMM and SODIMM-MagniVu. The first (SODIMM) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, SODIMM-MagniVu, will show all of the channels in 2/8GHz MagniVu mode (depending upon the acquisition card used), so that edge relationships can be examined around the MagniVu trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

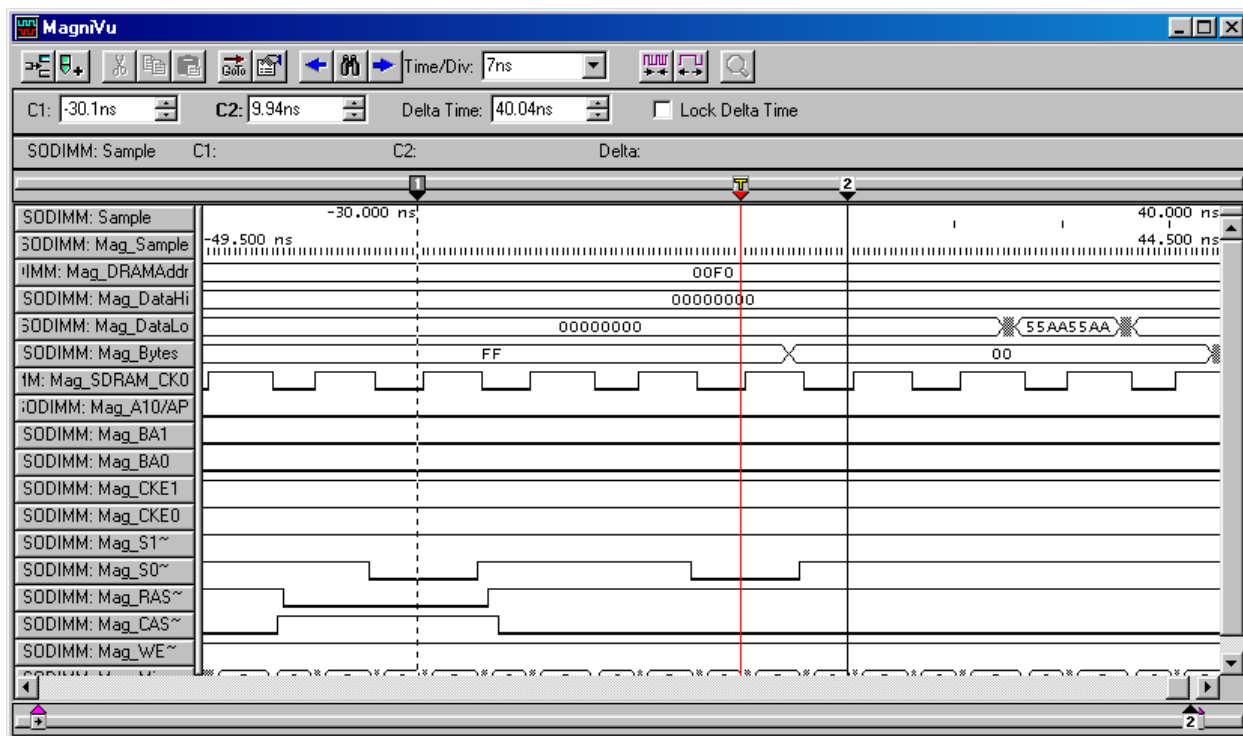


Figure 5- SODIMM MagniVu Display

## 7.0 HINTS & TIPS

### 7.1 Triggering on a Command using SODIMM

The SODIMM support package clocks data into the logic analyzer on the rising edge of the selected SODIMM Clock. Since the clock's rising edge is when Command information is valid this makes for a very easy trigger, as shown in Figure 6. In this case the example is testing for a valid Write command when either S0~ or S1~ are asserted low.

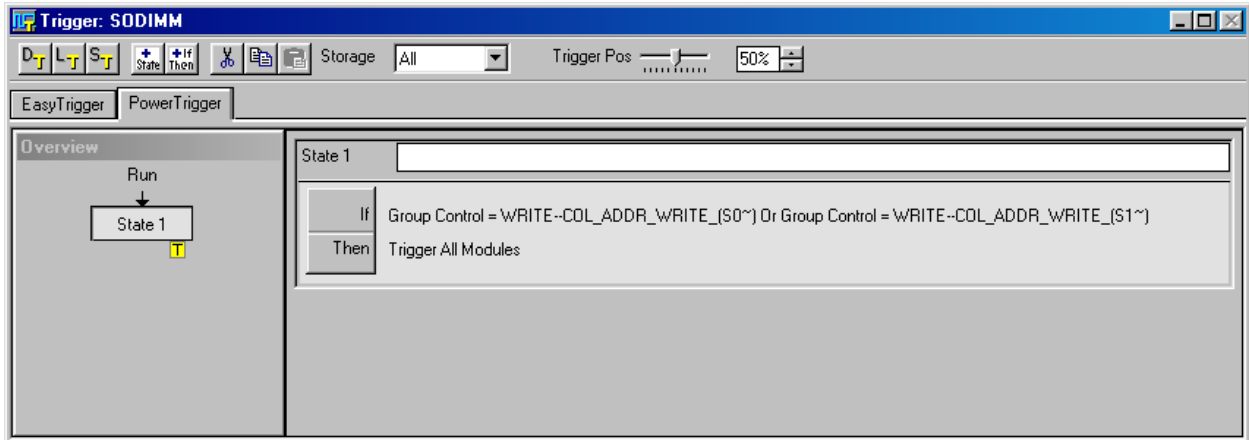


Figure 6- Recommended SODIMM Command Trigger

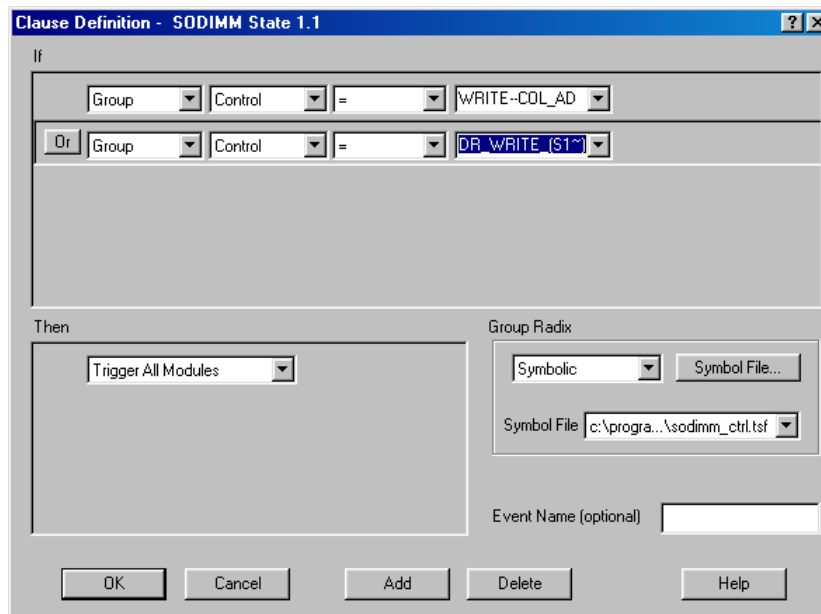
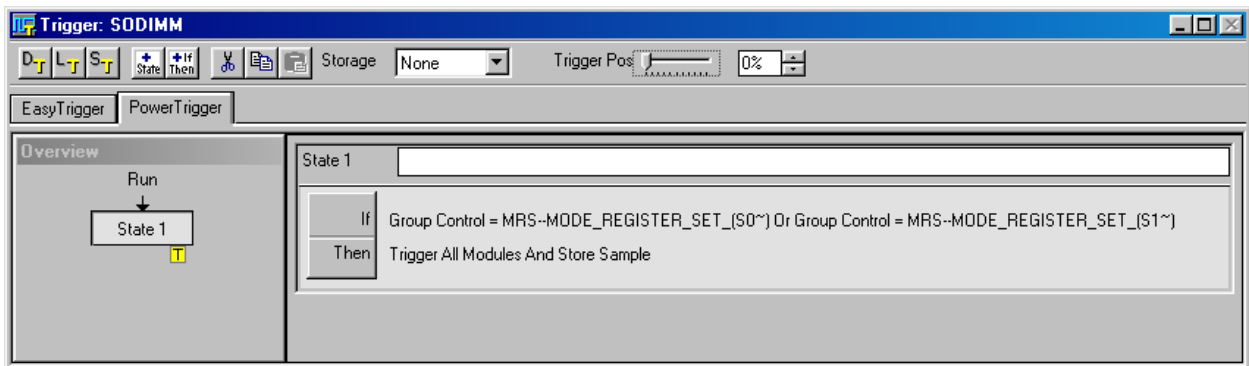


Figure 7- Recommended SODIMM Command Trigger - Detail

## 7.2 Capturing MRS (Mode Register Set) Data

If the characteristics of the SODIMM target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the SODIMM memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the SODIMM support for the post-processing software to properly decode the acquisitions. The TLA trigger shown in Figure 8 can be used to acquire the MRS cycles when using SODIMM support:

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added to the Trigger events, but the method shown ensures that the last valid MRS cycle will be acquired regardless of the memory depth setting of the acquisition card.



**Figure 8- SODIMM MRS Trigger**

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles have been seen during the boot process, and the example trigger shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in Figure 9. The last acquired MRS cycle will reflect the settings used in the SODIMM target – in this case, a CAS latency of 3 cycles with a Burst length of 4 and operating in Multiple Burst / Single Write mode.

Sample	SODIMM DRAMAddr	SODIMM DataHi	SODIMM DataLo	SODIMM Mnemonics	SODIMM Bytes	Timestamp
55	00F0	00000000	00000000	SO REF--REFRESH	FF	21.638,000 us
56	00F0	00000000	00000000	SO REF--REFRESH	FF	21.617,500 us
57	00F0	00000000	00000000	SO REF--REFRESH	FF	86.550,500 us
58	00F0	00000000	00000000	SO REF--REFRESH	FF	21.617,500 us
59	00F0	00000000	00000000	SO REF--REFRESH	FF	21.637,500 us
60	003A	00000000	00000000	SO MRS--MODE REGISTER SET	FF	434.072,500 us
	003A	00000000	00000000	Operating Mode: Multiple Burst/Single Wr>	FF	
	003A	00000000	00000000	Burst Type: Interleaved	FF	
	003A	00000000	00000000	Burst: 4	FF	
	003A	00000000	00000000	Latency: 3	FF	
61	00F0	00000000	00000000	S1 REF--REFRESH	FF	232.665,000 us
62	00F0	00000000	00000000	SO REF--REFRESH	FF	10.000 ns
63	00F0	00000000	00000000	S1 REF--REFRESH	FF	15.588,000 us
64	00F0	00000000	00000000	SO REF--REFRESH	FF	10.000 ns
65	00F0	00000000	00000000	S1 REF--REFRESH	FF	15.588,500 us

Figure 9- MRS Cycle Acquisition Disassembly

## **APPENDIX A - How SODIMM Data is Clocked**

All SODIMM data is acquired on the rising edge of the selected clock (SDRAM CK0 or CK1) with RAS~, CAS~, WE~, CKE0, CKE1, S0~, and S01~ used as clocking qualifiers.

There are two clocking modes that can be selected by the user:

**Selective Clocking** (default) – This mode will reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS~ or CAS~ is asserted low along with S0~ or S1~. After every assertion of CAS~ (with either S0~ or S1~ asserted) an additional 12 samples (Reads) or up to 9 samples (Writes) are taken on every SODIMM CLK rising edge. If CAS~ and a Chip Select are asserted during these storage cycles the count is reset.

**Rising Edge of Clock** – As the name implies this will cause the acquisition card to store data on every Rising edge of the selected SDRAM clock.

## **APPENDIX B - Considerations**

### **B.1 SODIMM Bus Loading**

It must be noted that the NEX-SODIMM Bus Adapter does not provide any buffering of the memory signals. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-SODIMM adapter, to see the exact timing relationships and signal waveforms from the system. This is particularly useful when using the Analog Mux capability of the TLA7AA4 and TLA7AB4 acquisition cards which permits the user to view Analog and Digital data simultaneously through a single probe connection.

## APPENDIX C - SDRAM SODIMM 144-pin Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	2	Vss	73	Reserved	74	CLK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	Reserved	78	Reserved
7	DQ2	8	DQ34	79	Reserved	80	Reserved
9	DQ3	10	DQ35	81	Vdd	82	Vdd
11	Vdd	12	Vdd	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	Vdd	28	Vdd	99	DQ23	100	DQ55
29	A0	30	A3	101	Vdd	102	Vdd
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	Vdd	114	Vdd
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	Vdd	46	Vdd	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	Reserved	58	Reserved	129	Vdd	130	Vdd
59	Reserved	60	Reserved	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	Vdd	64	Vdd	135	DQ30	136	DQ62
65	RAS~	66	CAS~	137	DQ31	138	DQ63
67	WE~	68	CKE1	139	Vss	140	Vss
69	S0~	70	A12	141	SDA	142	SCL
71	S1~	72	A13	143	Vdd	144	Vdd

## **APPENDIX D - NEX-SODIMM Mictor Pinout**

<b>Amp Mictor Pin #</b>	<b>Tek Mictor Pin #</b>	<b>TLA Channel</b>	<b>SODIMM Pin #</b>	<b>SODIMM Signal</b>	<b>Amp Mictor Pin #</b>	<b>Tek Mictor Pin #</b>	<b>TLA Channel</b>	<b>SODIMM Pin #</b>	<b>SODIMM Signal</b>
5	3	CK0		---	6	36	CK1	61	CK0
7	4	A3:7	70	A12	8	35	A1:7		---
9	5	A3:6	60	RSV60	10	34	A1:6	57	RSV57
11	6	A3:5	58	RSV58	12	33	A1:5	59	RSV59
13	7	A3:4	54	DQ47	14	32	A1:4	51	DQ14
15	8	A3:3	52	DQ46	16	31	A1:3	53	DQ15
17	9	A3:2	50	DQ45	18	30	A1:2	47	DQ12
19	10	A3:1	48	DQ44	20	29	A1:1	49	DQ13
21	11	A3:0	44	DQ43	22	28	A1:0	41	DQ10
23	12	A2:7	42	DQ42	24	27	A0:7	43	DQ11
25	13	A2:6	40	DQ41	26	26	A0:6	37	DQ8
27	14	A2:5	38	DQ40	28	25	A0:5	39	DQ9
29	15	A2:4	32	A4	30	24	A0:4	33	A2
31	16	A2:3		---	32	23	A0:3		---
33	17	A2:2		---	34	22	A0:2		---
35	18	A2:1		---	36	21	A0:1		---
37	19	A2:0		---	38	20	A0:0		---

### **Mictor Group A**

<b>Amp Mictor Pin #</b>	<b>Tek Mictor Pin #</b>	<b>TLA Channel</b>	<b>SODIMM Pin #</b>	<b>SODIMM Signal</b>	<b>Amp Mictor Pin #</b>	<b>Tek Mictor Pin #</b>	<b>TLA Channel</b>	<b>SODIMM Pin #</b>	<b>SODIMM Signal</b>
5	3	CLK3	74	CK1	6	36	Q1	65	RAS~
7	4	C3:7	79	RSV79	8	35	C1:7	72	A13
9	5	C3:6	77	RSV77	10	34	C1:6	73	RSV73
11	6	C3:5	85	DQ17	12	33	C1:5	78	RSV78
13	7	C3:4	83	DQ16	14	32	C1:4	80	RSV80
15	8	C3:3	89	DQ19	16	31	C1:3	84	DQ48
17	9	C3:2	87	DQ18	18	30	C1:2	86	DQ49
19	10	C3:1	95	DQ21	20	29	C1:1	88	DQ50
21	11	C3:0	93	DQ20	22	28	C1:0	90	DQ51
23	12	C2:7	99	DQ23	24	27	C0:7	94	DQ52
25	13	C2:6	97	DQ22	26	26	C0:6	96	DQ53
27	14	C2:5	105	A8	28	25	C0:5	98	DQ54
29	15	C2:4	103	A6	30	24	C0:4	100	DQ55
31	16	C2:3	67	WE~	32	23	C0:3	104	A7
33	17	C2:2	69	S0~	34	22	C0:2	106	BA0
35	18	C2:1	68	CKE1	36	21	C0:1	110	BA1
37	19	CK3	71	S1~	38	20	A0:0	112	A11

### **Mictor Group C**

## **APPENDIX D - NEX-SODIMM Mictor Pinout (cont'd)**

Amp Mictor Pin #	Tek Mictor Pin #	TLA Channel	SODIMM Pin #	SODIMM Signal	Amp Mictor Pin #	Tek Mictor Pin #	TLA Channel	SODIMM Pin #	SODIMM Signal
5	3	Q0		---	6	36	CK2	142	SCL
7	4	D3:7	118	DQMB7	8	35	D1:7	109	A9
9	5	D3:6	124	DQ57	10	34	D1:6	115	DQMB2
11	6	D3:5	128	DQ59	12	33	D1:5	121	DQ24
13	7	D3:4	134	DQ61	14	32	D1:4	125	DQ26
15	8	D3:3	138	DQ63	16	31	D1:3	131	DQ28
17	9	D3:2	116	DQMB6	18	30	D1:2	135	DQ30
19	10	D3:1	122	DQ56	20	29	D1:1	141	SDA
21	11	D3:0	126	DQ58	22	28	D1:0	111	A10
23	12	D2:7	132	DQ60	24	27	D0:7	117	DQMB3
25	13	D2:6	136	DQ62	26	26	D0:6	123	DQ25
27	14	D2:5		---	28	25	D0:5	127	DQ27
29	15	D2:4		---	30	24	D0:4	133	DQ29
31	16	D2:3		---	32	23	D0:3	137	DQ31
33	17	D2:2		---	34	22	D0:2		---
35	18	D2:1		---	36	21	D0:1		---
37	19	D2:0		---	38	20	D0:0		---

### **Mictor Group D**

Amp Mictor Pin #	Tek Mictor Pin #	TLA Channel	SODIMM Pin #	SODIMM Signal	Amp Mictor Pin #	Tek Mictor Pin #	TLA Channel	SODIMM Pin #	SODIMM Signal
5	3	Q3	62	CKE0~	6	36	Q2	66	CAS~
7	4	E3:7	29	A0	8	35	E1:7	26	DQMB5
9	5	E3:6	23	DQMB0	10	34	E1:6	20	DQ39
11	6	E3:5	17	DQ6	12	33	E1:5	16	DQ37
13	7	E3:4	13	DQ4	14	32	E1:4	10	DQ35
15	8	E3:3	7	DQ2	16	31	E1:3	6	DQ33
17	9	E3:2	1	DQ0	18	30	E1:2	4	DQ32
19	10	E3:1	31	A1	20	29	E1:1	34	A5
21	11	E3:0	25	DQMB1	22	28	E1:0	30	A3
23	12	E2:7	19	DQ7	24	27	E0:7	24	DQMB4
25	13	E2:6	15	DQ5	26	26	E0:6	18	DQ38
27	14	E2:5	9	DQ3	28	25	E0:5	14	DQ36
29	15	E2:4	5	DQ1	30	24	E0:4	8	DQ34
31	16	E2:3		---	32	23	E0:3		---
33	17	E2:2		---	34	22	E0:2		---
35	18	E2:1		---	36	21	E0:1		---
37	19	E2:0		---	38	20	E0:0		---

### **Mictor Group E**

## **APPENDIX E – NEX-SODIMM P6860 Compression Probe Pinout**

For further information on the P6860 Connectorless probe compression footprint, please refer to the “P6810, P6860 and P6880 Logic Analyzer Probes Instruction Manual”, Tektronix part number 071-1059-00.

<b>Pad #</b>	<b>TLA Channel</b>	<b>DDR Pin #</b>	<b>DDR Signal Name</b>
A15	CK1-	---	GND
A13	CK1+	61	CK0
B12	A1:7		---
B10	A1:6	57	RSV57
A12	A1:5	59	RSV59
A10	A1:4	51	DQ14
B9	A1:3	53	DQ15
B7	A1:2	47	DQ12
A9	A1:1	49	DQ13
A7	A1:0	41	DQ10
B6	A0:7	43	DQ11
B4	A0:6	37	DQ8
A6	A0:5	39	DQ9
A4	A0:4	33	A2
B3	A0:3		---
B1	A0:2		---
A3	A0:1		---
A1	A0:0		---

**Probe Connection A0/A1**

<b>Pad #</b>	<b>TLA Channel</b>	<b>DDR Pin #</b>	<b>DDR Signal Name</b>
A15	CK0-		
A13	CK0+		---
B12	A3:7	70	A12
B10	A3:6	60	RSV60
A12	A3:5	58	RSV58
A10	A3:4	54	DQ47
B9	A3:3	52	DQ46
B7	A3:2	50	DQ45
A9	A3:1	48	DQ44
A7	A3:0	44	DQ43
B6	A2:7	42	DQ42
B4	A2:6	40	DQ41
A6	A2:5	38	DQ40
A4	A2:4	32	A4
B3	A2:3		---
B1	A2:2		---
A3	A2:1		---
A1	A2:0		---

**Probe Connection A2/A3**

Pad #	TLA Channel	DDR Pin #	DDR Signal Name
A15	Q1-	---	GND
A13	Q1+	65	RAS~
B12	C1:7	72	A13
B10	C1:6	73	RSV73
A12	C1:5	78	RSV78
A10	C1:4	80	RSV80
B9	C1:3	84	DQ48
B7	C1:2	86	DQ49
A9	C1:1	88	DQ50
A7	C1:0	90	DQ51
B6	C0:7	94	DQ52
B4	C0:6	96	DQ53
A6	C0:5	98	DQ54
A4	C0:4	100	DQ55
B3	C0:3	104	A7
B1	C0:2	106	BA0
A3	C0:1	110	BA1
A1	A0:0	112	A11

**Probe Connection C0/C1**

Pad #	TLA Channel	DDR Pin #	DDR Signal Name
A15	CK3-	---	GND
A13	CLK3+	74	CK1
B12	C3:7	79	RSV79
B10	C3:6	77	RSV77
A12	C3:5	85	DQ17
A10	C3:4	83	DQ16
B9	C3:3	89	DQ19
B7	C3:2	87	DQ18
A9	C3:1	95	DQ21
A7	C3:0	93	DQ20
B6	C2:7	99	DQ23
B4	C2:6	97	DQ22
A6	C2:5	105	A8
A4	C2:4	103	A6
B3	C2:3	67	WE~
B1	C2:2	69	S0~
A3	C2:1	68	CKE1
A1	CK3	71	S1~

**Probe Connection C2/C3**

Pad #	TLA Channel	DDR Pin #	DDR Signal Name
A15	CK2-	---	GND
A13	CK2	142	SCL
B12	D1:7	109	A9
B10	D1:6	115	DQMB2
A12	D1:5	121	DQ24
A10	D1:4	125	DQ26
B9	D1:3	131	DQ28
B7	D1:2	135	DQ30
A9	D1:1	141	SDA
A7	D1:0	111	A10
B6	D0:7	117	DQMB3
B4	D0:6	123	DQ25
A6	D0:5	127	DQ27
A4	D0:4	133	DQ29
B3	D0:3	137	DQ31
B1	D0:2		---
A3	D0:1		---
A1	D0:0		---

**Probe Connection D0/D1**

Pad #	TLA Channel	DDR Pin #	DDR Signal Name
A15	Q0-		
A13	Q0+		---
B12	D3:7	118	DQMB7
B10	D3:6	124	DQ57
A12	D3:5	128	DQ59
A10	D3:4	134	DQ61
B9	D3:3	138	DQ63
B7	D3:2	116	DQMB6
A9	D3:1	122	DQ56
A7	D3:0	126	DQ58
B6	D2:7	132	DQ60
B4	D2:6	136	DQ62
A6	D2:5		---
A4	D2:4		---
B3	D2:3		---
B1	D2:2		---
A3	D2:1		---
A1	D2:0		---

**Probe Connection D2/D3**

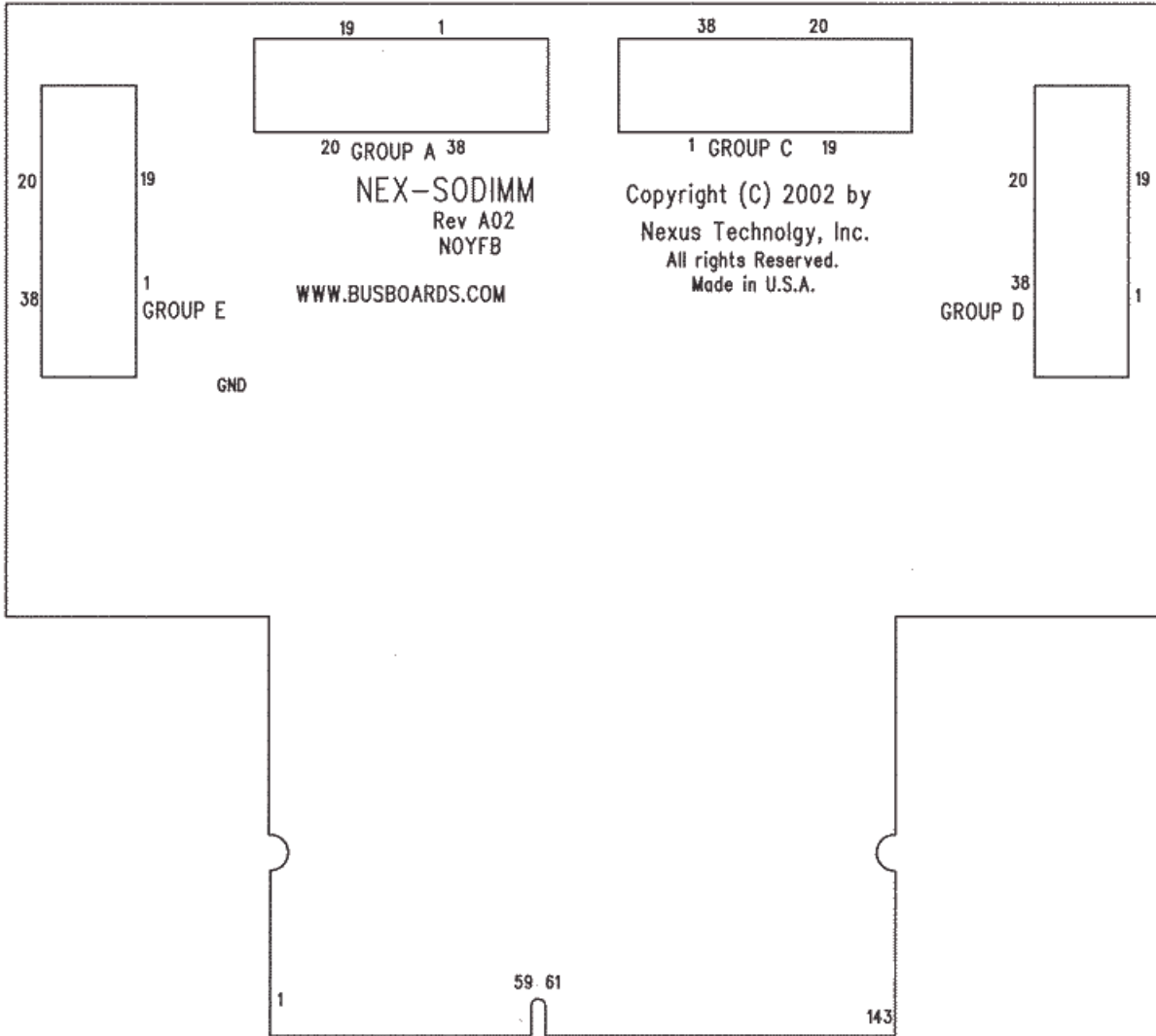
Pad #	TLA Channel	DDR Pin #	DDR Signal Name
A15	Q2-	---	GND
A13	Q2+	66	CAS~
B12	E1:7	26	DQMB5
B10	E1:6	20	DQ39
A12	E1:5	16	DQ37
A10	E1:4	10	DQ35
B9	E1:3	6	DQ33
B7	E1:2	4	DQ32
A9	E1:1	34	A5
A7	E1:0	30	A3
B6	E0:7	24	DQMB4
B4	E0:6	18	DQ38
A6	E0:5	14	DQ36
A4	E0:4	8	DQ34
B3	E0:3		---
B1	E0:2		---
A3	E0:1		---
A1	E0:0		---

**Probe Connection E0/E1**

Pad #	TLA Channel	DDR Pin #	DDR Signal Name
A15	Q3-		
A13	Q3+	62	CKE0~
B12	E3:7	29	A0
B10	E3:6	23	DQMB0
A12	E3:5	17	DQ6
A10	E3:4	13	DQ4
B9	E3:3	7	DQ2
B7	E3:2	1	DQ0
A9	E3:1	31	A1
A7	E3:0	25	DQMB1
B6	E2:7	19	DQ7
B4	E2:6	15	DQ5
A6	E2:5	9	DQ3
A4	E2:4	5	DQ1
B3	E2:3		---
B1	E2:2		---
A3	E2:1		---
A1	E2:0		---

**Probe Connection E2/E3**

## APPENDIX F – NEX-SODIMM Silkscreen



## **APPENDIX G - Support**

### **About Nexus Technology, Inc.**



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.  
78 Northeastern Blvd. #2  
Nashua, NH 03062

TEL: 877-595-8116  
FAX: 877-595-8118

Web site: <http://www.nexustechnology.com>

### **Support Contact Information**

Technical Support	<b><a href="mailto:techsupport@nexustechnology.com">techsupport@nexustechnology.com</a></b>
General Information	<b><a href="mailto:support@nexustechnology.com">support@nexustechnology.com</a></b>
Quote Requests	<b><a href="mailto:quotes@nexustechnology.com">quotes@nexustechnology.com</a></b>

We will try to respond within one business day.

### **If Problems Are Found**

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

## **APPENDIX H - References**

JEDEC Standard No. 21-C “Configurations for Solid State Memories”

Release 7, January 1997

Hitachi HB526C264EN/464EN Series Synchronous Dynamic RAM Module Data Sheet

ADE-203-629 (Z), Preliminary, Rev. 0.0, Aug 20, 1996

Intel 133MHz PC SDRAM Unbuffered SO-DIMM Specification

Revision 1.0C, August 2000

Tektronix TLA700 System User’s Manual

Tektronix TLA700 Logic Analyzer User’s Manual