



NEX-VME64 & NEX-VME64X VME 64 Bus Adapter Users Manual

Including these Software Support packages:
VME64Ful VME64Ltd

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1.0 OVERVIEW

1.1 General Information

The NEX-VME64 product is the same as the NEX-VME64X except for the P0 connector. While the P0 connector is installed on the NEX-VME64X adapter it is not installed on the NEX-VME64 adapter. The P0 connectors are shipped with the NEX-VME64 product in case they are needed at a later date.

The NEX-VME64X adapter has been designed to provide a quick and easy connection to interface a Tektronix TLA-Series Logic Analyzer to a VME, VME64 or VME64X backplane. Logic Analyzer connections are made through P6434 probes or P6860 High-Density Connectorless probes with Mictor-on-PCB to Compression adapters.

The NEX-VME64X support requires the following Tektronix Logic Analyzer acquisition configurations:

Full Acquisition

To acquire the VME, VME64 or VME64X bus signals including the seven IRQ's requires at a minimum a TLA acquisition system with 136-channels. This can be made up as follows:

- A TLA700-series analyzer with a TLA7L/M/N/P/Q4 136-channel acquisition card and four P6434 probes,
- A TLA700-series analyzer with a TLA7AA4 or TLA7AB4 136-channel acquisition card, four P6860 probes and four Mictor-on-PCB to Compression adapters,
- A TLA6X4 with four P6434 probes,
- A TLA5204 Logic Analyzer with either four P6434 probes or eight P6419 probes and four Mictor-on-PCB to Compression adapters.

Merged acquisition cards can also be used to acquire more than 136 VME signals.

Limited Signal Acquisition

The TLA channel count requirement can be reduced from 136-channels to 102-channels by looking at only one of the seven IRQ signals on the VME, VME64 or VME64X bus. This option is jumper selectable on the NEX-VME64X. If Limited Signal Acquisition mode is used the user would connect the TLA to three of the four available 38-pin Mictor connectors on the NEX-VME64X adapter. The TLA requirements to support this acquisition mode are as follows:

- A TLA700-series analyzer with a TLA7L/M/N/P/Q3 102-channel or TLA7L/M/N/P/Q4 136-channel acquisition card and three P6434 probes,

- A TLA700-series analyzer with a TLA7AA3/AB3 102-channel acquisition card or TLA7AA4/AB4 136-channel acquisition card, three P6860 probes and three Mictor-on-PCB to Compression adapters,
- A TLA6X3 or TLA6X4 with three P6434 probes,
- A TLA5203 or TLA5204 Logic Analyzer with either three P6434 probes or six P6419 probes and three Mictor-on-PCB to Compression adapters.

The NEX-VME64X software also post-processes the acquired data to display valid cycle information to the user.

Note that this manual uses some terms generically. For instance, references to a TLA apply to all suitable TLA5000/600/700 Logic Analyzers unless otherwise noted. References to the VME64 bus apply to both the VME64 and VME64X variants unless otherwise noted.

Appendix E has a silk-screened print of the NEX-VME64X adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the VME64X Specification and the Tektronix TLA Logic Analyzers. It is also expected that the user is familiar with the Windows environment used on the TLA (Win95, Win98 or Win2000).

2.0 SOFTWARE INSTALLATION

The NEX-VME64X software is installed using the same method as other Windows programs. Place the *VME64Ful* or *VME64Ltd* Install disk in the floppy drive of the TLA. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA, first select the desired Logic Analyzer module in the Setup window, select Load Support Package from the File pull-down, then choose *VME64Ful* or *VME64Ltd* and click on **Okay**.

3.0 CONNECTING to the NEX-VME64X ADAPTER

3.1 General

The NEX-VME64X adapter is larger than a standard VME64/VME64X module and is designed to function as an extender card, providing an easy connection to the logic analyzer for VME64 data acquisition. Because of this design approach it is entirely possible that placing a target card onto the NEX-VME64X adapter may result in improper operation of the target card and/or system.

The TLA Logic analyzer probes should be connected to the NEX-VME64X adapter by following the silk screen. The standard connections are made to Mictor connectors labeled Group A, C, D, and E which correspond to Tektronix probe channel groups A, C, D, and E.

IMPORTANT: Care should be taken when ejecting a VME customer board from the NEX-VME64X adapter. The card guides should not have excessive force applied to them or the guides could be cracked or damaged.

3.2 Jumper Installation for Limited Signal Acquisition

When using Limited Signal Acquisition, only one IRQ can be monitored. The IRQ selection is made by installing a jumper on the appropriate IRQ header pins (Fig. 1).

NOTE: Placing more than one jumper on the IRQ header pins may result in failure of the target to operate. Under no circumstances should more than one IRQ jumper be installed.

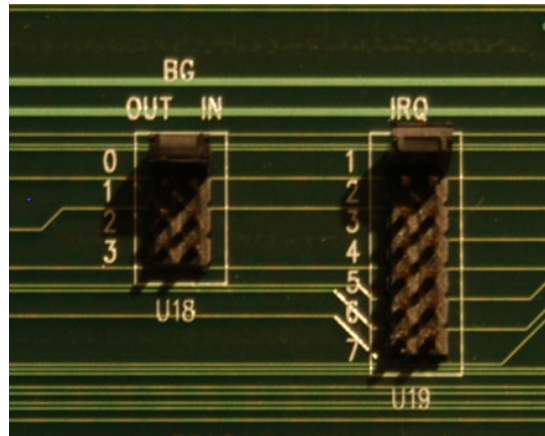


Figure 1- BG Jumper Installed

3.3 Jumper Installation for Connecting BGIN/BGOUT

If required BGIN can be connected to BGOUT on the NEX-VME64X adapter. This is done by installing a jumper on the appropriate BG OUT/IN header pins.

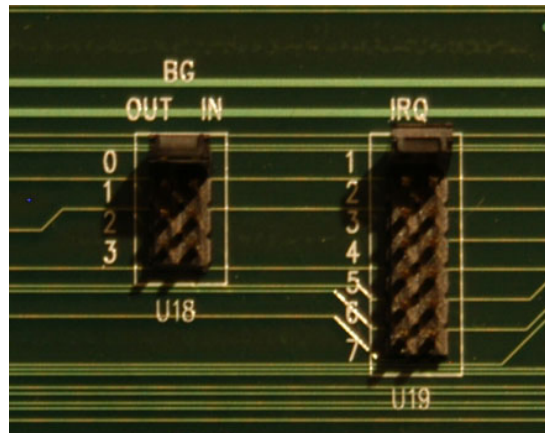


Figure 2- IRQ Jumper Installed

3.4 Connecting the TLA to User Defined or other signals

User Defined or other signals can be probed with the TLA700 by soldering the included dual in-line right angle headers to the NEX-VME64X adapter. Please refer to Figure 5 for an image of the header installed in the NEX-VME64 adapter. It is important to note the orientation of the pins - the black plastic piece should be flat against the adapter board. If the header is installed incorrectly the Tektronix probes will not have sufficient mechanical clearance to connect to the headers. Once the right angle headers are installed the TLA700 can connect to the headers using Tektronix P6417/P6418 or similar flying lead probes.

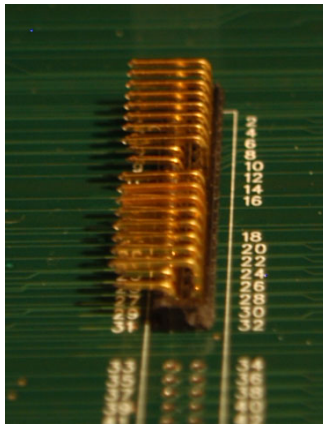


Figure 3- Right angle headers installed in a NEX-VME64X adapter

The following VME64X signals are routed to UA1 on the NEX-VME64X adapter. The silk screen shows the signal names for the headers. The routing to the TLA will depend on the probe connected to these headers.

VME64X pins: D5, D8, D9, D10, D11, D13, D15, D17, D19, D21, D23, D25, D27, D29, Z1, Z3, Z5, Z7, Z9, Z11, Z13, Z15, Z17, Z19, Z21, Z23, Z25, Z27, Z29, Z31.

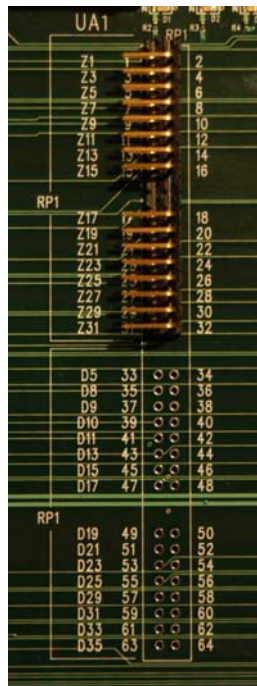


Figure 4- Right angle headers installed in a NEX-VME64X adapter

There are many User Defined Signals. The NEX-VME64X adapter provides the ability to monitor a maximum of 64 of them. U24 and U25 can have the included right angle headers soldered onto the NEX-VME64X adapter for connection to User Defined Signals. Every pin on

U24 and U25 has an associated pad. This pad can be connected to any User Defined signal that is routed to P0 and P2. This connection is made with a thin wire (30awg wire wrap wire is suggested) that must be soldered between P0/P2 and U24/U25. P0 and P2 copy the VME64X J0 and J2 connector pinout so an easy reference to the desired User Defined Signal is possible

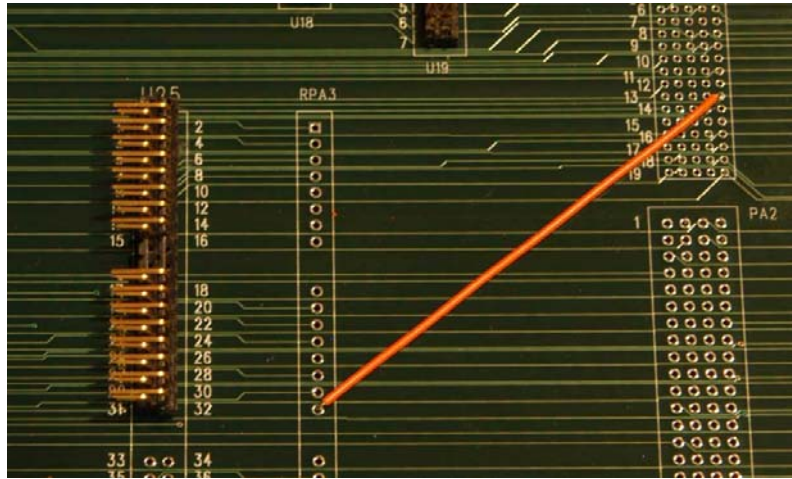


Figure 5- Wire added to connect User Defined signal to U25

CAUTION!!!

It is the responsibility of the user to ensure that the input voltage requirements of the TLA Acquisition card are not exceeded when connected to a User Defined signal. Please refer to the acquisition card and probe specifications from Tektronix, or contact your local Tektronix representative, to ensure that no equipment will be damaged by the voltage levels of a User Defined signal. Nexus Technology, Inc. assumes no responsibility or liability for damage caused to any equipment caused by connecting said equipment to any VME, VME64, or VME64X signal.

Group Name	Signal Name	VME64X Pin #	TLA Input	Group Name	Signal Name	VME64X Pin #	TLA Input
A16_Addr (Hex)	ADD15	P1.C23	A1:7	A32_Addr (Hex)	ADD31	P2.B11	A3:7
	ADD14	P1.C24	A1:6		ADD30	P2.B10	A3:6
	ADD13	P1.C25	A1:5		ADD29	P2.B9	A3:5
	ADD12	P1.C26	A1:4		ADD28	P2.B8	A3:4
	ADD11	P1.C27	A1:3		ADD27	P2.B7	A3:3
	ADD10	P1.C28	A1:2		ADD26	P2.B6	A3:2
	ADD9	P1.C29	A1:1		ADD25	P2.B5	A3:1
	ADD8	P1.C30	A1:0		ADD24	P2.B4	A3:0
	ADD7	P1.A24	A0:7		ADD23	P1.C15	A2:7
	ADD6	P1.A25	A0:6		ADD22	P1.C16	A2:6
	ADD5	P1.A26	A0:5		ADD21	P1.C17	A2:5
	ADD4	P1.A27	A0:4		ADD20	P1.C18	A2:4
	ADD3	P1.A28	A0:3		ADD19	P1.C19	A2:3
	ADD2	P1.A29	A0:2		ADD18	P1.C20	A2:2
	ADD1	P1.A30	A0:1		ADD17	P1.C21	A2:1
	ADD0	GND	A0:0		ADD16	P1.C22	A2:0
A24_Addr (Hex)	ADD23	P1.C15	A2:7	ADD15	P1.C23	A1:7	
	ADD22	P1.C16	A2:6	ADD14	P1.C24	A1:6	
	ADD21	P1.C17	A2:5	ADD13	P1.C25	A1:5	
	ADD20	P1.C18	A2:4	ADD12	P1.C26	A1:4	
	ADD19	P1.C19	A2:3	ADD11	P1.C27	A1:3	
	ADD18	P1.C20	A2:2	ADD10	P1.C28	A1:2	
	ADD17	P1.C21	A2:1	ADD9	P1.C29	A1:1	
	ADD16	P1.C22	A2:0	ADD8	P1.C30	A1:0	
	ADD15	P1.C23	A1:7	ADD7	P1.A24	A0:7	
	ADD14	P1.C24	A1:6	ADD6	P1.A25	A0:6	
	ADD13	P1.C25	A1:5	ADD5	P1.A26	A0:5	
	ADD12	P1.C26	A1:4	ADD4	P1.A27	A0:4	
	ADD11	P1.C27	A1:3	ADD3	P1.A28	A0:3	
	ADD10	P1.C28	A1:2	ADD2	P1.A29	A0:2	
	ADD9	P1.C29	A1:1	ADD1	P1.A30	A0:1	
	ADD8	P1.C30	A1:0	ADD0	GND	A0:0	
	ADD7	P1.A24	A0:7	Ungrouped	BG3OUT*		C1:3
	ADD6	P1.A25	A0:6		BG2OUT*		C1:2
	ADD5	P1.A26	A0:5		BG1OUT*		C1:1
	ADD4	P1.A27	A0:4		BG0OUT*		C1:0
	ADD3	P1.A28	A0:3		IACKIN*		C2:5
	ADD2	P1.A29	A0:2		IACKOUT		C2:3
					*		
	ADD1	P1.A30	A0:1		SERB		C1:5
	ADD0	GND	A0:0		SERA		C1:4

Table 1- VME64Ful/Ltd TLA Channel Grouping

Group Name	Signal Name	VME64X Pin #	TLA Input	Group Name	Signal Name	VME64X Pin #	TLA Input
A40_Addr (Hex)	DAT7	P1.A8	D0:7	Transfer (Sym)	DS1*		C2:2
	DAT6	P1.A7	D0:6		DS0*		C2:1
	DAT5	P1.A6	D0:5	ADD1		A0:1	
	DAT4	P1.A5	D0:4	LWORD*		C2:0	
	DAT3	P1.A4	D0:3	ADD2		A0:2	
	DAT2	P1.A3	D0:2	Mode (Sym)	AM5		C3:7
	DAT1	P1.A2	D0:1		AM4		C3:6
	DAT0	P1.A1	D0:0		AM3		C3:5
	DAT15	P1.C8	D1:7		AM2		C3:4
	DAT14	P1.C7	D1:6		AM1		C3:3
	DAT13	P1.C6	D1:5	AM0		C3:2	
	DAT12	P1.C5	D1:4	Control (Sym)	RETRY*		CK2
	DAT11	P1.C4	D1:3		AS*		CK0
	DAT10	P1.C3	D1:2		DTACK*		CK1
	DAT9	P1.C2	D1:1		BERR*		CK3
	DAT8	P1.C1	D1:0	WRITE*		C2:4	
	ADD23	P1.C15	A2:7	Misc (Sym)	SYSCLK		Q0
	ADD22	P1.C16	A2:6		SYSRESET		Q1
	ADD21	P1.C17	A2:5		*		
	ADD20	P1.C18	A2:4		ACFAIL*		C1:7
	ADD19	P1.C19	A2:3		SYSFAIL*		C1:6
	ADD18	P1.C20	A2:2		IACK*		C2:7
	ADD17	P1.C21	A2:1		IRQx*		See Note
	ADD16	P1.C22	A2:0	BusReq (Hex)	BCLR*		C3:0
	ADD15	P1.C23	A1:7		BBSY*		C3:1
	ADD14	P1.C24	A1:6		BR3*		C0:3
	ADD13	P1.C25	A1:5		BR2*		C0:2
	ADD12	P1.C26	A1:4		BR1*		C0:1
	ADD11	P1.C27	A1:3	BusGrant (Hex)	BR0*		C0:0
	ADD10	P1.C28	A1:2		BG3IN*		C0:7
ADD9	P1.C29	A1:1	BG2IN*			C0:6	
ADD8	P1.C30	A1:0	BG1IN*			C0:5	
ADD7	P1.A24	A0:7		BG0IN*		C0:4	
ADD6	P1.A25	A0:6	Interrupts (Bin)	IRQ7*		E0:6	
ADD5	P1.A26	A0:5		IRQ6*		E0:5	
ADD4	P1.A27	A0:4	VME64Ful only	IRQ5*		E0:4	
ADD3	P1.A28	A0:3		IRQ4*		E0:3	
ADD2	P1.A29	A0:2		IRQ3*		E0:2	
ADD1	P1.A30	A0:1		IRQ2*		E0:1	
ADD0	GND	A0:0		IRQ1*		E0:0	

Table 1 – VME64Ful/Ltd TLA Channel Grouping (cont'd.)

Note: IRQx is the jumper selectable IRQ signal that is selected as described in Section 3.2 Jumper Installation for Limited Signal Acquisition

Group Name	Signal Name	VME64X Pin #	TLA Input	Group Name	Signal Name	VME64X Pin #	TLA Input
A64_Addr Bits 63-32 (Hex)	DAT31	P2.B30	D3:7	A64_Addr (cont'd) Bits 31-0 (Hex)	ADD31	P2.B11	A3:7
	DAT30	P2.B29	D3:6		ADD30	P2.B10	A3:6
	DAT29	P2.B28	D3:5		ADD29	P2.B9	A3:5
	DAT28	P2.B27	D3:4		ADD28	P2.B8	A3:4
	DAT27	P2.B26	D3:3		ADD27	P2.B7	A3:3
	DAT26	P2.B25	D3:2		ADD26	P2.B6	A3:2
	DAT25	P2.B24	D3:1		ADD25	P2.B5	A3:1
	DAT24	P2.B23	D3:0		ADD24	P2.B4	A3:0
	DAT23	P2.B21	D2:7		ADD23	P1.C15	A2:7
	DAT22	P2.B20	D2:6		ADD22	P1.C16	A2:6
	DAT21	P2.B19	D2:5		ADD21	P1.C17	A2:5
	DAT20	P2.B18	D2:4		ADD20	P1.C18	A2:4
	DAT19	P2.B17	D2:3		ADD19	P1.C19	A2:3
	DAT18	P2.B16	D2:2		ADD18	P1.C20	A2:2
	DAT17	P2.B15	D2:1		ADD17	P1.C21	A2:1
	DAT16	P2.B14	D2:0		ADD16	P1.C22	A2:0
	DAT15	P1.C8	D1:7		ADD15	P1.C23	A1:7
	DAT14	P1.C7	D1:6		ADD14	P1.C24	A1:6
	DAT13	P1.C6	D1:5		ADD13	P1.C25	A1:5
	DAT12	P1.C5	D1:4		ADD12	P1.C26	A1:4
	DAT11	P1.C4	D1:3		ADD11	P1.C27	A1:3
	DAT10	P1.C3	D1:2		ADD10	P1.C28	A1:2
	DAT9	P1.C2	D1:1		ADD9	P1.C29	A1:1
	DAT8	P1.C1	D1:0		ADD8	P1.C30	A1:0
	DAT7	P1.A8	D0:7		ADD7	P1.A24	A0:7
	DAT6	P1.A7	D0:6		ADD6	P1.A25	A0:6
	DAT5	P1.A6	D0:5		ADD5	P1.A26	A0:5
	DAT4	P1.A5	D0:4		ADD4	P1.A27	A0:4
	DAT3	P1.A4	D0:3		ADD3	P1.A28	A0:3
	DAT2	P1.A3	D0:2		ADD2	P1.A29	A0:2
	DAT1	P1.A2	D0:1		ADD1	P1.A30	A0:1
	DAT0	P1.A1	D0:0		ADD0	GND	A0:0

Table 1 – VME64Ful/Ltd TLA Channel Grouping (cont'd.)

Group Name	Signal Name	VME64X Pin #	TLA Input	Group Name	Signal Name	VME64X Pin #	TLA Input
RawData (Hex)	DAT31	P2.B30	D3:7	RawAddr (Hex)	ADD31	P2.B11	A3:7
	DAT30	P2.B29	D3:6		ADD30	P2.B10	A3:6
	DAT29	P2.B28	D3:5		ADD29	P2.B9	A3:5
	DAT28	P2.B27	D3:4		ADD28	P2.B8	A3:4
	DAT27	P2.B26	D3:3		ADD27	P2.B7	A3:3
	DAT26	P2.B25	D3:2		ADD26	P2.B6	A3:2
	DAT25	P2.B24	D3:1		ADD25	P2.B5	A3:1
	DAT24	P2.B23	D3:0		ADD24	P2.B4	A3:0
	DAT23	P2.B21	D2:7		ADD23	P1.C15	A2:7
	DAT22	P2.B20	D2:6		ADD22	P1.C16	A2:6
	DAT21	P2.B19	D2:5		ADD21	P1.C17	A2:5
	DAT20	P2.B18	D2:4		ADD20	P1.C18	A2:4
	DAT19	P2.B17	D2:3		ADD19	P1.C19	A2:3
	DAT18	P2.B16	D2:2		ADD18	P1.C20	A2:2
	DAT17	P2.B15	D2:1		ADD17	P1.C21	A2:1
	DAT16	P2.B14	D2:0		ADD16	P1.C22	A2:0
	DAT15	P1.C8	D1:7		ADD15	P1.C23	A1:7
	DAT14	P1.C7	D1:6		ADD14	P1.C24	A1:6
	DAT13	P1.C6	D1:5		ADD13	P1.C25	A1:5
	DAT12	P1.C5	D1:4		ADD12	P1.C26	A1:4
	DAT11	P1.C4	D1:3		ADD11	P1.C27	A1:3
	DAT10	P1.C3	D1:2		ADD10	P1.C28	A1:2
	DAT9	P1.C2	D1:1		ADD9	P1.C29	A1:1
	DAT8	P1.C1	D1:0		ADD8	P1.C30	A1:0
	DAT7	P1.A8	D0:7		ADD7	P1.A24	A0:7
	DAT6	P1.A7	D0:6		ADD6	P1.A25	A0:6
	DAT5	P1.A6	D0:5		ADD5	P1.A26	A0:5
	DAT4	P1.A5	D0:4		ADD4	P1.A27	A0:4
	DAT3	P1.A4	D0:3		ADD3	P1.A28	A0:3
	DAT2	P1.A3	D0:2		ADD2	P1.A29	A0:2
	DAT1	P1.A2	D0:1		ADD1	P1.A30	A0:1
	DAT0	P1.A1	D0:0		ADD0	GND	A0:0

Table 1 – VME64Ful/Ltd TLA Channel Grouping (cont'd.)

Note: IRQx is the jumper selectable IRQ signal that is selected as described in Section 3.2 Jumper Installation for Limited Signal Acquisition

4.0 CLOCK SELECTION

There are no clocking selections for VME64X support. The default VME64Ful/Ltd clocking will acquire and store all data on the falling edges of AS*, DTACK*, BERR* and RETRY*.

5.0 VIEWING DATA

5.1 Viewing State Data on the TLA

After making an initial acquisition, the TLA will display the data in the Listing (State) format. Several Symbol Tables have been included in the support package to make the acquired data easier to read (see Tables 2, 3, 4 and 5).

It is important to note that changing the group, channel, or wiring of and of the groups that use Symbol tables can result in incorrect symbol information being displayed.

Symbol	Definition
QUAD/OCTAL_BYTE	0000x
DOUBLE_BYTE_0-1	0001x
BYTE_1-2_R_OR_W	0010x
DOUBLE_BYTE_2-3	0011x
BYTE_0-2_R_OR_W	0100x
SINGLE_EVEN_BYTE0	0101x
ILLEGAL	0110
SINGLE_EVEN_BYTE2	0111x
BYTE_1-3_R_OR_W	1000x
SINGLE_ODD_BYTE1	1001x
ILLEGAL	1010
SINGLE_ODD_BYTE3	1011x
ADDRESS_ONLY	11xxx

Table 2- VME64Ful/Ltd Transfer Symbol Table
Signals, left-to-right: DS1* DS0* A1 LWORD* A2

Symbol	Definition
RETRY	0xxxx
ADDRESS-WRITE	10110
ADDRESS-READ	10111
DTACK	1x01x
BUS_ERROR	1xx0x

Table 3- VME64Ful/Ltd Control Symbol Table

Signals, left-to-right: RETRY*, AS*, DTACK*, BERR*, WRITE*

Symbol	Definition
SYS_RESET	x0xxxx
AC_FAIL	xx0xxx
SYS_FAIL	xxx0xx
INTERRUPT	x111x0

Table 4- VME64Ful/Ltd Misc. Symbol Table

Signals, left-to-right: SYSCLK, SYSRESET*, ACFAIL*, SYSFAIL*, IACK*, IRQx*

Symbol	Definition
A24_Sup_BLT	111111
A24_Sup_pgm_access	111110
A24_Sup_data_access	111101
A24_Sup_64-bit_BLT	111100
A24_Non-priv_BLT	111011
A24_Non-priv_pgm_access	111010
A24_Non-priv_dat_access	111001
A24_Non-priv_64-bit_BLT	111000
A40BLT	110111
Reserved	110110
A40_Lock_command	110101
A40_access	110100
Reserved	110011
A24_Lock_command	110010
Reserved	110001
Reserved	110000
CR/CSR_register	101111
Reserved	101110
A16_Sup_access	101101
A16_Lock_command	101100
Reserved	101011
Reserved	101010
A16_Non-priv_access	101001
Reserved	101010
A16_Non-priv_access	101001
A16_Non-priv_access	101001
Reserved	101010
A16_Non-priv_access	101001

Table 5- VME64Ful/Ltd Mode Symbol Table

Signals, left-to-right: AM5, AM4, AM3, AM2, AM1, AM0

Symbol	Definition
Reserved	101000
Reserved	100111
Reserved	100110
Reserved	100101
Reserved	100100
Reserved	100011
Reserved	100010
Reserved	100001
User-defined	010010
User-defined	010001
User-defined	010000
A32_Sup_BLT	001111
A32_Sup_pgm_access	001110
A32_Sup_data_access	001101
A32_Sup_64-bit_MBLT	001100
A32_Non-priv_BLT	001011
A32_Non-priv_pgm_access	001010
A32_Non-priv_data_access	001001
A32_Non-priv_64-bit_MBLT	001000
Reserved	000111
Reserved	000110
A32_Lock_command	000101
A64_Lock_command	000100
A64_BLT	000011
Reserved	000010
A64_single_transfer	000001
A64_64-bit_MBLT	000000

Table 5 – VME64Ful/Ltd Mode Symbol Table (cont'd.)

Signals, left-to-right: AM5, AM4, AM3, AM2, AM1, AM0

Symbol	Definition
	1111
BG3	0xxx
BG2	x0xx
BG1	xx0x
BG0	xxx0

Table 6- VME64Ful/Ltd BG Symbol Table
 Signals, left-to-right: BG3*, BG2*, BG1*, BG0*

Symbol	Definition
	1111111
IRQ7	0xxxxxx
IRQ6	x0xxxxx
IRQ5	xx0xxxx
IRQ4	xxx0xxx
IRQ3	xxxx0xx
IRQ2	xxxxx0x
IRQ1	xxxxxxx0

Table 7- VME64Ful (only) Interrupt Symbol Table
 Signals, left-to-right: IRQ7*, IRQ6*, IRQ5*, IRQ4*, IRQ3*, IRQ2*, IRQ1*

5.2 Viewing Timing Data on the TLA700

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: VME64Ful (or VME64Ltd) and VME64Ful: MagniVu (or VME64Ltd: MagniVu). The first (VME64Ful or VME64Ltd) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection, VME64Ful: MagniVu (or VME64Ltd: MagniVu), will show all of the channels in 2GHz or 8GHz MagniVu mode (depending upon the acquisition card used), so that edge relationships can be examined with very high resolution. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

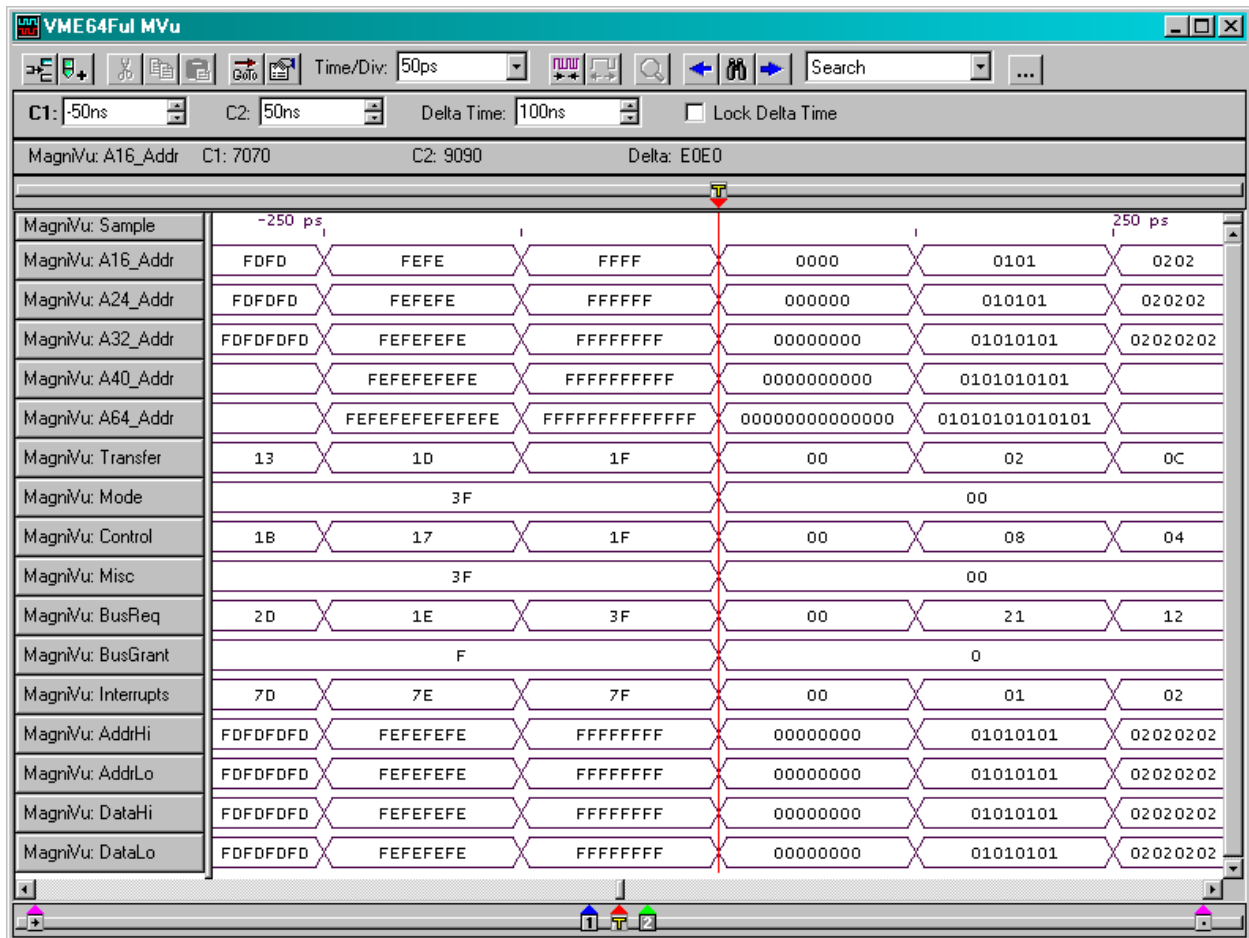


Figure 6- VME64Ful/Ltd MagniVu Display on TLA

APPENDIX A - How VME64 Data is Acquired

The VME64Ful and VME64Ltd support packages are designed to acquired data on all logic analyzer channels on the falling edges of AS*, DTACK*, BERR* and RETRY*.

APPENDIX B - Considerations

B.1 VME64X Bus Loading

It must be noted that the NEX-VME64X Bus Adapter does not provide any buffering of the VME64X signals and therefore violates the signal trace specification for the VME Bus. This was a conscious design decision that was made by balancing the tradeoffs of loading versus design simplicity and signal acquisition accuracy. By not introducing signal buffers it is possible, using this adapter, to see the exact timing relationships and signal waveforms from the system. However, it is entirely possible that, depending upon the design of the system being used, that operation of the target may be adversely affected by the use of the NEX-VME64X adapter.

APPENDIX C - NEX-VME64X Mictor Pinouts

Tek Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal	Tek Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal
3	5	CK0	P1.A18	AS	36	6	CK1	P1.A16	DTACK
4	7	A3:7	P2.B11	A31	35	8	A1:7	P1.C23	A15
5	9	A3:6	P2.B10	A30	34	10	A1:6	P1.C24	A14
6	11	A3:5	P2.B9	A29	33	12	A1:5	P1.C25	A13
7	13	A3:4	P2.B8	A28	32	14	A1:4	P1.C26	A12
8	15	A3:3	P2.B7	A27	31	16	A1:3	P1.C27	A11
9	17	A3:2	P2.B6	A26	30	18	A1:2	P1.C28	A10
10	19	A3:1	P2.B5	A25	29	20	A1:1	P1.C29	A9
11	21	A3:0	P2.B4	A24	28	22	A1:0	P1.C30	A8
12	23	A2:7	P1.C15	A23	27	24	A0:7	P1.A24	A7
13	25	A2:6	P1.C16	A22	26	26	A0:6	P1.A25	A6
14	27	A2:5	P1.C17	A21	25	28	A0:5	P1.A26	A5
15	29	A2:4	P1.C18	A20	24	30	A0:4	P1.A27	A4
16	31	A2:3	P1.C19	A19	23	32	A0:3	P1.A28	A3
17	33	A2:2	P1.C20	A18	22	34	A0:2	P1.A29	A2
18	35	A2:1	P1.C21	A17	21	36	A0:1	P1.A30	A1
19	37	A2:0	P1.C22	A16	20	38	A0:0	---	GND

Mictor Group A

Tek Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal	Tek Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal
3	5	CK3	P1.C11	BERR	36	6	Q1	P1.C12	SYSRESET
4	7	C3:7	P1.C14	AM5	35	8	C1:7	P1.B3	ACFAIL
5	9	C3:6	P1.A23	AM4	34	10	C1:6	P1.C10	SYSFAIL
6	11	C3:5	P1.B19	AM3	33	12	C1:5	P1.B22	SERB
7	13	C3:4	P1.B18	AM2	32	14	C1:4	P1.B21	SERA
8	15	C3:3	P1.B17	AM1	31	16	C1:3	P1.B11	BG3OUT
9	17	C3:2	P1.B16	AM0	30	18	C1:2	P1.B9	BG2OUT
10	19	C3:1	P1.B1	BBSY	29	20	C1:1	P1.B7	BG1OUT
11	21	C3:0	P1.B2	BCLR	28	22	C1:0	P1.B5	BG0OUT
12	23	C2:7	P1.A20	IACK	27	24	C0:7	P1.B10	BG3IN
13	25	C2:6	---	IRQx*	26	26	C0:6	P1.B8	BG2IN
14	27	C2:5	P1.A21	IACKIN	25	28	C0:5	P1.B6	BG1IN
15	29	C2:4	P1.A14	WRITE	24	30	C0:4	P1.B4	BG0IN
16	31	C2:3	P1.A22	IACKOUT	23	32	C0:3	P1.B15	BR3
17	33	C2:2	P1.A12	DS1	22	34	C0:2	P1.B14	BR2
18	35	C2:1	P1.A13	DS0	21	36	C0:1	P1.B13	BR1
19	37	C2:0	P1.C13	LWORD	20	38	C0:0	P1.B12	BR0

Mictor Group C

Tek Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal	Tek Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal
3	5	Q0	P1.A10	SYSCLK	36	6	CK2	P2.B3	RETRY
4	7	D3:7	P2.B30	D31	35	8	D1:7	P1.C8	D15
5	9	D3:6	P2.B29	D30	34	10	D1:6	P1.C7	D14
6	11	D3:5	P2.B28	D29	33	12	D1:5	P1.C6	D13
7	13	D3:4	P2.B27	D28	32	14	D1:4	P1.C5	D12
8	15	D3:3	P2.B26	D27	31	16	D1:3	P1.C4	D11
9	17	D3:2	P2.B25	D26	30	18	D1:2	P1.C3	D10
10	19	D3:1	P2.B24	D25	29	20	D1:1	P1.C2	D9
11	21	D3:0	P2.B23	D24	28	22	D1:0	P1.C1	D8
12	23	D2:7	P2.B21	D23	27	24	D0:7	P1.A8	D7
13	25	D2:6	P2.B20	D22	26	26	D0:6	P1.A7	D6
14	27	D2:5	P2.B19	D21	25	28	D0:5	P1.A6	D5
15	29	D2:4	P2.B18	D20	24	30	D0:4	P1.A5	D4
16	31	D2:3	P2.B17	D19	23	32	D0:3	P1.A4	D3
17	33	D2:2	P2.B16	D18	22	34	D0:2	P1.A3	D2
18	35	D2:1	P2.B15	D17	21	36	D0:1	P1.A2	D1
19	37	D2:0	P2.B14	D16	20	38	D0:0	P1.A1	D0

Mictor Group D

Tek Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal	Mictor Pin #	Amp Mictor Pin #	TLA Channel	VME64X Pin #	VME64X Signal
3	5	Q3	---	---	36	6	Q2	---	---
4	7	E3:7	---	---	35	8	E1:7	---	---
5	9	E3:6	---	---	34	10	E1:6	---	---
6	11	E3:5	---	---	33	12	E1:5	---	---
7	13	E3:4	---	---	32	14	E1:4	---	---
8	15	E3:3	---	---	31	16	E1:3	---	---
9	17	E3:2	---	---	30	18	E1:2	---	---
10	19	E3:1	---	---	29	20	E1:1	---	---
11	21	E3:0	---	---	28	22	E1:0	---	---
12	23	E2:7	---	---	27	24	E0:7	---	---
13	25	E2:6	---	---	26	26	E0:6	P1.B24	IRQ7
14	27	E2:5	---	---	25	28	E0:5	P1.B25	IRQ6
15	29	E2:4	---	---	24	30	E0:4	P1.B26	IRQ5
16	31	E2:3	---	---	23	32	E0:3	P1.B27	IRQ4
17	33	E2:2	---	---	22	34	E0:2	P1.B28	IRQ3
18	35	E2:1	---	---	21	36	E0:1	P1.B29	IRQ2
19	37	E2:0	---	---	20	38	E0:0	P1.B30	IRQ1

Mictor Group E

APPENDIX E - References

Tektronix TLA700 System User's Manual

Tektronix TLA700 Logic Analyzer User's Manual

P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual
Tektronix part number 071-1059-00

Tektronix P6434 Mass Termination Probe Manual
070-9793-02

VMEbus Specification
Revision C.1, October 1985

American National Standard for VME64
ANSI/VITA 1-1994

American National Standard for VME64 Extensions
ANSI/VITA 1.1-1997

APPENDIX F - Support

About Nexus Technology, Inc.



Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Support Contact Information

Technical Support	techsupport@nexustechnology.com
General Information	support@nexustechnology.com
Quote Requests	quotes@nexustechnology.com

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.