Nexus DDR3 Sample Point Analyzer

Synopsis

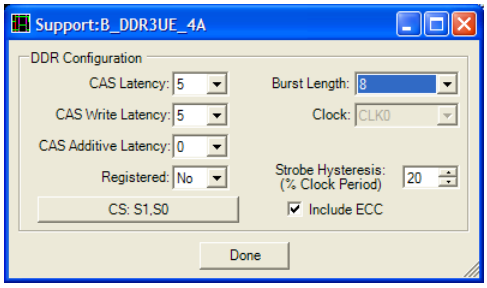
Nexus Technology's DDR3 Sample Point Analyzer (SPA) facilitates configuring a Tektronix Logic Analyzer (TLA) to acquire and decode memory exchanges for a DDR3 or DDR2 target. The DDR3 SPA automatically recognizes a Nexus Technology support is loaded on TLA modules and allows retrieval and analysis of MagniVu® data to tune the configuration to the target that is attached.

To reliably acquire data from a DDR target, variations in voltage and timing must be taken into account. The threshold, which controls the digitization of the data signals on the bus, and the sample point, which determines when data is valid, must both be adjusted for the target to optimize acquiring correct data.

In addition to these parameters, the DDR3 SPA is also able to account for some other conditions that affect analysis. This often allows determination of correct settings, even when conditions are not ideal.

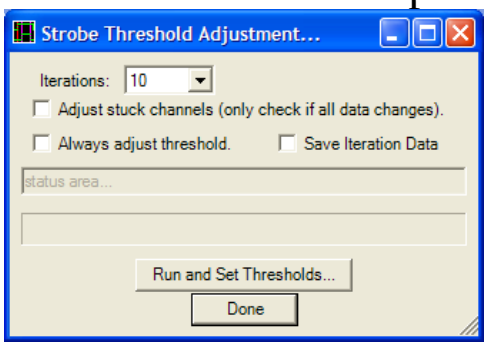
Configuration Information

Configuration parameters must be known for the given target. The minimum parameters required are CAS (read) Latency, CAS Write Latency, CAS Additive Latency, Burst Length and DIMM type (registered or unbuffered). The latency and burst length parameters can be determined by capturing a Mode Register Set (MRS) operation. Additionally, the DDR3 SPA needs to know the type of DIMM that the target uses, unbuffered (UDIMM) or registered (RDIMM). These settings are shown below.

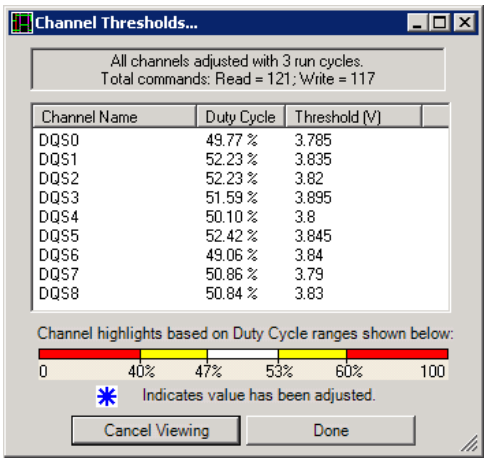


Logic Analyzer Threshold Adjustments

The first tuning that should be done to optimize acquiring data from a DDR3 target is tuning thresholds for strobe (DQS) and data (DQ) channels, in that order. As DDR speeds increase, the analog nature of the bus signals becomes significant. Tuning thresholds helps insure the accuracy of the digitized data. The DDR3 SPA provides automation of threshold setting for both DQS and DQ signals. The DDR3 SPA analyzes the current acquisition, adjusts the thresholds appropriately and re-acquires data to re-evaluate the threshold effectiveness. The main window for the strobe threshold tuning is shown below.

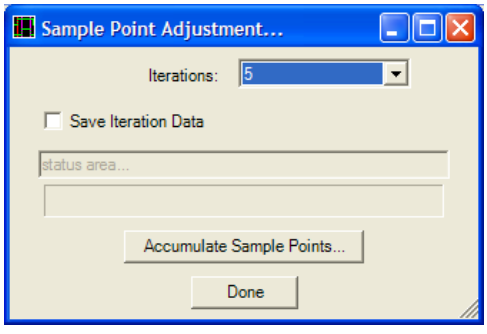


The result window is shown below. Any channels that need further adjustment or are marginal, based on the DDR3 specification, would be highlighted in the appropriate color.

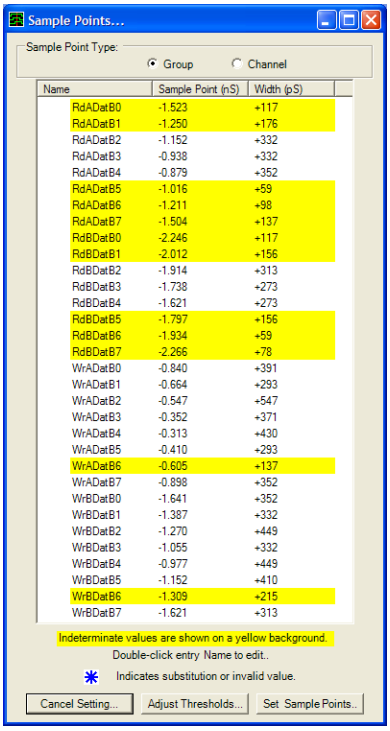


Logic Analyzer Sample Point Adjustment

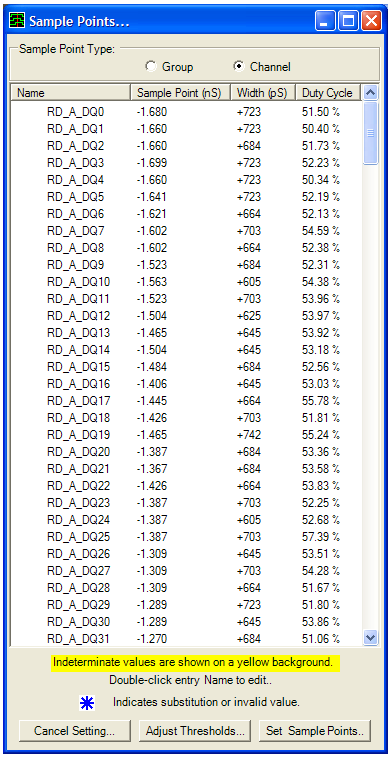
The next step in proper configuration is sample point determination. This aligns the acquisition system to the target, which helps to insure that data is being sampled at the correct location. The DDR3 SPA allows determination from a single acquisition or the ability to tune the sample points over multiple acquisitions when the target has timing variations that affect the phase of the data. The main window for multiple-acquisition sample point determination is shown below.



The result window is shown below.

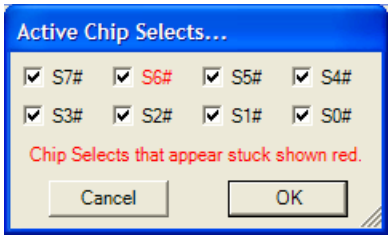


The values highlighted in yellow indicate that the group values do not have sufficient data eye width. Under these conditions, individual channel values should be used. An example of channel value results is shown below.



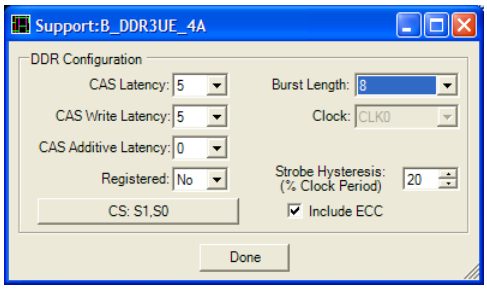
Additional Features

As mentioned earlier, the DDR3 SPA also has provision to account for other conditions that affect analysis of data. Some of these features are handling "stuck" chip select (CS) channels, handling glitches on strobe channels and specifying if ECC signals are used on the target.
When the analysis of the current acquisition indicates that a given CS signal is always active, the DDR3 SPA will alert the user with the alert window shown below.



To correct for these CS signals, simply uncheck the stuck chip selects to exclude them from analysis.

Glitches on strobe channels can affect the analysis of an acquisition. In cases where glitches appear on strobe channels, the DDR3 SPA can ignore transitions close together, so a determination of sample points may still be possible. The adjustment of the tolerance of strobe glitches (Strobe Hysteresis) is shown below.



This window also shows the check box that allows exclusion of ECC analysis, when the target does not utilize ECC signals.

Summary

The DDR3 SPA provides a number of easy to use features that assist in configuration and tuning of the TLA to facilitate reliable acquisition of DDR3 data from the target.