

Applications Note

Using the SODIMMDDRII667/800 NEXVu product – a step by step overview with Signal Integrity Display

Introduction

The SODIMMDDRIINEXVu667/800 is an instrumented NEXVu SODIMM that provides high quality measurements at the DDR2 memory pads. The NEXVu has minimum impact on the signal integrity of the signals between the memory controller and the DDR2 SDRAMs*. The logic analyzer probes attached to the NEXVu provide probing for both the logic analyzer and the oscilloscope using the iCapture and iView capabilities of the Tektronix TLA7Ax4 logic analyzer acquisition cards. SODIMMDDRIINEXVu667/800 software decodes the DDR2 commands and shows them in the logic analyzer Listing Window with the DDR2 data.

* Please refer to the Nexus Technology White paper available online for additional information on the benefits of the NEXVu design:

http://www.nexustechnology.com/products/memory/ddrii/DDRIICaptureAbove400 Whitepaper.pdf

Connecting to the Target

The SODIMMDDRIINEXVu667/800 NEXVu has eight probe connections on the front for easy attachment of Tektronix P68xx series logic analyzer probes. These probe connections are also duplicated on the back of the NEXVu so that the eight probes can be attached to either the front or the back of the NEXVu for mechanical clearance in a target. Figures 1 and 2 below show a NEXVu with eight P68xx probes on the back side of the NEXVu installed in a laptop target.

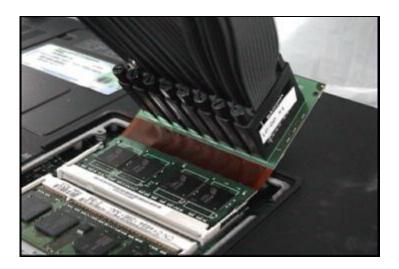


Figure 1: SODIMMDDRIINEXVu in a laptop



Figure 2: SODIMMDDRIINEXVu in a laptop

Logic Analyzer Acquisition

The logic analyzer captures 125ps high-resolution timing waveforms with MagniVu. It also has the ability to acquire state data at the DDR2 667 and 800 SDRAM data rates. All acquisitions and traces in Figures 3 through 14 and are from a DDR2 667 NEXVu SODIMM.

State Acquisition

Figure 3 is a logic analyzer Listing window of state acquisitions from a DDR2 667 target showing an MRS cycle. Figure 4 shows a Read transaction and figure 5 shows a Write transaction.

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C1: SDI	4 DR2-2K	C2: SD	7 🗧 Delta Time: 42.7377s 🔮 DR2-2K	☐ Loc	:k Delta Time	•		
	Sample	SDDR 2-2K Address	SDDR2-2K Mnemonics	SDDR2-2K DataHi	SDDR2-2K DataLo	SDDR2-2K DataMasks	Timestamp	
		04040 04040	Output Buffer: Enabled RDOS Enable: No				3	
		04040	DOS# Enable: Enable					
		04040	OCD Operation: OCD calibration mode exit					
		04040	Rtt: 150 ohm					
		04040 04040	Additive Latency: 0 Output Drive Strength: 100%					
		04040	Output Drive Strength: 100% DLL Enable: Enable (Normal)					
	3	0085B	MRS - MODE REGISTER SET (SO#)				241.966,000 us	
	153	0085B	Normal MRS		00000000		10.455562550.05255354255	
		0085B 0085B	PD Mode: Standard Write Recovery: 5					and a
		0085B	BLL Reset: No					
		0085B	Operating Mode: Normal					
		0085B	Latency: 5					
		0085B	Burst Type: Interleaved					
	4	0085B 0085B	Burst: 8 MRS - MODE REGISTER SET (SO#)				170 105 250	
	4	0085B	Normal MRS				139.185,250 us	
		0085B	PD Mode: Standard					
		0085B	Write Recovery: 5					
		0085B	DLL Reset: No					
		0085B 0085B	Operating Mode: Normal Latency: 5					
		0085B	Burst Type: Interleaved					
	0.00	0085B	Burst Ťype: Interleaved Burst: 8				MALCONALCONSEN.	1
	5	042C0	MRS - MODE REGISTER SET (SO#)				93.545,750 us	
		042C0	Extended MRS					
		042C0 042C0	Output Buffer: Enabled RDOS Enable: No					
		04200	DQS# Enable: Enable					
		042C0	OCD Operation: Undefined					
		042C0	Rtt: 150 ohm					
		042C0 042C0	Additive Latency: 0 Output Drive Strength: 100%					
		04200	DLL Enable: Enable (Normal)					
7)	6	04040	MRS - MODE REGISTER SET (SO#)				28.304.125 us	
The second	(7,7)	04040	Extended MRS					
		04040	Output Buffer: Enabled					457
		04040	RDQS Enable: No DOS# Enable: Enable					
		04040 04040	OCD Operation: OCD calibration mode exit					
		04040	Rtt: 150 ohm					
		04040	Additive Latency: 0					
		04040	Output Drive Strength: 100%					
	2253	04040	DLL Enable: Enable (Normal)					
7	7	00082	(UNKNOWN)	00000000	00000000	.00	42.737,626,527,625 s	-
	•			,	5	·		

Figure 3: Listing window of Mode Register and Extended Mode Register configuration cycles captured by the NEXVu and the logic analyzer. Normal Mode Register shows DDR2 667 SDRAM being configured for burst length of 8 and CAS latency of 5 cycles. Extended Mode Register is configured with Additive Latency of 0.

Sample	SDDR 2-2K Address	SDDR2-2K Mnemonics	SODR 2-2K DataHi	SDDR 2-2K DataLo	SODR 2-2K DataMasks	Timestamp	4
2045		DESL - IGNORE COMMAND				3.000 ns	-
2046		DESL - IGNORE COMMAND				3.000 ns	
2047	04800	READ - COL ADDR READ (SO#)				3.000 ns	
2048		DESL - IGNORE COMMAND				3.000 ns	
2049		DESL - IGNORE COMMAND				3.000 ns	
2050		DESL - IGNORE COMMAND				3.000 ns	
2051		DESL - IGNORE COMMAND				3.125 ns	
2052		READ DATA	4949C6F0	34526810		2.875 ns	
		READ DATA	33B9724B	8C0B3CD8			
2053		READ DATA	51908590	00081466		3.000 ns	
		READ DATA	088200C2	A654681D			
2054		READ DATA	010C7243	FF82005C		3.000 ns	
		READ DATA	000000A7	B3193666		Contract Contract Contract	
2055		READ DATA	2900A900	001028FA		3.125 ns	
		READ DATA	5A95A592	68C928EB			
2056		DESL - IGNORE COMMAND				2.875 ns	
2057		DESL - IGNORE COMMAND				3.000 ns	
2058		DESL - IGNORE COMMAND				3.000 ns	
2059		DESL - IGNORE COMMAND				3.125 ns	
2060		DESL - IGNORE COMMAND				2.875 ns	
2061		DESL - IGNORE COMMAND				3.125 ns	
2062		DESL - IGNORE COMMAND				2.875 ns	
2063		DESL - IGNORE COMMAND				3.125 ns	
2064		DESL - IGNORE COMMAND				3.000 ns	
2065		DESL - IGNORE COMMAND				3.000 ns	18

Figure 4: Listing window showing triggering on DDR2 SDRAM Read command with a burst length of 8 for the Read data. This Read data is also shown in timing waveforms in Figure 7. The logic analyzer verifies the Read CAS latency is 5 cycles. The logic analyzer is configured to acquiring every DDR2 clock cycle including the Deselect states.

Sample	SDDR 2-2K Address	SDDR 2-2K Mnemonics	SDDR2-2K DataHi	SDDR2-2K DataLo	SDDR2-2K DataMasks	Timestamp		
2046		DESL - IGNORE COMMAND				3.000		1
2047	OCAD8	WRITE - COL ADDR WRITE (SO#)				3.000	ns	
2048		DESL - IGNORE COMMAND				3.000	ns	1
2049		DESL - IGNORE COMMAND				3.000		
2050		DESL - IGNORE COMMAND				3.000	ns	£
2051		WRITE DATA	00000000	00000000	00	3.125	ns	
		WRITE DATA	99460000	00CE7E43	00	1.000	600.80	
2052		WRITE DATA	CA271000	028E00BE	00	3.000	ns	
		WRITE DATA	000000000	000000000	00			
2053		WRITE DATA	96A5A500	78855A69	00	2.875	ns	
		WRITE DATA	96A5A55A	78855A69	00		10.00	
2054		WRITE DATA	96A5A500	78855A69	00	3.000	ins	-
		WRITE DATA	96A5A55A	78855A69	00			
2055		DESL - IGNORE COMMAND				3.129	ns	
2056		DESL - IGNORE COMMAND				3.000		
2057		DESL - IGNORE COMMAND				3.000		
2058	04004	PRE - PRECHARGE SELECT BANK (SO#)				3.000		
2059		DESL - IGNORE COMMAND				3.000		
2060		DESL - IGNORE COMMAND				3.000		
2061		DESL - IGNORE COMMAND				3.000		
2062		DESL - IGNORE COMMAND				3.000		
2063		DESL - IGNORE COMMAND				3,000		
2064		DESL - IGNORE COMMAND				3.125		
2065		DESL - IGNORE COMMAND				2.875		
2066		DESL - IGNORE COMMAND				3.000		1

Figure 5: Listing window showing triggering on DDR2 SDRAM Write command with a burst length of 8 for the Write data. This data is also shown in timing waveforms in Figure 9. The logic analyzer verifies the Write CAS latency is 4 cycles, which is one less then the 5 cycles for Read. Notice the Precharge command is closing out the open row after the Write data and is preparing the memory for a future Refresh or Activate command.

Asynchronous Acquisition (Timing acquisition)

The MagniVu 125ps high-resolution timing acquisition capability of the TLA7Ax4 cards provides excellent logic analyzer timing analysis of the DDR2 667 SDRAM bus. The TLA7Ax4 provides simultaneous high-resolution timing acquisition with state acquisition through one logic analyzer probe. The Figures 6 through 9 are Read and Write commands with their associated data as seen by the TLA7Ax4's 125ps MagniVu acquisition capability.

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	Goto Time/I	Div: 2ns 💌 🐺	¥ Q +	🕅 🔶 Sear	rch	·		
C1: 15.13ns 🚊	C2: 16.51ns	Delta Time: 1.38ns	<u>н</u> Г	ock Delta Time				
MagniVu: A_DatLo 0	C1: 3452681D	C2: 8C0B3CD8	Delta: B859	54C5				
	Ţ			1	1 <u></u>			
MagniVu: Address				04800				•
MagniVu: Misc(0)	يحد وي من	لككر وركلا ور		للكري	1	مد وي ک		يسر
MagniVu: Control	25			20				
MagniVu: Command	05			00				
MagniVu: A_DatHi		00000000		X				
MagniVu: A_DatLo		0000000		X	X		CKX	
MagniVu: RDDatBy7		00		X	49	51 08	01 00 29	SA
MagniVu: RDDatBy6		00			49 B	9 90 82	00 00	95
MagniVu: RDDatBy5		00			6 72	85 00	72 00 A9	AS
MagniVu: RDDatBy4		00		X	F0 48	90 C2	43 A7 00	92
MagniVu: RDDatBy3		00		X	34 (8C	OC A6	FF B3 00	68
MagniVu: RDDatBy2		00		X	52 0B	08 54	82 19 10	Co
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Figure 6: The second waveform from the top is the DDR2 SDRAM clock. The bottom bus form waveforms show the double data rate of the Read data compared to the DDR2 SDRAM clock.

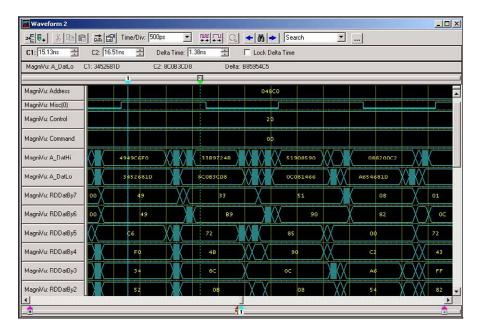


Figure 7: Zoomed in view of the Read data shown in Figure 6. MagniVu: A_DatHi is the upper 32-bits (8 hex digits) of Read data and MagniVu: A_DatLo is the lower 32-bits (8 hex digits) of Read data.

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C1: 10.8ns	C2: 12	2ns	÷	Delta Ti	me: 1	.4ns	*	Lock)elta Time						
MagniVu: A_DatLo	C1: 000000	000	0	:2: 000A	7E02		Delta	000A7E02							
		Ţ_						1	And the second						
MagniVu: Sample	-2.875 m	\$	manna	miranni					mmminn		mannin				24.875 ns
MagniVu: Address		ADS	X					04014				X	04A	90	
MagniVu: Misc(0)				ي ال				اريور							ي الك
MagniVu: Control	7C 🗙	74		7B	Х	6B	X		7B			70	60	_X_	70
MagniVu: Command	10	14		18	χ	ов	X		18			10	00	X	10
MagniVu: A_DatHi				B76FE	E00					DX	X	XX	\mathbf{X}	964	45A55A
MagniVu: A_DatLo				78423	49F				X	X		1	7885	5A69	

Figure 8: The top MagniVu Sample waveform shows the 125ps high-resolution timing ticks for the waveform display window.

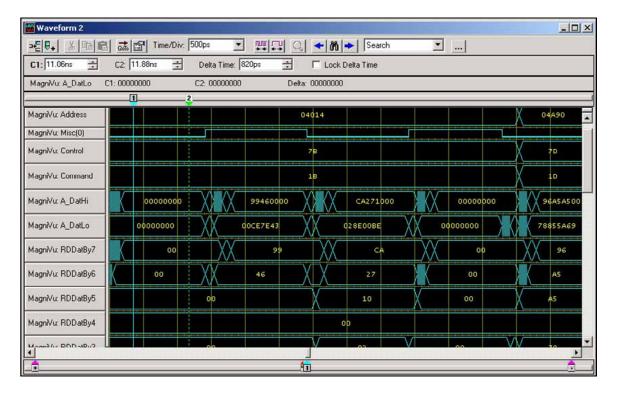


Figure 9: Zoom in display of the waveform data shown in Figure 8. Timing display of Write command using MagniVu 125ps high-resolution timing acquisition.

Signal Integrity

Nexus Technology's unique NEXVu design provides an interface that in minimally intrusive on the target and presents excellent signal fidelity to the Tektronix TLA logic analyzer for acquisition. The adapter must preserve the signal integrity of the target to allow the target to function properly and to present the DDR2 signals realistically to the TLA. The following oscilloscope waveforms are the DDR2 SDRAM Clock, Strobe, S0, Address and Data. Notice the excellent signal characteristics. These traces were captured using the Tektronix TLA's iCapture and iView capability which makes analog viewing easy for any signal probed by the TLA7Ax logic analyzer ascquisition card. iCapture and iView eliminate the need to double probe signals with an oscilloscope probe.

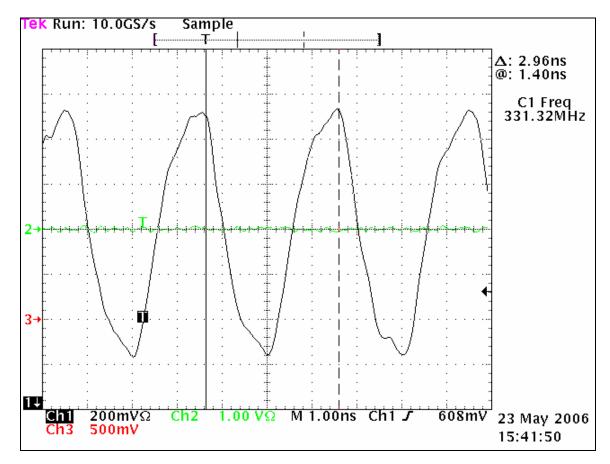


Figure 10: Oscilloscope waveform of the DDR2 667 SDRAM clock signal using the TLA7AA4 logic analyzer probing.

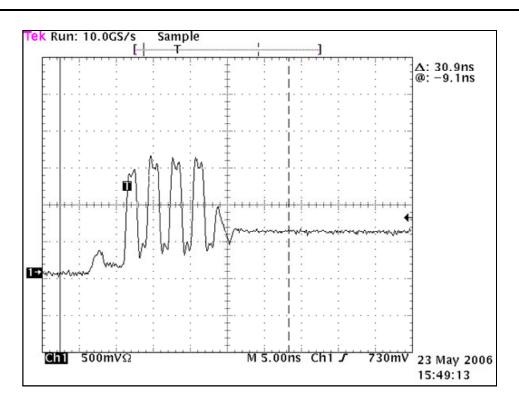


Figure 11: Oscilloscope waveform of the DDR2 667 SDRAM strobe signal using the TLA7AA4 logic analyzer probing. Notice the 8 strobe edges reflecting the burst length of 8.

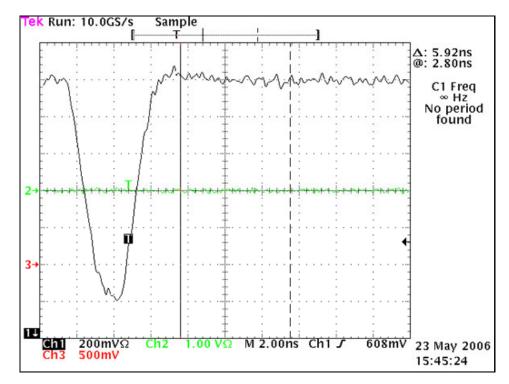


Figure 12: Oscilloscope waveform of the SODIMM S0 signal using the TLA7AA4 logic analyzer probing.

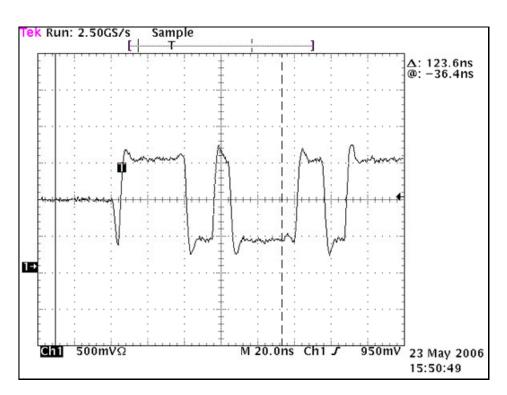


Figure 13: Oscilloscope waveform of the DDR2 667 SDRAM address signal using the TLA7AA4 logic analyzer probing.

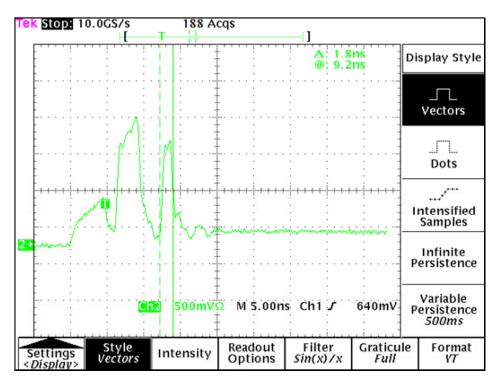


Figure 14: Oscilloscope waveform of the DDR2 667 SDRAM data signal using the TLA7AA4 logic analyzer probing.

More Information

All acquisition data was taken using a laptop with DDR2 667 SDRAM plugged into an SODIMMDDRIINEXVu.

SODIMMDDRIINEXVu specific information including a downloadable datasheet and manual can be obtained at: <u>http://www.nexustechnology.com/products/memory/ddrii/sodimmddrii800nexvu/</u>

For more information on Nexus products please visit <u>www.nexustechnology.com</u>.

Questions regarding this Applications Note or the NEX-SODIMMDDRII667/800NEXVu product should be directed to Nexus Technology at support@nexustechnology.com or 877-595-8116.