NEXUS TECHNOLOGY

Applications Note

Using the SODIMMDDRII667/800 NEXVu product – a step by step overview with Signal Integrity Display

Introduction

The SODIMMDDRIINEXVu667/800 is an instrumented NEXVu SODIMM that provides high quality measurements at the DDR2 memory pads. The NEXVu has minimum impact on the signal integrity of the signals between the memory controller and the DDR2 SDRAMs*. The logic analyzer probes attached to the NEXVu provide probing for both the logic analyzer and the oscilloscope using the iCapture and iView capabilities of the Tektronix TLA7Ax4 logic analyzer acquisition cards. SODIMMDDRIINEXVu667/800 software decodes the DDR2 commands and shows them in the logic analyzer Listing Window with the DDR2 data.

* Please refer to the Nexus Technology White paper available online for additional information on the benefits of the NEXVu design:

http://www.nexustechnology.com/products/memory/ddrii/DDRIICaptureAbove400_Whitepaper.pdf

Connecting to the Target

The SODIMMDDRIINEXVu667/800 NEXVu has eight probe connections on the front for easy attachment of Tektronix P68xx series logic analyzer probes. These probe connections are also duplicated on the back of the NEXVu so that the eight probes can be attached to either the front or the back of the NEXVu for mechanical clearance in a target. Figures 1 and 2 below show a NEXVu with eight P68xx probes on the back side of the NEXVu installed in a laptop target.

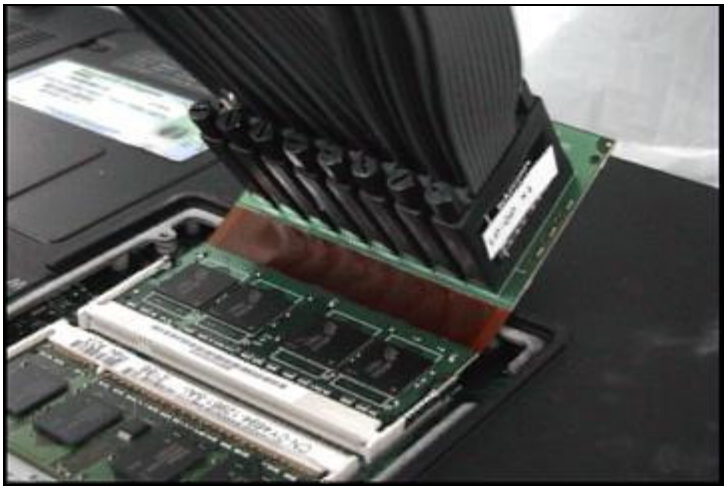


Figure 1: SODIMMDDRIINEXVu in a laptop

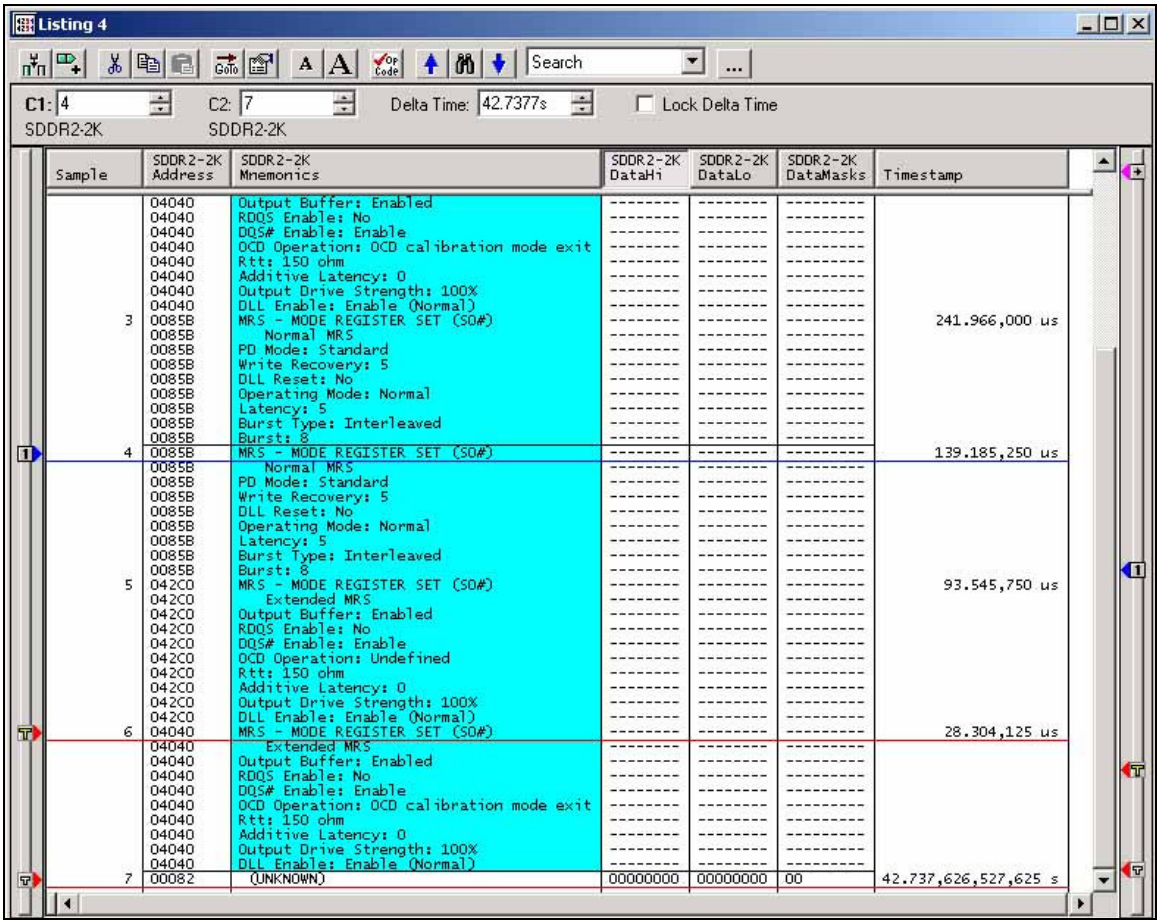
Figure 2: SODIMMDDRIINEXVu in a laptop

Logic Analyzer Acquisition

The logic analyzer captures 125ps high-resolution timing waveforms with MagniVu. It also has the ability to acquire state data at the DDR2 667 and 800 SDRAM data rates. All acquisitions and traces in Figures 3 through 14 and are from a DDR2 667 NEXVu SODIMM.

State Acquisition

Figure 3 is a logic analyzer Listing window of state acquisitions from a DDR2 667 target showing an MRS cycle. Figure 4 shows a Read transaction and figure 5 shows a Write transaction.



Sample	SDDR2-2K Address	SDDR2-2K Mnemonics	SDDR2-2K DataHi	SDDR2-2K DataLo	SDDR2-2K DataMasks	Timestamp
	04040	Output Buffer: Enabled	--------	--------	--------	
	04040	RDQS Enable: No	--------	--------	--------	
	04040	DQS# Enable: Enable	--------	--------	--------	
	04040	OCD Operation: OCD calibration mode exit	--------	--------	--------	
	04040	Rtt: 150 ohm	--------	--------	--------	
	04040	Additive Latency: 0	--------	--------	--------	
	04040	Output Drive Strength: 100%	--------	--------	--------	
	04040	DLL Enable: Enable (Normal)	--------	--------	--------	
3	0085B	MRS - MODE REGISTER SET (SO#)	--------	--------	--------	241.966,000 us
	0085B	Normal MRS	--------	--------	--------	
	0085B	PD Mode: Standard	--------	--------	--------	
	0085B	Write Recovery: 5	--------	--------	--------	
	0085B	DLL Reset: No	--------	--------	--------	
	0085B	Operating Mode: Normal	--------	--------	--------	
	0085B	Latency: 5	--------	--------	--------	
	0085B	Burst Type: Interleaved	--------	--------	--------	
	0085B	Burst: 8	--------	--------	--------	
4	0085B	MRS - MODE REGISTER SET (SO#)	--------	--------	--------	139.185,250 us
	0085B	Normal MRS	--------	--------	--------	
	0085B	PD Mode: Standard	--------	--------	--------	
	0085B	Write Recovery: 5	--------	--------	--------	
	0085B	DLL Reset: No	--------	--------	--------	
	0085B	Operating Mode: Normal	--------	--------	--------	
	0085B	Latency: 5	--------	--------	--------	
	0085B	Burst Type: Interleaved	--------	--------	--------	
	0085B	Burst: 8	--------	--------	--------	
5	042C0	MRS - MODE REGISTER SET (SO#)	--------	--------	--------	93.545,750 us
	042C0	Extended MRS	--------	--------	--------	
	042C0	Output Buffer: Enabled	--------	--------	--------	
	042C0	RDQS Enable: No	--------	--------	--------	
	042C0	DQS# Enable: Enable	--------	--------	--------	
	042C0	OCD Operation: Undefined	--------	--------	--------	
	042C0	Rtt: 150 ohm	--------	--------	--------	
	042C0	Additive Latency: 0	--------	--------	--------	
	042C0	Output Drive Strength: 100%	--------	--------	--------	
	042C0	DLL Enable: Enable (Normal)	--------	--------	--------	
6	04040	MRS - MODE REGISTER SET (SO#)	--------	--------	--------	28.304,125 us
	04040	Extended MRS	--------	--------	--------	
	04040	Output Buffer: Enabled	--------	--------	--------	
	04040	RDQS Enable: No	--------	--------	--------	
	04040	DQS# Enable: Enable	--------	--------	--------	
	04040	OCD Operation: OCD calibration mode exit	--------	--------	--------	
	04040	Rtt: 150 ohm	--------	--------	--------	
	04040	Additive Latency: 0	--------	--------	--------	
	04040	Output Drive Strength: 100%	--------	--------	--------	
	04040	DLL Enable: Enable (Normal)	--------	--------	--------	
7	00082	(UNKNOWN)	00000000	00000000	00	42.737,626,527,625 s

Figure 3: Listing window of Mode Register and Extended Mode Register configuration cycles captured by the NEXVu and the logic analyzer. Normal Mode Register shows DDR2 667 SDRAM being configured for burst length of 8 and CAS latency of 5 cycles. Extended Mode Register is configured with Additive Latency of 0.

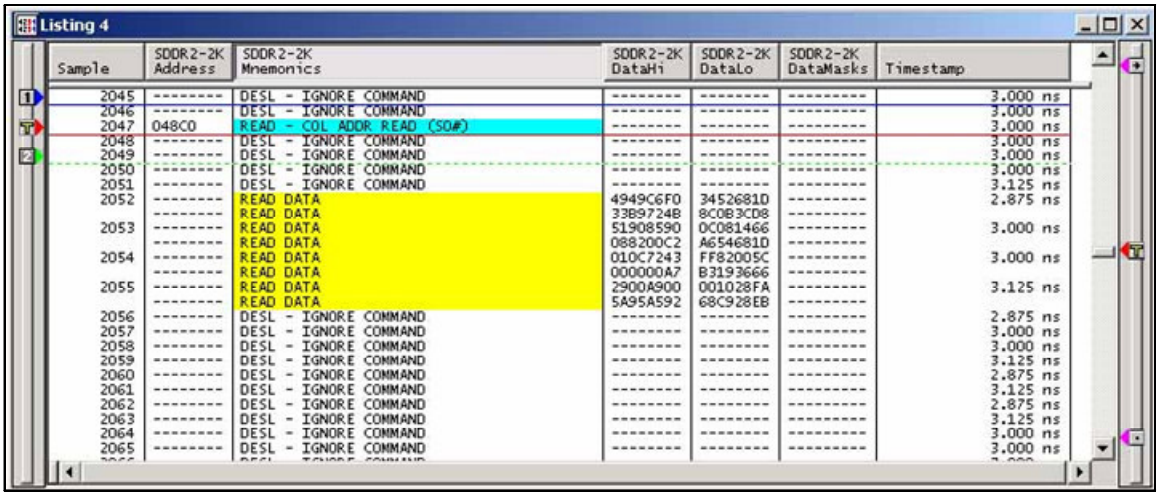


Figure 4: Listing window showing triggering on DDR2 SDRAM Read command with a burst length of 8 for the Read data. This Read data is also shown in timing waveforms in Figure 7. The logic analyzer verifies the Read CAS latency is 5 cycles. The logic analyzer is configured to acquiring every DDR2 clock cycle including the Deselect states.

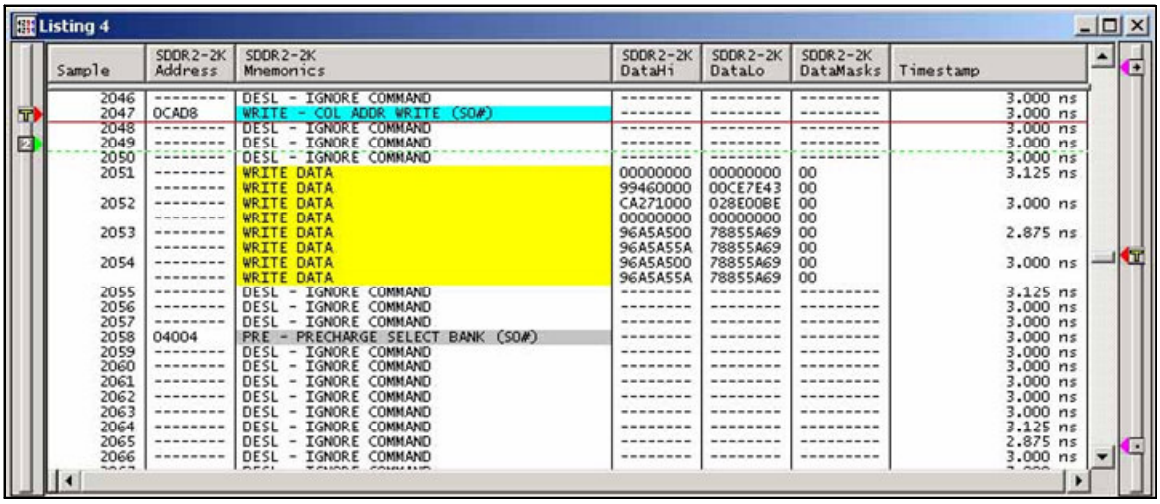


Figure 5: Listing window showing triggering on DDR2 SDRAM Write command with a burst length of 8 for the Write data. This data is also shown in timing waveforms in Figure 9. The logic analyzer verifies the Write CAS latency is 4 cycles, which is one less then the 5 cycles for Read. Notice the Precharge command is closing out the open row after the Write data and is preparing the memory for a future Refresh or Activate command.

Asynchronous Acquisition (Timing acquisition)

The MagniVu 125ps high-resolution timing acquisition capability of the TLA7Ax4 cards provides excellent logic analyzer timing analysis of the DDR2 667 SDRAM bus. The TLA7Ax4 provides simultaneous high-resolution timing acquisition with state acquisition through one logic analyzer probe. The Figures 6 through 9 are Read and Write commands with their associated data as seen by the TLA7Ax4's 125ps MagniVu acquisition capability.

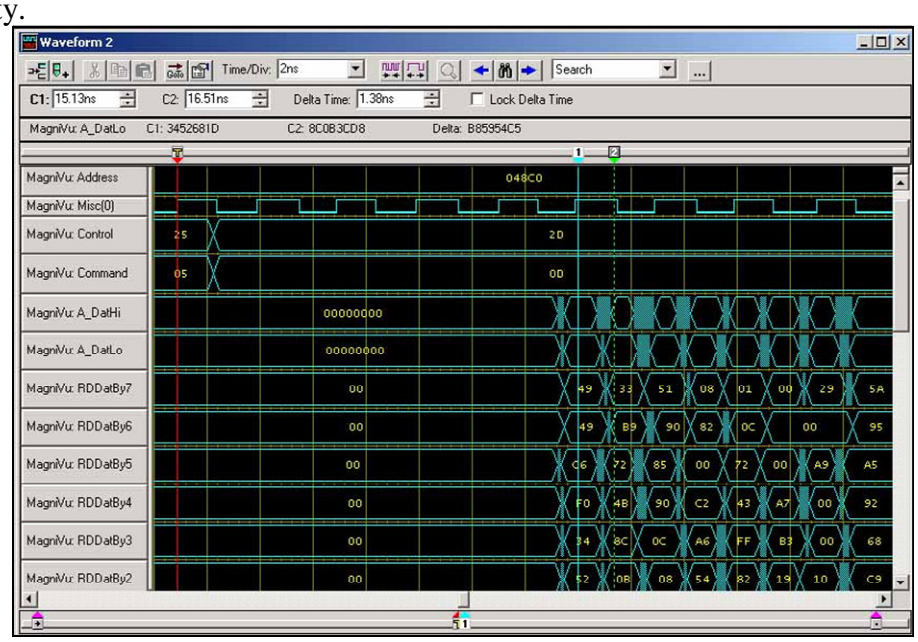


Figure 6: The second waveform from the top is the DDR2 SDRAM clock. The bottom bus form waveforms show the double data rate of the Read data compared to the DDR2 SDRAM clock.

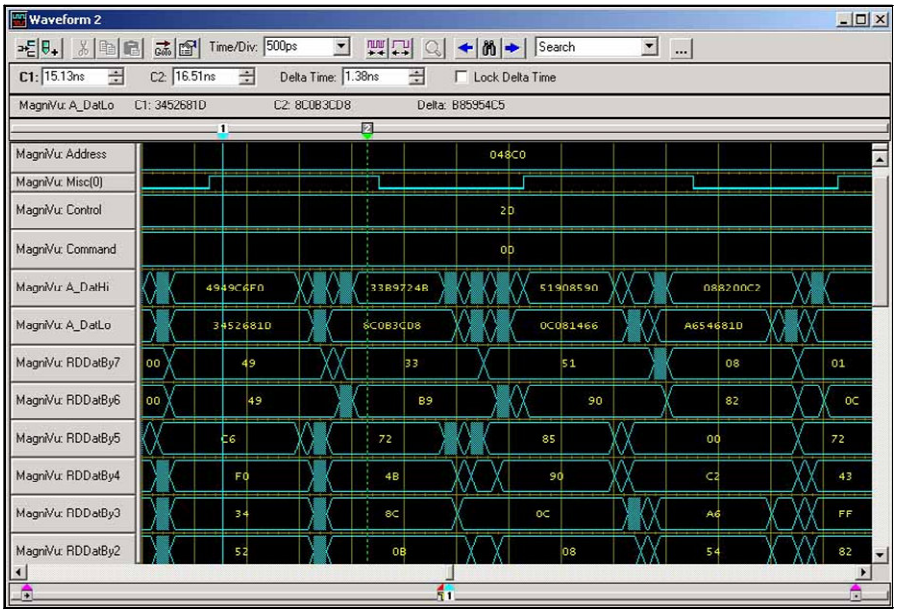


Figure 7: Zoomed in view of the Read data shown in Figure 6.
MagniVu: A_DatHi is the upper 32-bits (8 hex digits) of Read data and
MagniVu: A_DatLo is the lower 32-bits (8 hex digits) of Read data.

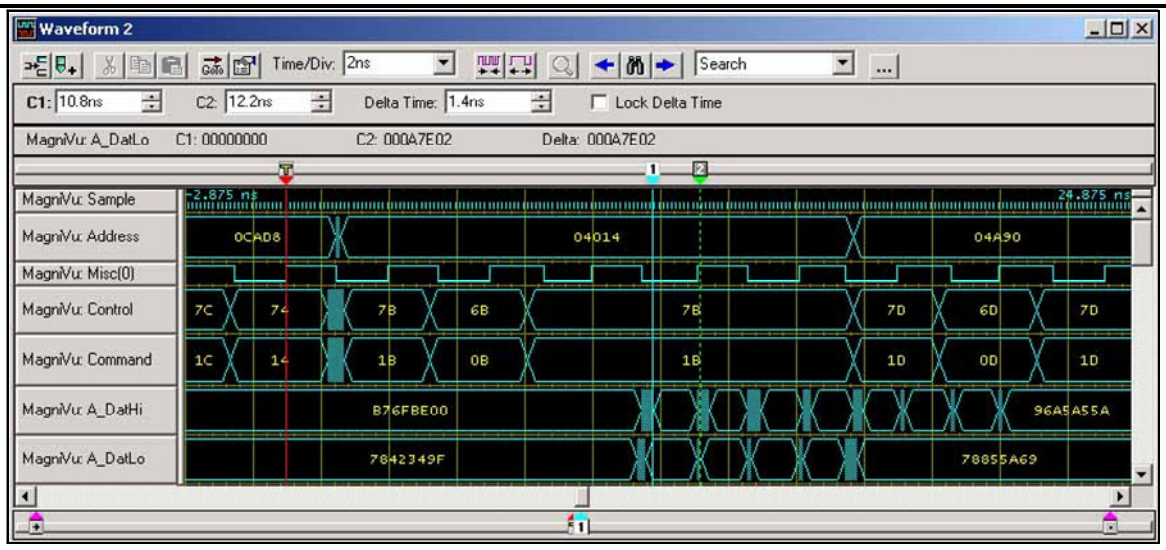


Figure 8: The top MagniVu Sample waveform shows the 125ps high-resolution timing ticks for the waveform display window.

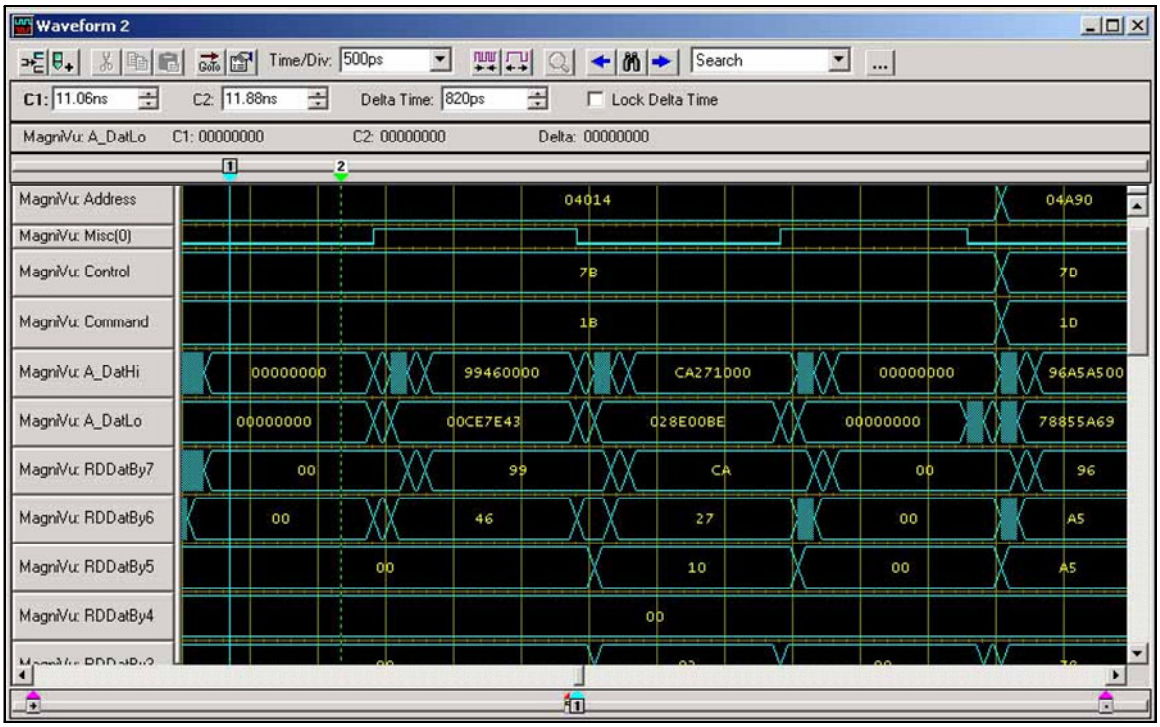


Figure 9: Zoom in display of the waveform data shown in Figure 8. Timing display of Write command using MagniVu 125ps high-resolution timing acquisition.

Signal Integrity

Nexus Technology's unique NEXVu design provides an interface that in minimally intrusive on the target and presents excellent signal fidelity to the Tektronix TLA logic analyzer for acquisition. The adapter must preserve the signal integrity of the target to allow the target to function properly and to present the DDR2 signals realistically to the TLA. The following oscilloscope waveforms are the DDR2 SDRAM Clock, Strobe, S0, Address and Data. Notice the excellent signal characteristics. These traces were captured using the Tektronix TLA's iCapture and iView capability which makes analog viewing easy for any signal probed by the TLA7Ax logic analyzer ascquisition card. iCapture and iView eliminate the need to double probe signals with an oscilloscope probe.

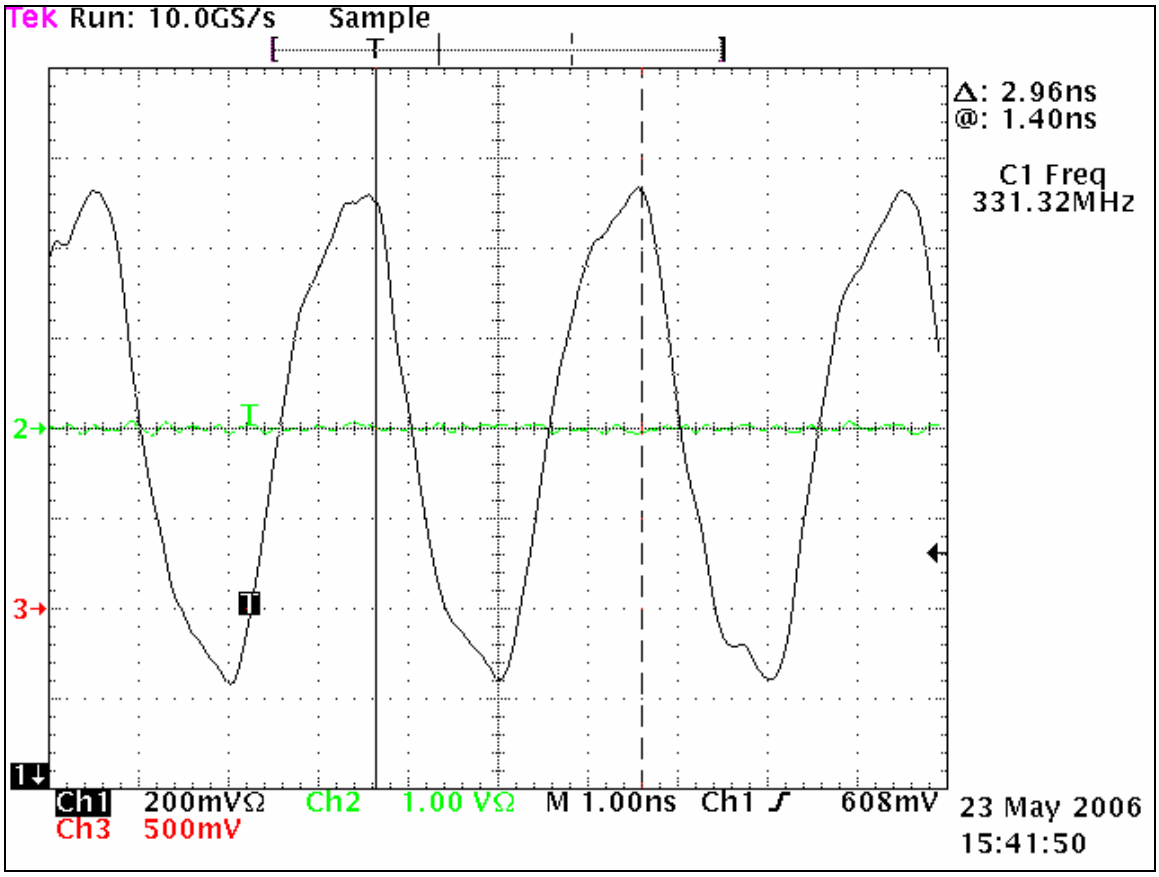


Figure 10: Oscilloscope waveform of the DDR2 667 SDRAM clock signal using the TLA7AA4 logic analyzer probing.

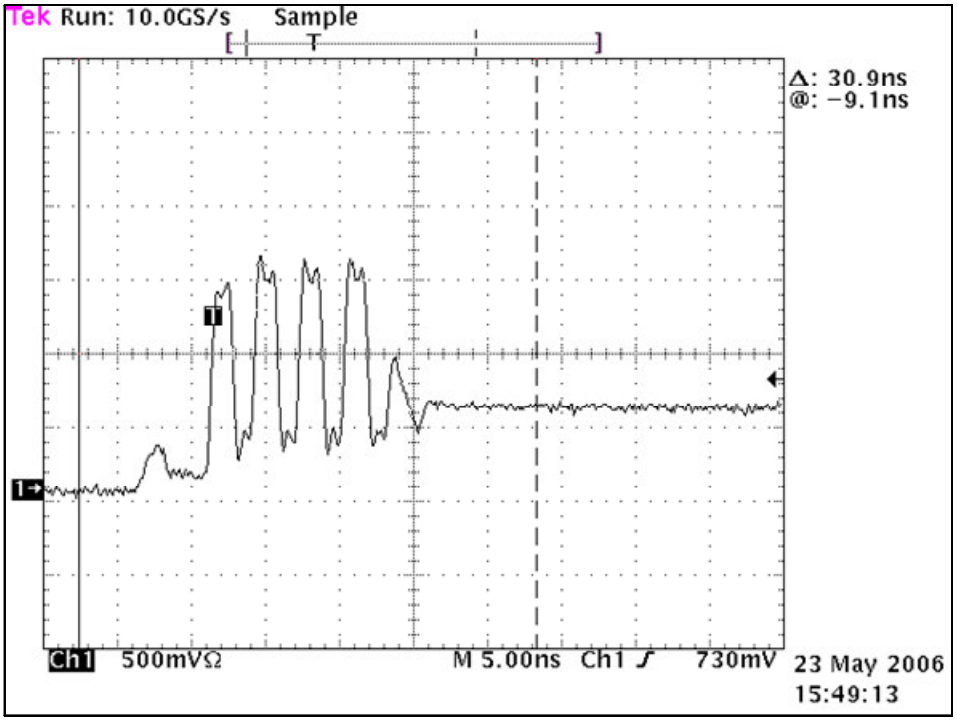


Figure 11: Oscilloscope waveform of the DDR2 667 SDRAM strobe signal using the TLA7AA4 logic analyzer probing. Notice the 8 strobe edges reflecting the burst length of 8.

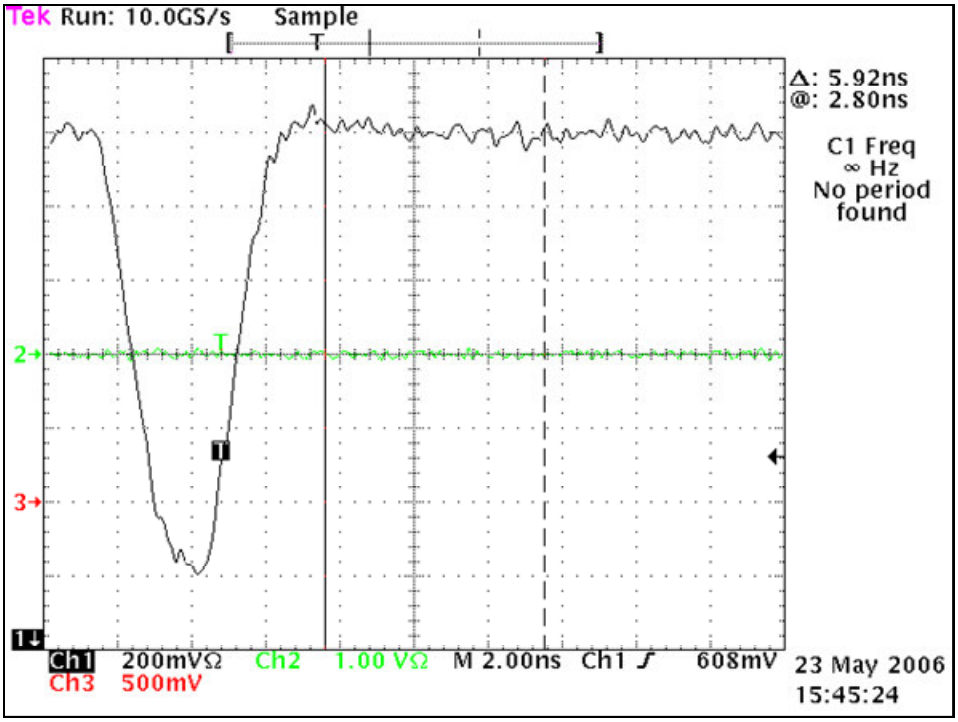


Figure 12: Oscilloscope waveform of the SODIMM S0 signal using the TLA7AA4 logic analyzer probing.

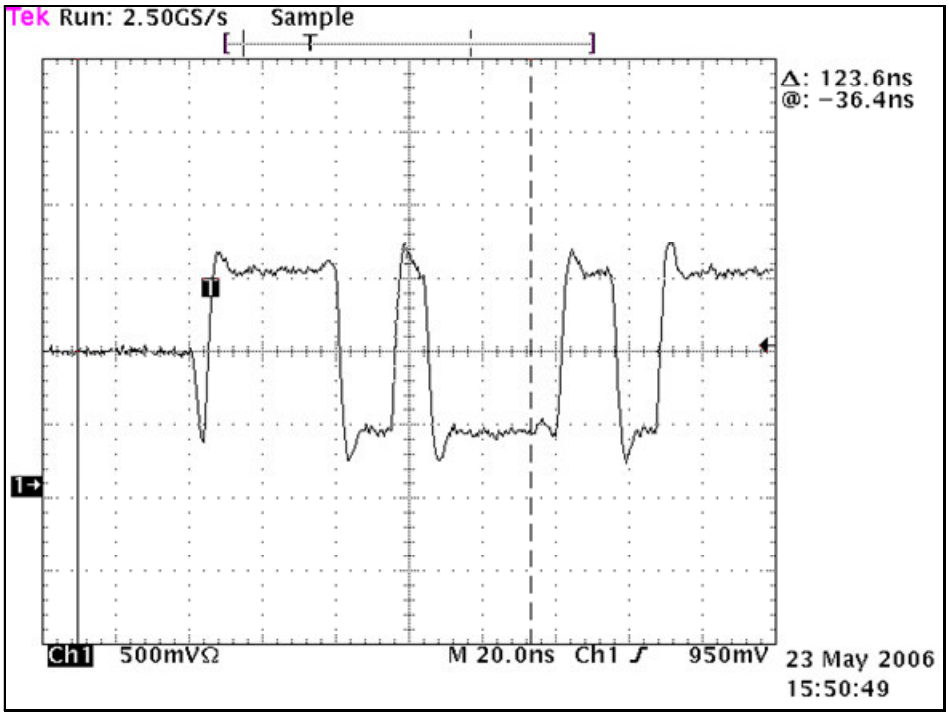


Figure 13: Oscilloscope waveform of the DDR2 667 SDRAM address signal using the TLA7AA4 logic analyzer probing.

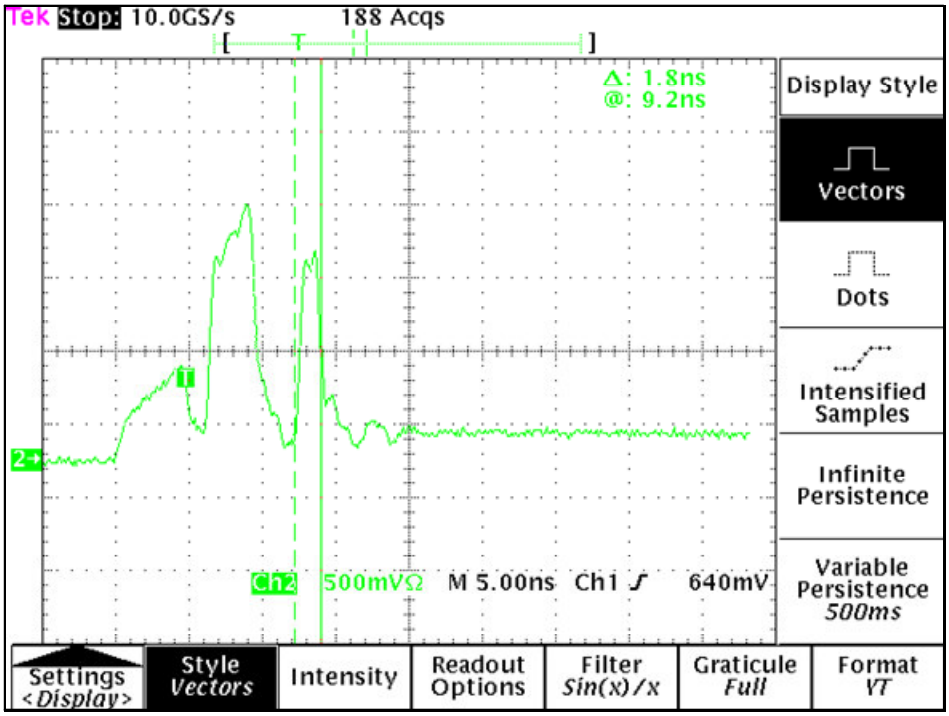


Figure 14: Oscilloscope waveform of the DDR2 667 SDRAM data signal using the TLA7AA4 logic analyzer probing.

More Information

All acquisition data was taken using a laptop with DDR2 667 SDRAM plugged into an SODIMMDDRIINEXVu.

SODIMMDDRIINEXVu specific information including a downloadable datasheet and manual can be obtained at: http://www.nexustechnology.com/products/memory/ddrii/sodimmddrii800nexvu/

For more information on Nexus products please visit www.nexustechnology.com.

Questions regarding this Applications Note or the NEX-SODIMMDDRII667/800NEXVu product should be directed to Nexus Technology at support@nexustechnology.com or 877-595-8116.

