DDR Support for Tektronix TLA Logic Analyzers

What is DDR?

DDR stands for Double Data Rate SDRAM. It is the follow-on to conventional PC100 / PC133 SDRAM. The biggest difference is that data is clocked on both edges of the SDRAM clock, hence the name Double Data Rate.

DDR Specifications that are critical for acquisition with a Logic Analyzer

DDR has Differential Clocks, and a Logic Analyzer cannot directly accept a differential clock.

DDR data strobes (DQS) are used to clock DDR data bits. During Read cycles the Data strobes (DQS) are edge aligned with the read data. The strobe can occur before or during the data valid window. During Write cycles the Data Strobes (DQS) are centered in the write data. Although this is not a problem it is different from the read data. The data strobes (DQS) are either center aligned (for Write data) or edge aligned (for Read data) which means that you cannot set a single acquisition point relative to the strobes to acquire both Read and Write data.

There are 64 data bits and 8 data strobes. Each data strobe has 8 data bits associated with it. There is a fixed timing relationship between groups of 8 data bits and their associated strobes. However, there can be skew between the data strobes. This could require individual acquisition settings for each group of 8 data bits.

NEX-DDR Design Decisions

Getting the DDR signals to the TLA

The NEX-DDR adapter:

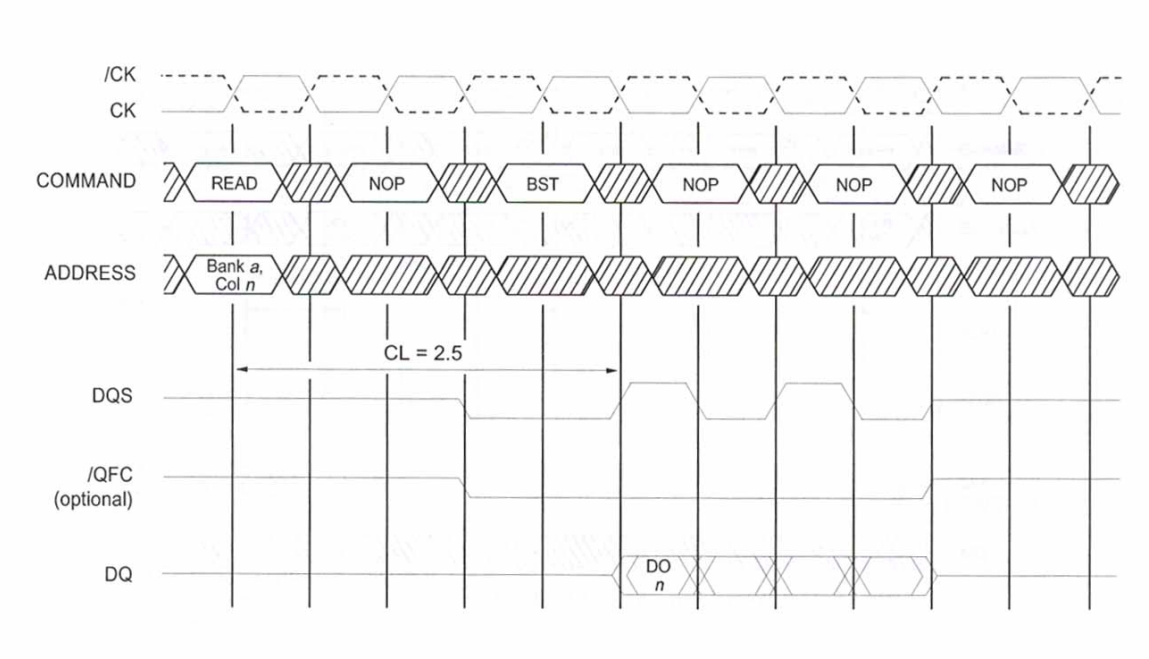
- Is an Extender design so that no user DDR slots are lost. This also permits use in a single-slot application
- Uses Isolation resistors to minimize the effect of the Tektronix P6434 probes (already low at <2pf per signal input)
- Was designed with extensive care in the layout process to guarantee maximum signal integrity
- Has matched trace length layout to maintain DDR bus timing
- Is Impedance controlled to minimize transmission reflections
- Has DDR signals routed to Mictor connectors to maximize the quality of the layout

Acquiring the DDR signals on the TLA

All data is clocked using one of the DDR Clocks (either CK0 or CK1). The positive rail of the differential DDR clock is used as the clock to the TLA Logic Analyzer. The DDR Common Clock was used as a reference because the TLA does not support (nor does any other Logic Analyzer on the market) 8 individual clock inputs which would be required if the Strobes were to be used. DDR Read and Write Data is acquired at different times by utilizing the ability of the TLA to acquire different groups of data at different points in time relative to a clock edge, thus negating the need to use the Strobes as clocks. The acquisition points for the Read and Write data can be set to the proper acquisition points so that valid data can always be acquired with no regard to the skews between Strobes. The benefits are:

- No differential to single-ended conversion required
- Critical signal timing is maintained since there is no delay added with a converter chip
- No hardware on the adapter is required to latch the Read and Write data

DDR Timing / Read Command

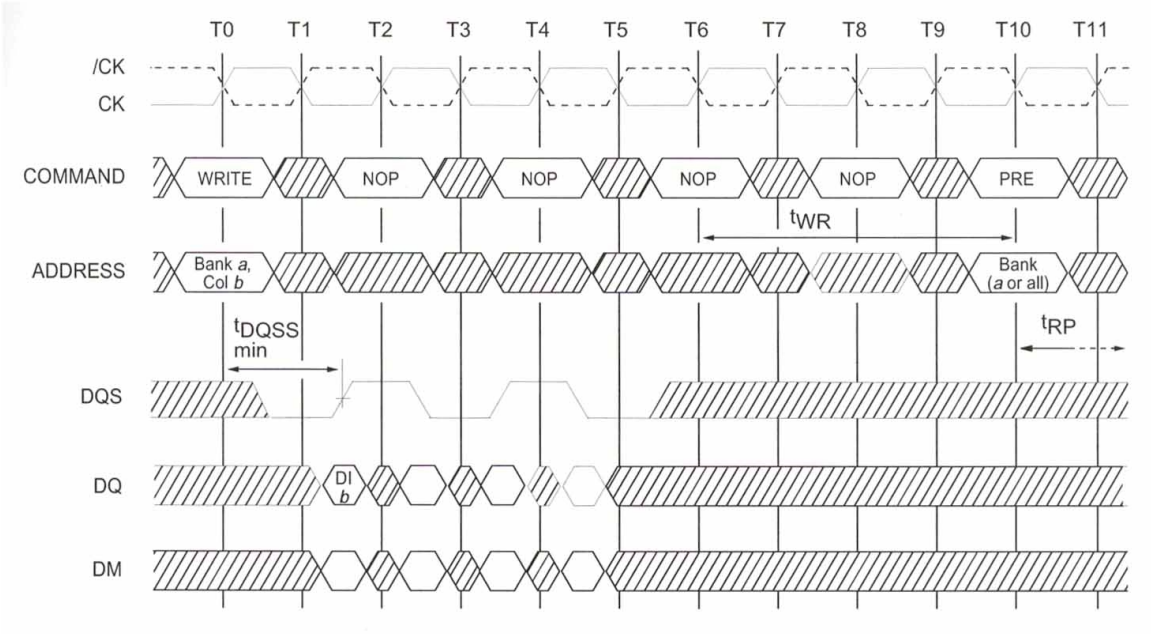


Address, Command and Read Data timing relative to Data Strobes and CLK

DDR Address and Command are valid on the rising edge of DDR clock (CK). DDR Address and Command are acquired with the TLA using the rising edge of CK as the clock input. Read data is edge aligned with the Data Strobes (DQS) and the DDR clock (CK). Read data is acquired on the TLA by acquiring the data relative to the DDR clock

(CK). The programmable setup/hold on the TLA is set to acquire the DDR data shortly after the DDR CK rising and falling edge.

DDR Timing / Write Command



Address, Command and Write Data timing relative to Data Strobes and CLK

DDR Address and Command are valid on the rising edge of DDR clock (CK) just as they are during a Read Command. DDR Address and Command are acquired with the TLA using the rising edge of CK as the clock input. Write data is center aligned with the Data Strobes (DQS). Write data is acquired on the TLA by acquiring the data relative to the DDR clock (CK). The timing difference is measured between the DDR clock (CLK) and the data valid window. This difference is used as the acquisition point relative to the DDR clock edges. It is entered on the TLA as a programmable setup/hold setting for acquisition.

DDR Data Acquisition Explained

Background

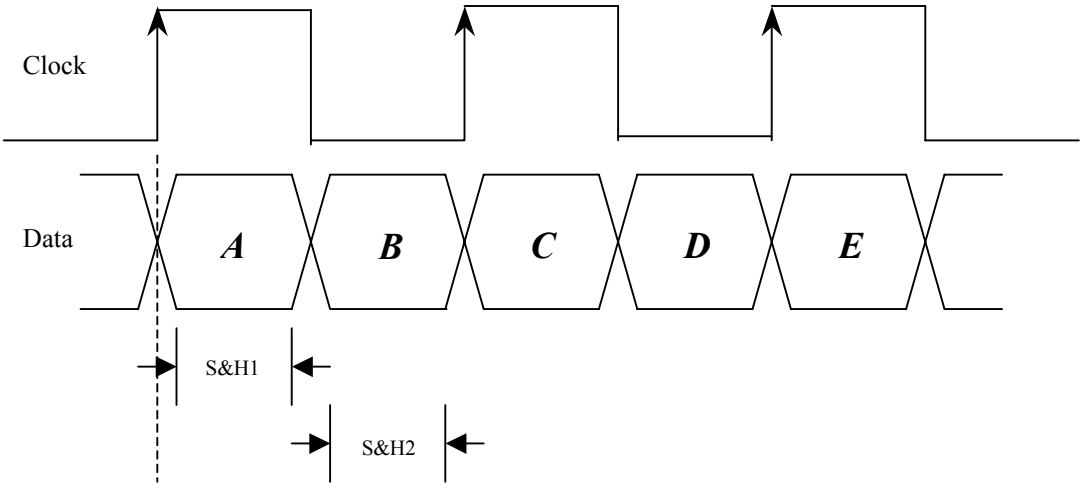
Many people look at the specifications for DDR data acquisition and conclude that the TLA is unable to acquire DDR data because of the speeds involved. Although some may concede that DDR200 could be supported (200MHz data rate), many assume that DDR266 (266MHz data rate) is beyond the reach of the TLA. Most parties assume this because of the 200MHz synchronous clock speed specification of the TLA.

Those people couldn't be further from the truth.

Because of the unique and powerful architecture of the TLA acquisition cards, it is possible to acquire data at up to a 400MHz data rate. This is possible because of two features – the ability to demultiplex incoming data and the ability to shift the data sample points on a group-by-group basis.

Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section ***and*** the D3 section. Through the User Interface of the TLA, demux can be performed by connecting the A0-A3 sections and storing the data in both the A0-A3 and D0-D3 data sections. More extensive demux capabilities are possible using the software tools that were used to create the various DDR packages. A very useful side benefit of using demux is that, since only one set of TLA data channels have to be connected, only one probe load is added to the target, even though data is stored in two different locations of the acquisition card.

The second piece of the DDR puzzle falls into place using the adjustable sample points with different TLA data groups. Building on the previous example of demuxing A3 data to D3 sections, two groups would be created. One group would contain A3 data; the second D3 data. By defining two different sample points for each group (S&H1 and S&H2) it is possible to acquire data at two different times in relation to the clock edge. This results in two data samples for every clock edge, or a data rate that is twice the frequency of the clock. When connected to a 200MHz clock this results in a data rate of 400MHz.



Given a data stream and clock as shown, the proper TLA setup would be as follows:

Group A	A3:7-0	Sample Point: S&H1
Group B	D3:7-0	Sample Point: S&H2

Since data will be acquired using demux, only the Group A channels (A3:7-0) need to be connected to the target. This setup results in a data display as follows:

Sample	Group A	Group B
0	A	B
1	C	D
.		
.		
.		

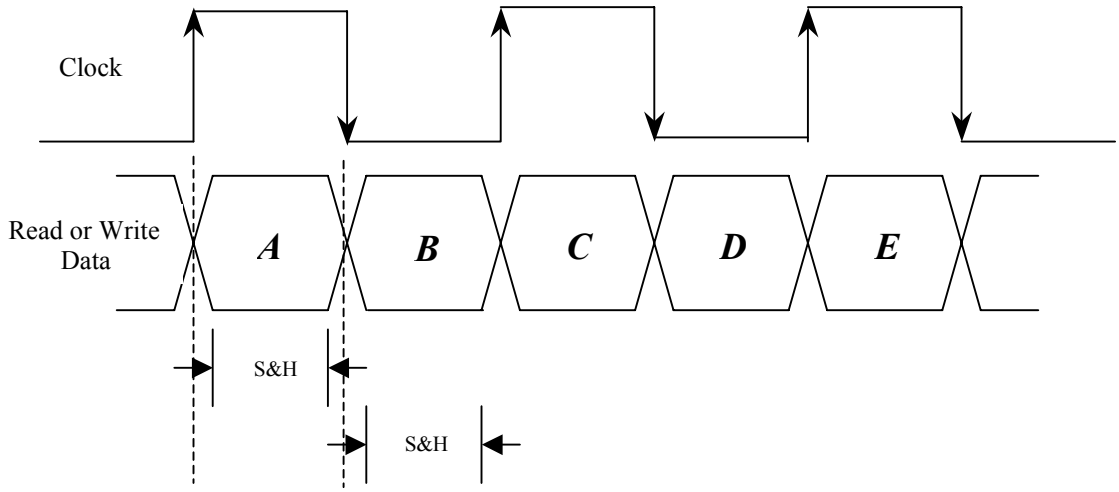
When a 136-channel TLA acquisition card is used in this mode one can acquire 68-channels of data (because of the 1-2 demux) at a 400MHz rate.

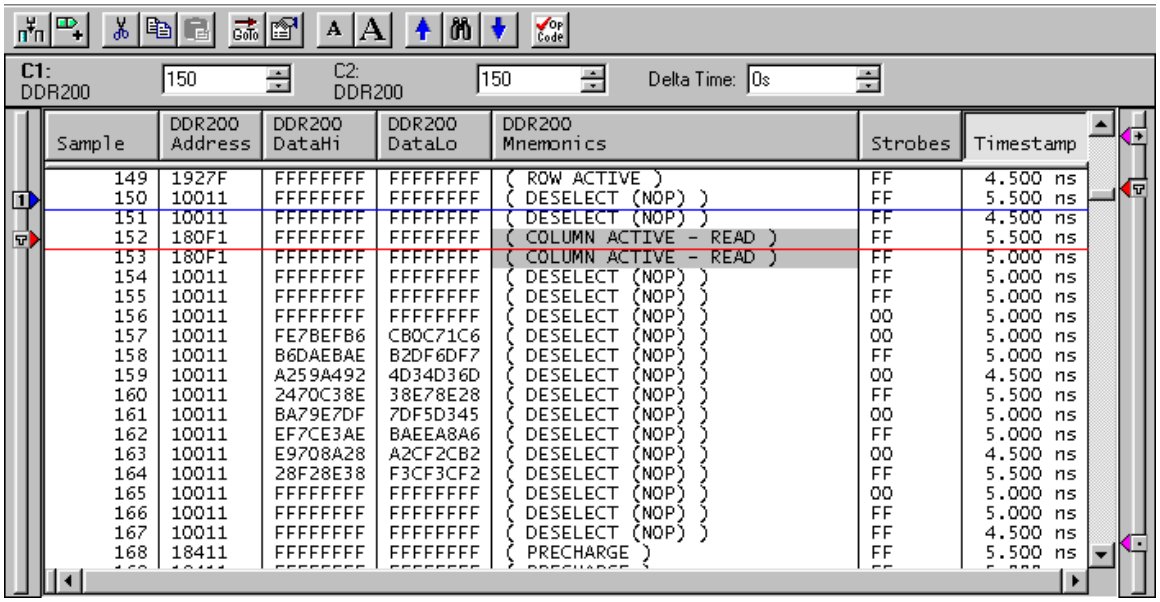
DDR Acquisition - General

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. The speeds of DDR (200 and 266MHz) require different setups to enable proper data acquisition. In addition, instead of trying to use the 8 Data Strobes to acquire data our solution uses one of the DDR SDRAM Clocks (either CK0 or CK1, user selectable) and all data acquisition is adjusted in relation to the clock edges. The 8 Data Strobes cannot be easily used to acquire data as the TLA only supports 4 Clock Inputs.

DDR200 Support

This support requires a single 200MHz 136-channel TLA acquisition card or a 200MHz TLA6X4 Logic Analyzer. Because of the speed and channel count requirements only Read or Write data can be acquired during a single acquisition. Data is acquired on every edge of the 100MHz DDR clock, and demultiplexing of the data is not done. Typical usage requires setting the Sample Point only for the DataHi and DataLo groups. However, if unusually large skews exist between some of the Data Strobes and their associated groups, then Sample Points can be set for each of the 8 Data groups (DatByte0-7) so that valid data acquisition can be assured. It is important to note that setting Sample Points (termed Setup & Hold points in the TLA) on any of the individual data groups (DatByte0-7) will override any adjustments made to the overall data groups (DataHi and DataLo).

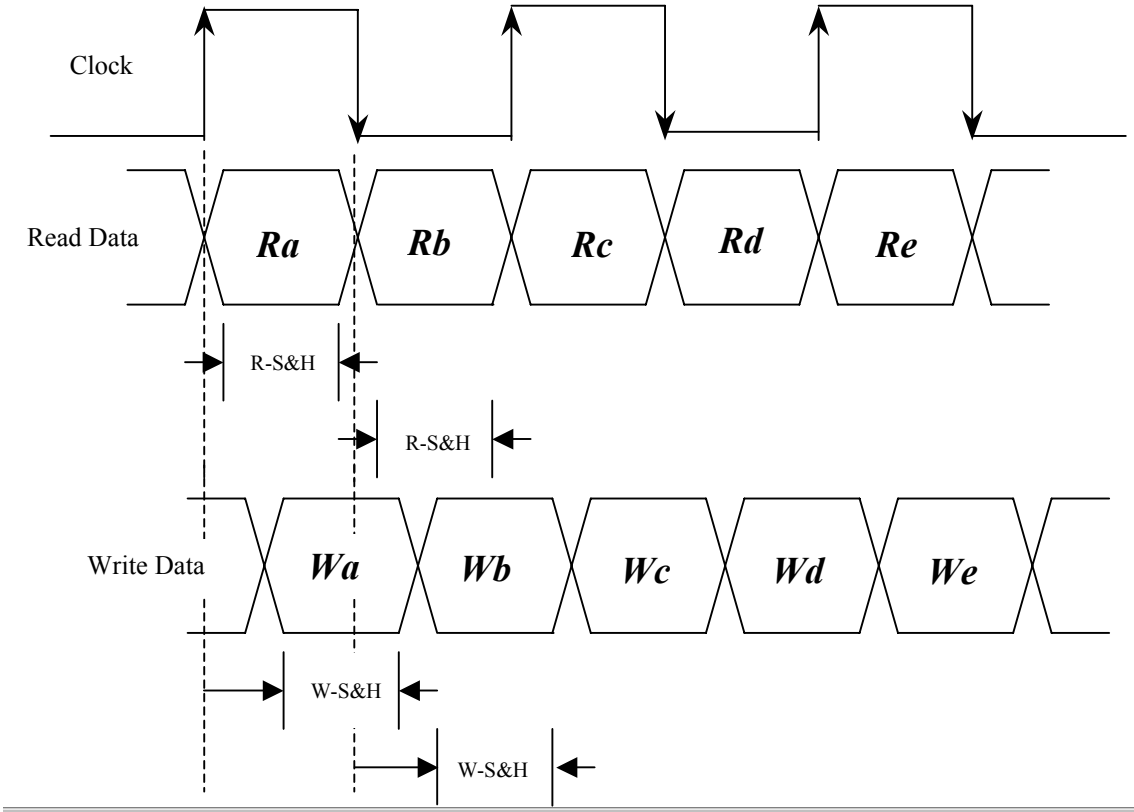



C1: DDR200 150 C2: DDR200 150 Delta Time: 0s

Sample	DDR200 Address	DDR200 DataHi	DDR200 DataLo	DDR200 Mnemonics	Strobes	Timestamp
149	1927F	FFFFFFFF	FFFFFFFF	(ROW ACTIVE)	FF	4.500 ns
150	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.500 ns
151	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	4.500 ns
152	180F1	FFFFFFFF	FFFFFFFF	(COLUMN ACTIVE - READ)	FF	5.500 ns
153	180F1	FFFFFFFF	FFFFFFFF	(COLUMN ACTIVE - READ)	FF	5.000 ns
154	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.000 ns
155	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.000 ns
156	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	00	5.000 ns
157	10011	FE7BEFB6	CB0C71C6	(DESELECT (NOP))	00	5.000 ns
158	10011	B6DAEBAE	B2DF6DF7	(DESELECT (NOP))	FF	5.000 ns
159	10011	A259A492	4D34D36D	(DESELECT (NOP))	00	4.500 ns
160	10011	2470C38E	38E78E28	(DESELECT (NOP))	FF	5.500 ns
161	10011	BA79E7DF	7DF5D345	(DESELECT (NOP))	00	5.000 ns
162	10011	EF7CE3AE	BAEEA8A6	(DESELECT (NOP))	FF	5.000 ns
163	10011	E9708A28	A2CF2CB2	(DESELECT (NOP))	00	4.500 ns
164	10011	28F28E38	F3CF3CF2	(DESELECT (NOP))	FF	5.500 ns
165	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	00	5.000 ns
166	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	5.000 ns
167	10011	FFFFFFFF	FFFFFFFF	(DESELECT (NOP))	FF	4.500 ns
168	18411	FFFFFFFF	FFFFFFFF	(PRECHARGE)	FF	5.500 ns

DDR200M Support

This support requires two (2) merged 136-channel 200MHz acquisition cards used in a TLA7XX. The merged cards enable both Read and Write data to be acquired simultaneously from a 200MHz DDR system. Data is acquired using both edges of the 100MHz DDR clock, and demultiplexing is done to permit acquiring both Read and Write data on every clock edge. One Sample Point must be adjusted to acquire valid Read data in reference to the clock edge; a second Sample Point must be set to acquire valid Write data in relation to the edge. Again, different Sample Points must be set for each of the Read / Write data groups (RDDatHi. RDDatLo, WRDatHi, and WRDatLo), and if necessary, sample points can be set for any of the 8-bit data groups.

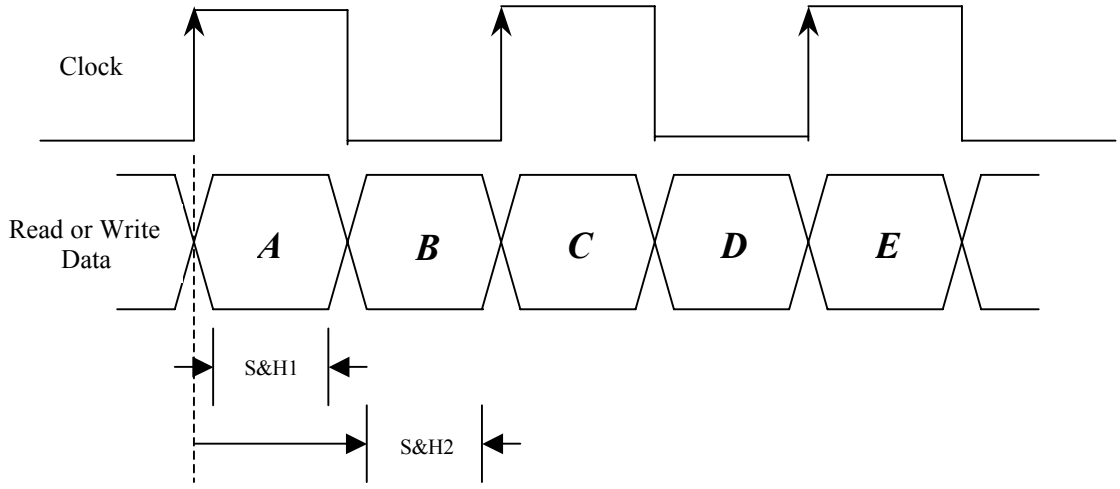


C1: No Data 61 C2: No Data 55 Delta Time: -30ns

Sample	Address	RDDatHi	RDDatLo	WRDatHi	WRDatLo	Command	Strobes	Timestamp
19	10011	20528000	008E0000	20528000	00070000	DESL--IGNORE_COMMAND--DATA?	20	-25.000 ns
20	142F3	20528004	0DCE0000	20528000	0DCE0000	ACTV--ROW_ADDRESS_STROBE_(SO~)	2C	-19.500 ns
21	142F3	20528004	0C460000	20528004	0DCE0000	ACTV--ROW_ADDRESS_STROBE_(SO~)	2C	-15.000 ns
22	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	-9.500 ns
23	10011	20528000	010C0000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	-5.000 ns
24	14031	2052800C	050C0000	20528000	050C0000	READ--COL_ADDR_READ_(SO~)	20	0 ps
25	14031	20528008	040C0000	2052800C	050C0000	READ--COL_ADDR_READ_(SO~)	28	5.000 ns
26	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	10.500 ns
27	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	15.000 ns
28	10011	20528000	040C0000	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	20.500 ns
29	10011	20D38C30	C30C20A2	20528000	040C0000	DESL--IGNORE_COMMAND--DATA?	20	25.000 ns
30	10011	2C528082	08248208	20D38C30	C30C20A2	DESL--IGNORE_COMMAND--DATA?	B4	30.500 ns
31	10011	7D77F7DF	FFFDF3C7	2C528082	08248208	DESL--IGNORE_COMMAND--DATA?	60	35.500 ns
32	10011	BA739659	65155555	7D77F7DF	FFFDF3C7	DESL--IGNORE_COMMAND--DATA?	FF	40.000 ns
33	10011	2EFAEBBE	FBAE39E7	BA739659	65155555	DESL--IGNORE_COMMAND--DATA?	20	45.000 ns
34	10011	E3DEB4D3	4D3492CB	2EFAEBBE	FBAE39E7	DESL--IGNORE_COMMAND--DATA?	FF	50.500 ns
35	10011	FBFFBCF7	DF6D9618	E3DEB4D3	4D3492CB	DESL--IGNORE_COMMAND--DATA?	20	55.500 ns
36	10011	A6DBEDB4	D75D65B6	FBFFBCF7	DF6D9618	DESL--IGNORE_COMMAND--DATA?	3C	60.500 ns
37	10011	A252A1B4	00044482	A6DBEDB4	D75D65B6	DESL--IGNORE_COMMAND--DATA?	20	65.000 ns
38	10011	AEDBADB6	0E0761B6	A6DBEDB4	D75D65B6	DESL--IGNORE_COMMAND--DATA?	20	70.500 ns
39	10011	A8D2AC30	08040010	AEDBADB6	0E0761B6	DESL--IGNORE_COMMAND--DATA?	21	75.000 ns
40	10011	2652A024	00054010	A0D2A030	00040010	PRE--PRECHARGE_SELECT_BANK_(SO~)	20	80.000 ns
41	14411	24528004	08044010	26528024	08054010	PRE--PRECHARGE_SELECT_BANK_(SO~)	20	85.000 ns
42	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	90.500 ns
43	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	20	95.000 ns
44	10011	20528000	00040000	20528000	00040000	DESL--IGNORE_COMMAND--DATA?	22	100.500 ns

DDR266 Support

This support also requires two (2) merged 136-channel 200MHz acquisition cards used in a TLA704, TLA714, TLA711, or TLA720. Data is acquired using the rising or falling edge of the 133MHz DDR clock, and demultiplexing is done to permit acquiring two samples of Read or Write data from the selected clock edge. Because of the increase in data bus speed, only Read or Write data can be acquired during a single acquisition. A_Data information is earlier (older) data than the information stored in B_Data. Again, different Sample Points must be set for each of the four 32-bit Data groups, and again, if necessary, sample points can be set for any of the 8-bit data groups.



C1: DDR266 0 C2: DDR266 0 Delta Time: 0s

Sample	Address	A_DatHi	A_DatLo	B_DatHi	B_DatLo	Command	Strobes	Timestamp
54	1A09F	20528000	00040000	20528000	01240000	PRE--PRECHARGE_SELECT_BANK_(SO~)	20	7.500 ns
55	1B871	20528008	00240000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
56	1B871	20528000	00050000	20528000	40040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
57	1A09F	20528000	00040000	20528000	01250000	ACTV--ROW_ADDRESS_STROBE_(SO~)	20	7.500 ns
58	1B871	20528008	00240000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
59	1B871	20528000	00040000	20528000	00240000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
60	1B871	20528000	00040000	20528000	00040000	READ--COL_ADDR_READ_(SO~)	20	7.500 ns
61	1B871	20528000	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
62	1B871	20528000	00050000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
63	1B871	20528000	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
64	1B871	AA7BA79E	7DF7DF5D	EB7EF3CE	3AEFAEAA	NOP--NO_OPERATION_(SO~)	FF	7.500 ns
65	1B871	EF7E9208	A28E2CB2	28F28A28	E38F3CF3	NOP--NO_OPERATION_(SO~)	FF	7.500 ns
66	1B871	28F28A28	E38F3CF3	28F28228	A00E3CF3	NOP--NO_OPERATION_(SO~)	20	7.500 ns
67	1B871	28528008	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	8.000 ns
68	1B871	20528000	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
69	1B871	20528000	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
70	1B871	20528000	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
71	1B871	20528000	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.500 ns
72	1B871	20528000	00040000	20528000	00040000	NOP--NO_OPERATION_(SO~)	20	7.000 ns