
NEX-CPCI-A



- High Density Connectors provide quick, convenient connection to the CompactPCI bus
- Disassembly of the CompactPCI bus
 - Cycle Identification
 - Config Cycle decoding including register evaluation
 - Ability to selectively ignore Idle and Wait States
- Extender card design works in either System Slot or Peripheral Slot
- Logic Analyzer Setup Software gets you up and running fast
- Unique features when using a TLA600 or TLA700
 - Timing Analysis to 8GHz (125ps) on each channel
 - Simultaneous State and Timing acquisition on each channel
 - Trigger on setup/hold violations on all channels
 - Part Number for AMP Mictor Connector is 767054-1

CPCI32A and CPCI64A Disassembly Software

The included NEX-CPCI32A and NEX-CPCI64A disassembly software executes on the Tektronix Logic Analyzer. This software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler. All CompactPCI Cycle types are identified and Config cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text (see Fig. 1). Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE disk, Video controller, network interface, etc.) is being accessed (see Fig. 1).

It is also possible to filter the data display to show only those cycle types of interest. The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest. Figure 4 shows the same area of acquired data as that in Figure 1, but with Memory and I/O cycles suppressed

Another feature of the disassembly software is its ability to intelligently acquire CompactPCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the disassembly software is able to acquire only the CompactPCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes the user also has the ability to override this function and acquire data on every CompactPCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Timing Analysis

Timing analysis of the CompactPCI bus can be done at the maximum asynchronous rate of the Tektronix Logic Analyzer. For example the TLA600 or TLA700 with a minimum of 102 channel acquisition module can acquire timing data at 8GHz (125ps) on each channel. Fast timing acquisition and low capacitive loading (the passive NEX-CPCI-A adapter module and the < 2pf/P6434 and 0.7pf/P6860 logic analyzer probe) provide excellent timing analysis on each monitored channel of the CompactPCI bus.

NEX-CPCI Adapter Module

The NEX-CPCI-A adapter provides a quick convenient connection to standard Tektronix logic analyzers. It requires the use of three Tektronix P6434/6860 high density probes for connection to the TLA600/700.

The NEX-CPCI-A extends the CompactPCI bus beyond the specified etch length. Depending on the design of the system, users may experience difficulties with this. The Logic Analyzer attaches to the NEX-CPCI-A adapter using a high density impedance matched connector. The typical Logic Analyzer loading is < 2pf/P6434 and 0.7pf/P6860.

The NEX-CPCI-A adapter supports 3.3V and 5V applications.

Timestamp

All acquired data is timestamped on Tektronix logic analyzers; no acquisition memory is used to accomplish this. The timestamp resolution on the TLA600/700 system is 125ps.

Correlation

While the NEX-CPCI-A package is being used with a Tektronix logic analyzer to monitor the CompactPCI activity, another acquisition module can be used to monitor activity elsewhere within the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred. For instance, the system microprocessor could be monitored and correlated with bus activity to verify CPU and CompactPCI bus communication.

Setup/Hold Triggering

Setup and hold specifications can be verified, and margins tested, using the TLA600/700. Each channel group (address, data, control, etc..) or individual channel can have a different setup time and hold time violation set as a fault trigger. If any individual channel or any channel in a group is ever in violation of the specified setup and hold time, the logic analyzer will stop and show the violation. The timing resolution of the acquired data at the violation point is 8GHz (125ps).

Setup and hold margin testing can be done by altering the setup and hold times set for the violation trigger in 125ps increments. Changing these values until a violation occurs will show the actual setup and hold of the system under test.

Simultaneous State and Timing Acquisition

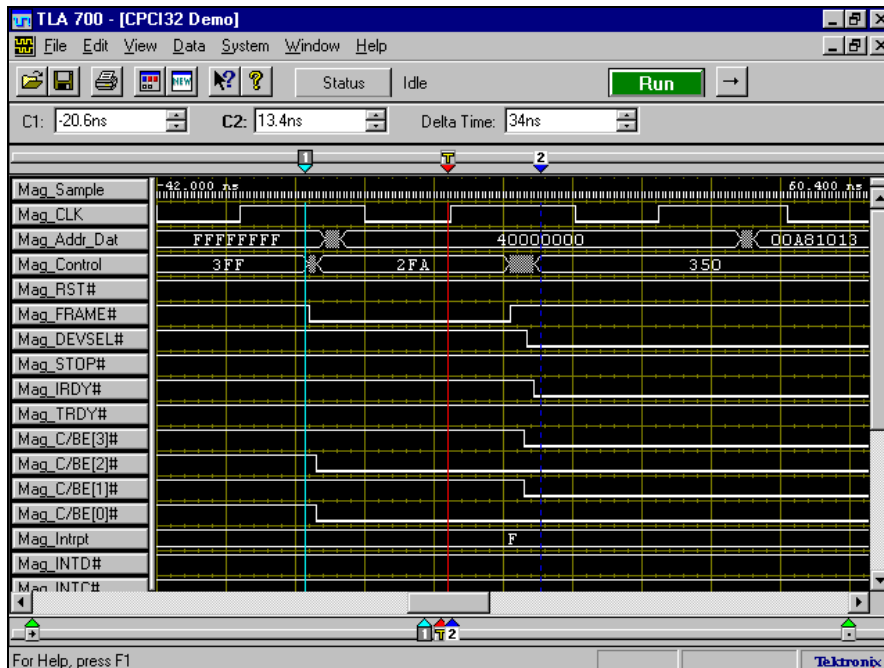
The Tektronix TLA600/700 Logic Analyzer offers the unique capability of being able to acquire timing and state data through the same probes at the same time. For example, a user is able to view timing data acquired at 125ps resolution, with state data acquired synchronously (for instance, using NEX-CPCI-A custom clocking or clocking on every rising edge of CLK). This resolution gives the hardware designer the ability to easily determine edge relationships between any signal without having to deal with the inconvenience and loading problems that are inherent when forced to double-probe with individual state and timing acquisition cards.

Disassembly (State Analysis)

Sample	CPCI32 Addr_Dat	CPCI32 Mnemonics	Timestamp
	----01BB	Parity Errors disabled	
	----01BB	VGA Palette Snoop enabled	
	----01BB	Mem Write & Inv. enabled	
	----01BB	Special Cycle Recog. enabled	
	----01BB	Master disabled	
	----01BB	Memory Access enabled	
	----01BB	I/O Access enabled	
65533	2000000C	CONFIG READ ADDRESS	1.120,500 us
	2000000C	Type 0 Register 3 Function 0	
65534	--00----	CONFIG READ DATA	121.000 ns
	--00----	Single Function; Header Type 0	
65535	40000000	CONFIG READ ADDRESS	1.059,000 us
	40000000	Type 0 Register 0 Function 0	
65536	00A81013	CONFIG READ DATA	90.500 ns
	00A81013	Device ID 168 Vendor ID 4115	
65537	40000008	CONFIG READ ADDRESS	1.059,000 us
	40000008	Type 0 Register 2 Function 0	
65538	030000FC	CONFIG READ DATA	91.000 ns
	030000FC	Class 0x03 - Display controller	
	030000FC	Sub-Class 0x00	
	030000FC	Prog. I/F 0x00 - VGA compatible	
	030000FC	Revision ID 252	
	4000000C	CONFIG READ ADDRESS	1.223,000 us

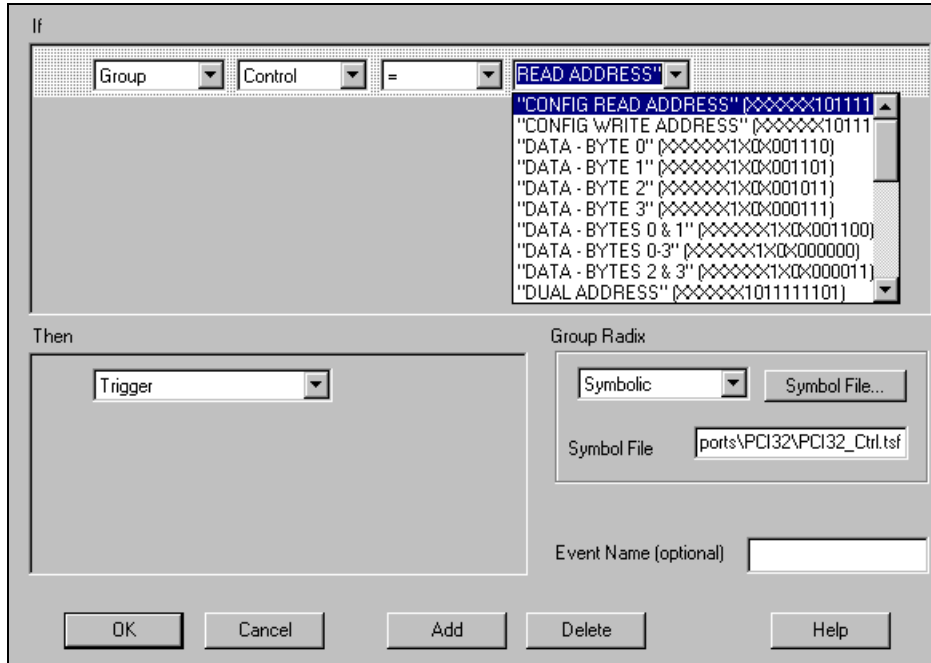
CompactPCI cycles are identified and Config cycles are decoded. Device information is translated according to Class, sub-Class and Type.

Timing Analysis



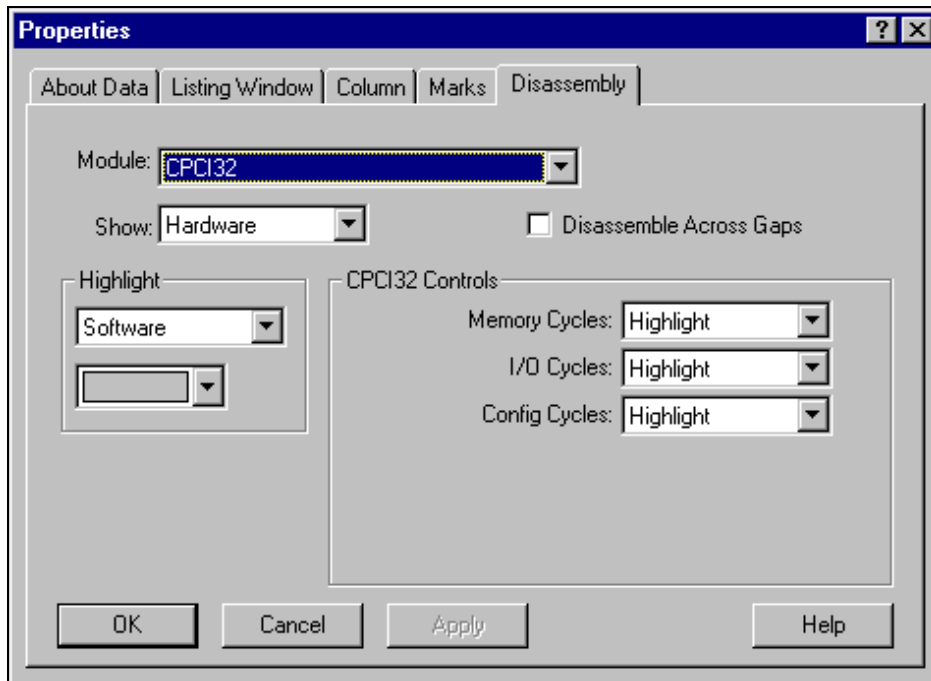
125ps acquisition on each channel provides excellent timing analysis. Each channel is labeled with the appropriate CompactPCI signal name. Bus format display of grouped signals shown.

Triggering



Trigger on pre-defined CompactPCI cycles.

Filter Select Menu

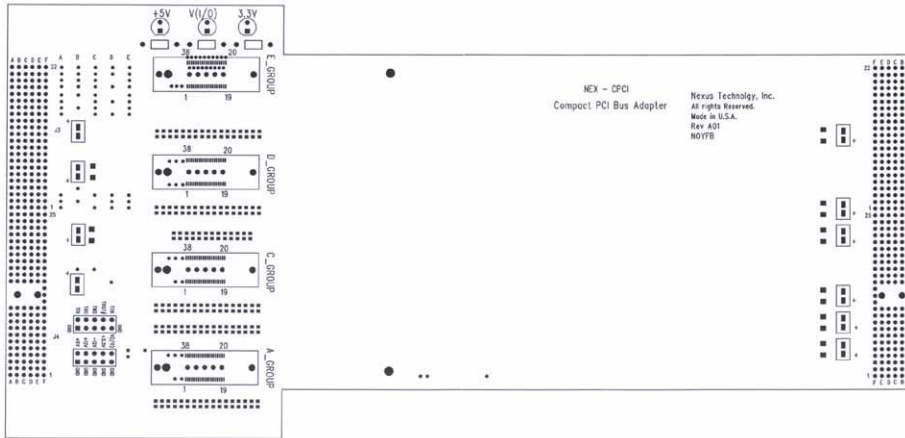


Selectable data filtering for memory, I/O and Config cycles.

Tektronix Logic Analyzers Supported

TLA600 or TLA700 with a minimum of 102 channel acquisition module (requires 3-P6434/P6860 probes from Tektronix).

Mechanical Outline



Ordering / Contact Information

Part Number NEX-CPCI-A

Includes: NEX-CPCI-A adapter
NEX-CPCI32A Software for TLA600/700
NEX-CPCI64A Software for TLA600/700
Manual

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Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

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