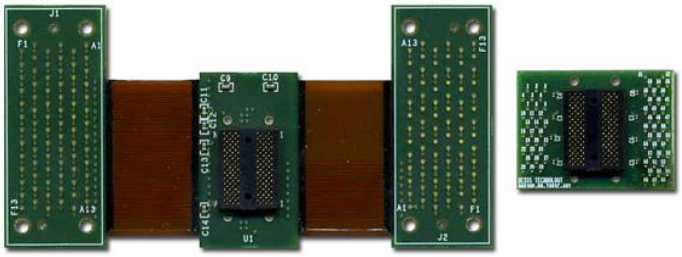
DDRII Component Interposers

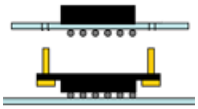
Premier DDRII Component Digital & Analog Validation

Nexus Technology recommends DDRII component interposers for applications requiring optimal digital and analog validation of speeds up to DDRII-1067 or for embedded applications, in general.

These interposers allow for logic analyzer and/or oscilloscope acquisition of command, address, read, and write data of x4, x8 and/or x16 DDRII memory components at speeds up to DDRII-1067.



Premier Component Interposer Design



Optimal DDRII validation requires analysis of the signals, as seen by the memory components. This allows for the highest confidence that the signals captured are representative, contain little interference, and present the maximum possible data eye size. Nexus Technology component interposers allow for logic analyzer and/or oscilloscope probing of the DDRII signals extremely close to the memory components.

Probe Installation

The process of attaching the interposer to your target has been greatly simplified using Nexus Technology's patented, high-bandwidth, component interposer sockets. These patented sockets **completely remove the need to contract specialized rework houses** to perform the installation. Instead, our customers can use standard BGA assembly practices to install the component interposer socket. Further, Nexus Technology can perform the attachment service for a nominal fee.

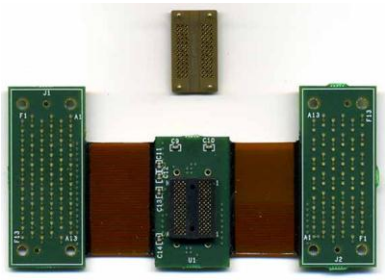
Once the interposer socket is installed on the target, logic analyzer or oscilloscope interposers can easily be inserted or removed from the socket. This provides a reusable interface to your target system and completely removes any need to rework customer targets or our component interposers. Note that the interposer socket elevates the interposer above the adjacent BGAs to provide the mechanical clearance necessary for easy probe attachment.

DDRII BGA Component Installation

A second socket for easy BGA memory component installation is also available for all Nexus Technology component interposers. These sockets are industry standard DDRII BGA sockets and allow for the quick swapping & testing of different memory components on the interposer. The NEXVu Sockets Quick Start Guide provides more information and is available on our website.

Logic Analyzer Component Interposers

Logic Analyzer Component Interposer Hardware



Connectivity and analysis to a logic analyzer are provided through x4, x8, and/or x16 logic analyzer memory component interposers. These controlled impedance, matched trace length interposers provide visibility up to 1,067MT/s (DDRII-1067) for digital validation using a logic analyzer. The rigid/flex/rigid design allows the interposer to be used in targets with little mechanical clearance around the target component.

Logic Analyzer Component Interposer Software

All Nexus Technology logic analyzer component interposers come with the required logic analyzer setup software, DDRII protocol decode software, DDRII data eye sample point analysis software, and a limited version of the protocol violation software. Optional full protocol analysis is available separately.

Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDRII transactions for easy display and logic analyzer triggering/filtering.

Data Sample Point Analysis Software

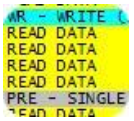
In order for the logic analyzer to capture data, the DDRII signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDRII data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes contain skew (relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

These, among other factors, can make reliable and accurate DDRII read and write data bus acquisition difficult - if done manually. NEX-DDR3-SPA, provided free, automates this process enabling quick and reliable DDRII read and write data bus acquisition in only minutes. For more information, please see the NEX-DDR3-SPA product page on our website.

Protocol Violation Software

There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDRII support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Full protocol violation analysis is available separately. Please see the NEX-DDR-PROTOCOL product for more information.

Logic Analyzer for Digital Validation

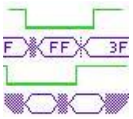


Logic analyzer setup software (TLA support package) is included with these products. This setup software acquires/reconstructs the command/address bus and acquires/reconstructs the read/write data from the data bus. The software also decodes and displays the bus protocol, shows the valid read/write data and provides easy DDR protocol triggering to quickly capture relevant data.

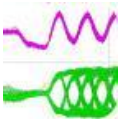
These products also come with a limited version of the NEX-DDR-PROTOCOL software tool. This software provides statistical information and global bus activity to quickly give the user an overview of the DDRII bus activity without having to revert to a listing or waveform window. The software also performs basic protocol violation checking. Advanced protocol violation checking is available for purchase separately. Please see the NEX-DDR-PROTOCOL product for more information on this powerful tool.

Logic Analyzer for Analog Validation

Although these logic analyzer interposers are designed for optimal digital validation, there are a number of useful features and tools available to assist in the analog validation process.



The most readily available tool is the Tektronix Logic Analyzer's 20ps (50GHz) MagniVu timing. This 2.5us deep acquisition space, separate from state acquisition memory is simultaneously acquired with state data, and is typically filled with bus activity that occurred around the state trigger. A wealth of analog information can be found in this data, including: positive/negative pulse widths, signal skew, and data glitches. Activity that appears too short, too long, unreasonably skewed relative to another signal, or that contains glitches are indications that there is an analog characteristic of that signal that deserves further attention.

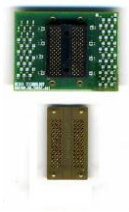


Another powerful analog validation feature is the Tektronix Logic Analyzer's Analog Mux capability. When paired with an oscilloscope, this feature enables analog visibility of every DDRII signal probed by the interposer. Any of the ten or so command bits, sixteen-plus address bits and any of the data bits can be viewed on an oscilloscope in seconds and - literally - with a touch of a button. This feature comes with two significant limitations. First, there is no calibration specification for the channel-to-channel skew through the Analog Mux. Second, the signals are bandwidth limited to 3GHz. This limitation acts as a high speed filter, limiting the visibility of the signal's harmonics that are over 3GHz. For DDRII-1067, this filtering will cause artificial increases in the slew rates which appear as rising/falling edges that take longer to transition. The effect on the data eyes will be similar, showing a rounding effect. Although these limitations force the user to find alternate methods for accurate analog validation, the importance of this tool for preliminary analog validation can not be understated. The ability of an digital validation engineer to quickly and easily assess the general analog health of a target can save an enormous amount of time and resources.

Tektronix discusses some of these topics in more detail in the application note, Debugging Timing Problems with a Logic Analyzer available for download from tek.com. Nexus Technology recommends these products for the debugging methods and practices described in this application note.

Oscilloscope Component Interposers

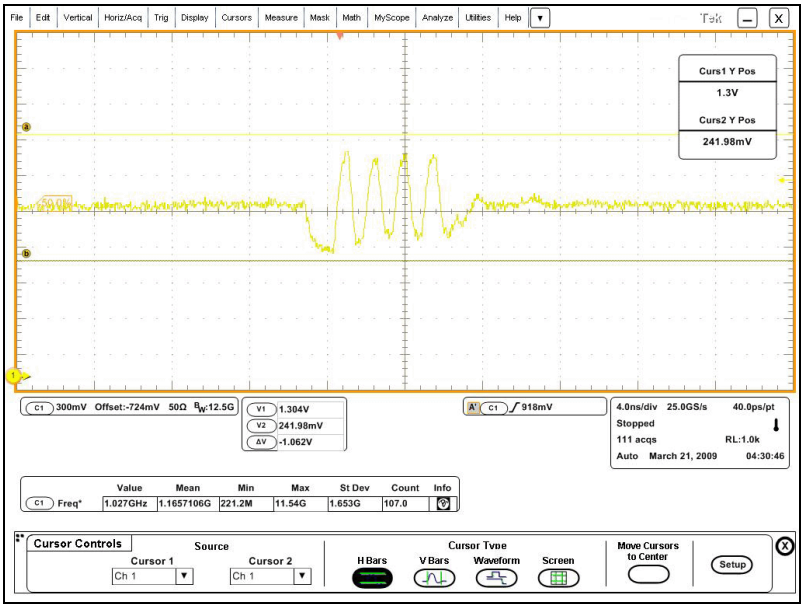
Oscilloscope Component Interposer Hardware



Connectivity and analysis to a oscilloscope are provided through x4, x8, and/or x16 oscilloscope memory component interposers. These controlled impedance, matched trace length interposers provide visibility up to 1,067MT/s (DDRII-1067) for analog validation using a oscilloscope. All signals are brought out to pads that are designed to accommodate Tektronix solder down probe tips. Probe adapters can also be used to easily move the oscilloscope probe between signals for quick and accurate measurement.

Oscilloscope Analog Validation

Filter software, available from Tektronix for use with select Tektronix oscilloscopes, removes the effect of the oscilloscope interposer. Although these interposers are designed to optimize signal integrity, this feature removes even the slightest effect the adapter has from the oscilloscope display.

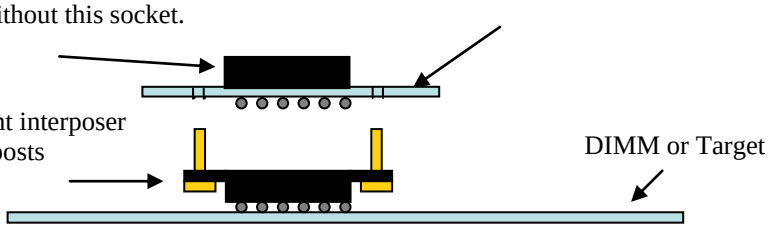


Strobe as Seen using the Oscilloscope Component Interposer

Attaching & Reusing Interposers

Memory component interposer.
Balls on the bottom simply push
into the custom socket on the target.

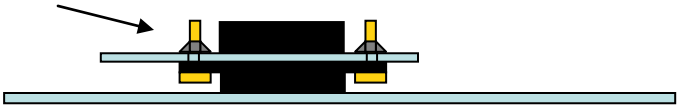
Standard DDRII socket on interposer, ready for
memory component insertion.
Also available without this socket.



Component interposer
socket w/posts

DIMM or Target

Solder added to mechanically
retain the adapter to the custom socket



Nexus Technology's Component Interposer Advantages

Probed at the BGA Balls

The best place to probe to eliminate reflections associated with standard embedded DDRII mid-bus probing or other methods. Interposers require no target footprints or special routing requirements that mid-bus probing requires.

Use with Existing Embedded Designs or DIMMs

No need to change existing designs. Simply add the interposer to your embedded target or DIMM with no re-design or added probe points.

Socket Design

The interposers are reusable. Once an interposer socket is installed, the interposer can be attached and removed by hand - allowing the interposer to be used on multiple targets quickly or allowing quick swapping of logic analyzer and oscilloscope interposers on the same target.

Support for DDRII x4, x8, and x16 Memory Devices

Full coverage for DDRII applications at speeds up to 1,067MT/s (DDRII-1067).

Easy to Install

By either adding the interposer socket using industry standard BGA attachment methods or by using Nexus Technology's attachment service.

Separate Oscilloscope & Logic Analyzer Products

Each interposer is designed for optimal signal integrity for use with an oscilloscope or logic analyzer.

Simple Digital & Analog Validation via Standard Interposer Socket

The easy to install interposer socket can be used with both the oscilloscope and logic analyzer interposers for maximum flexibility and very quick analog and digital validation.

Oscilloscope Interposer Software

Oscilloscope filter software removes effect of interposer. Available from Tektronix.

Logic Analyzer Software

Standard logic analyzer software includes: setup software, DDRII protocol decode software, DDRII data eye sample point analysis software, and protocol violation software.

Interposer Retention to the Target

The interposer socket has four posts that are soldered to four mounting holes on the interposer. This insures the interposer will not be mistakenly pulled off the target.

Product Configuration Tables

DDRII Oscilloscope Interposers

Nomenclature	Interposer Type	Data Width	DDR Speed	Component Socket Included	Installation Service Included
NEX-DDR2MP60BSCSK	Oscilloscope	x4/x8	DDRII-1067	Yes	No
NEX-DDR2MP60BSCSK-AT	Oscilloscope	x4/x8	DDRII-1067	Yes	Yes
NEX-DDR2MP60BSC	Oscilloscope	x4/x8	DDRII-1067	No	No
NEX-DDR2MP60BSC-AT	Oscilloscope	x4/x8	DDRII-1067	No	Yes
NEX-DDR2MP84BSCSK	Oscilloscope	x16	DDRII-1067	Yes	No
NEX-DDR2MP84BSCSK-AT	Oscilloscope	x16	DDRII-1067	Yes	Yes
NEX-DDR2MP84BSC	Oscilloscope	x16	DDRII-1067	No	No
NEX-DDR2MP84BSC-AT	Oscilloscope	x16	DDRII-1067	No	Yes

DDRII Logic Analyzer Interposers

Nomenclature	Interposer Type	Data Width	DDR Speed	Component Socket Included	Nexus Probes Included	Installation Service Included	Hardware Requirements
NEX-DDR2MP60BLASK	Logic Analyzer	x4/x8	DDRII-1067	Yes	No-See Note1	No	
NEX-DDR2MP60BLASK-AT	Logic Analyzer	x4/x8	DDRII-1067	Yes	No-See Note1	Yes	
NEX-DDR2MP60BLASKPR	Logic Analyzer	x4/x8	DDRII-1067	Yes	Yes-See Note1	No	
NEX-DDR2MP60BLASKPR-AT	Logic Analyzer	x4/x8	DDRII-1067	Yes	Yes-See Note1	Yes	
NEX-DDR2MP60BLA	Logic Analyzer	x4/x8	DDRII-1067	No	No-See Note1	No	
NEX-DDR2MP60BLA-AT	Logic Analyzer	x4/x8	DDRII-1067	No	No-See Note1	Yes	
NEX-DDR2MP60BLAPR	Logic Analyzer	x4/x8	DDRII-1067	No	Yes-See Note1	No	
NEX-DDR2MP60BLAPR-AT	Logic Analyzer	x4/x8	DDRII-1067	No	Yes-See Note1	Yes	1- TLA7000 Series Mainframe 1- TLA7Bxx See Note 2
NEX-DDR2MP84BLASK	Logic Analyzer	x16	DDRII-1067	Yes	No-See Note1	No	
NEX-DDR2MP84BLASK-AT	Logic Analyzer	x16	DDRII-1067	Yes	No-See Note1	Yes	
NEX-DDR2MP84BLASKPR	Logic Analyzer	x16	DDRII-1067	Yes	Yes-See Note1	No	
NEX-DDR2MP84BLASKPR-AT	Logic Analyzer	x16	DDRII-1067	Yes	Yes-See Note1	Yes	
NEX-DDR2MP84BLA	Logic Analyzer	x16	DDRII-1067	No	No-See Note1	No	
NEX-DDR2MP84BLA-AT	Logic Analyzer	x16	DDRII-1067	No	No-See Note1	Yes	
NEX-DDR2MP84BLAPR	Logic Analyzer	x16	DDRII-1067	No	Yes-See Note1	No	
NEX-DDR2MP84BLAPR-AT	Logic Analyzer	x16	DDRII-1067	No	Yes-See Note1	Yes	

Note 1: Two Nexus Technology NEX-PRB1XL probes are required and can be ordered as a complete package as shown in the table above.
Note 2: A TLA7BB2, TLA7BB3, or TLA7B4 module can be used. The module can have either the 750MHz or 1.4GHz state speed option.

Optional Additional Component Interposer Sockets

Nomenclature	Data Width	Quantity of Sockets
NEX-DDR260BGASKBA	x4/x8	1
NEX-DDR260BGASKBA-3	x4/x8	3
NEX-DDR284BGASKBA	x16	1
NEX-DDR284BGASKBA-3	x16	3

Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST.

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