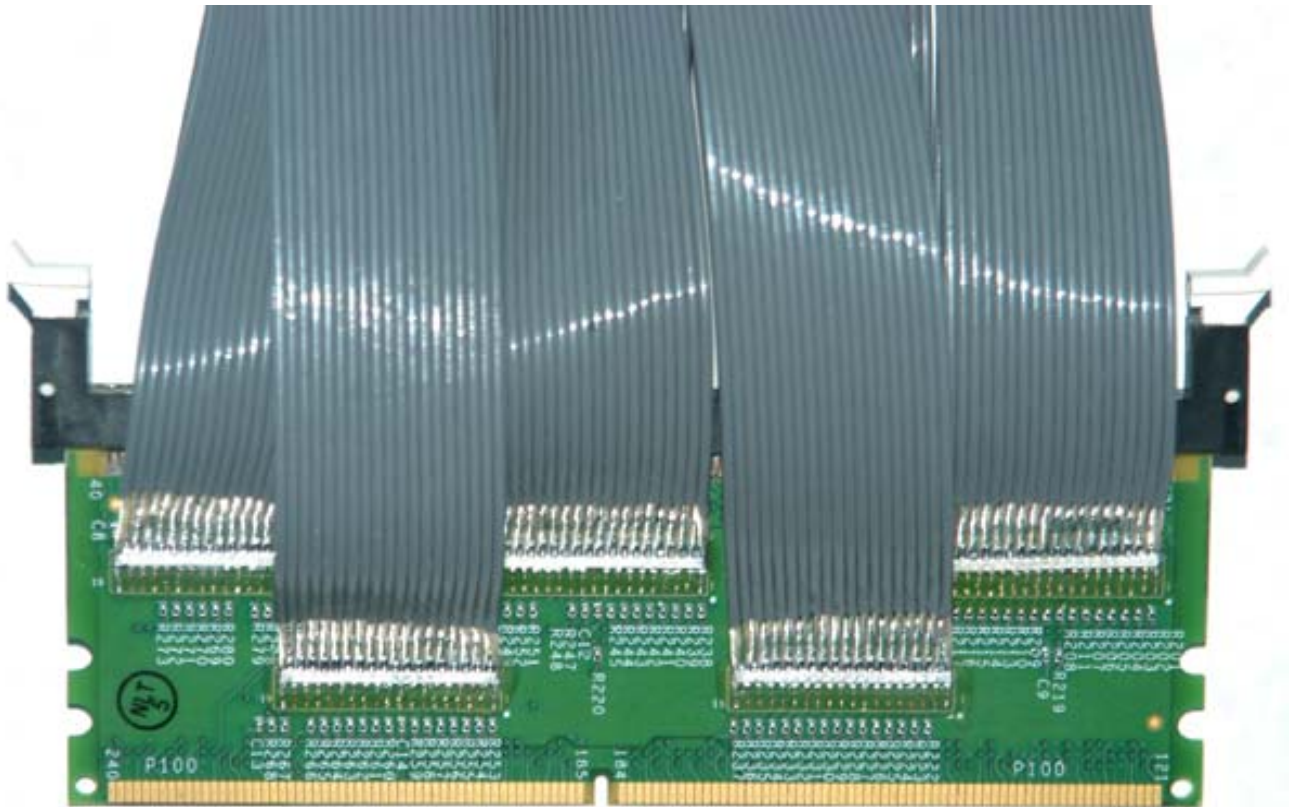

NEX-DDRII400DC



- Very short interposer with Straddle mount DDR2 connector and permanently attached Logic Analyzer probes for use in standard DDR2 DIMM targets that have very limited side-to-side access.
- Acquisition of DDR2-400MT/s Address/Command, Read and Write Data
- Quick and easy connection between the DIMM DDR2 bus and Tektronix Logic Analyzers
- Extender design does not require a dedicated slot
- Impedance controlled, matched trace length design
- No active buffering of the DDR signals
- Accurate 8GHz Timing Analysis
- Simultaneous State and Timing on every channel of the TLA
- Correlation with data acquired from other acquisition modules

General Description

NEX-DDR2400DC allows for the acquisition of Address/Command, Read and Write Data of 240-pin, Unbuffered or Registered DDR2 400 DIMMs.

Pre-Defined Symbols for the following Command Cycles allow for easy Trigger Setup:

- Read Col Address Read
- Write Col Address Write
- Mode Register Set
- Row Address Strobe
- Refresh
- Precharge
- Precharge Select Bank
- No Operation
- Ignore Command Data
- Burst Stop

Selective Clocking option stores valid cycles and significantly reduces the amount of Idle cycles acquired by the LA. This results in the LA capturing more information of interest and fewer unwanted Idle cycles.

Oscilloscope Connectivity to any channel without having to re-probe via the TLA's Enhanced iView Analog Mux capability.

Timing analysis available on all DDR2 signals.

Pre-defined Trigger setup for the following: Read Col Address Read, Write Col Address Write, Mode Register Set, Row Address Strobe, No Operation, Ignore Command Data, Burst Stop, Refresh, Precharge, and Precharge Select Bank.

The following support package has been included with the NEX-DDR2400DC adapter to support 400MT/s DIMM DDR2:

SDDR2-2A software package allows the user to acquire DDR2 400 Read **AND** Write data from a target. This support requires two merged TLA7AA4 or TLA7AB4 136-channel 450MHz state speed acquisition cards. No Logic Analyzer probes are necessary.

LA Support / Configuration

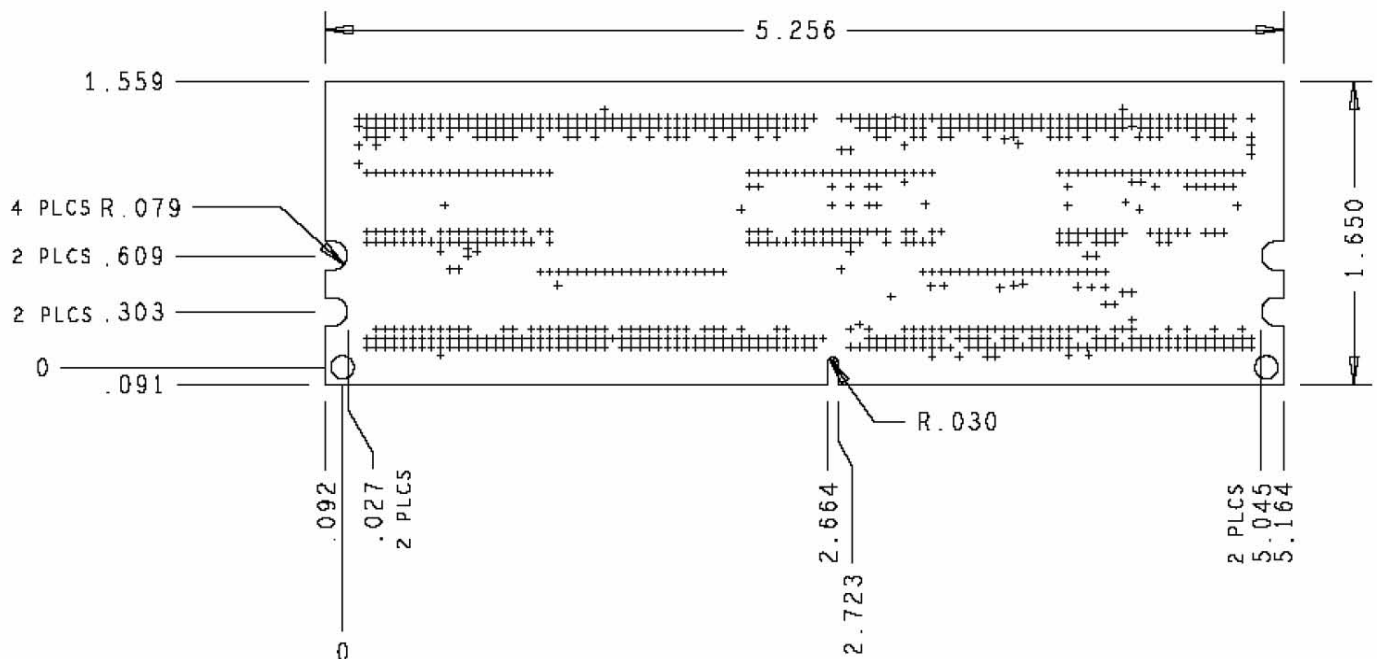
Acquisition Type	400 MHz	TLA7xx4 Module Count
Timing Only	X	2 - merged
Read and Write	X	2 - merged

A TLA700 equipped with two 450 MHz state speed acquisition module (TLA7AA4 or TLA7AB4 card) is required for DDR Read and Write Data acquisition. No probes are required.

8 GHz MagniVu Timing and Enhanced iView Analog Mux capabilities are available.

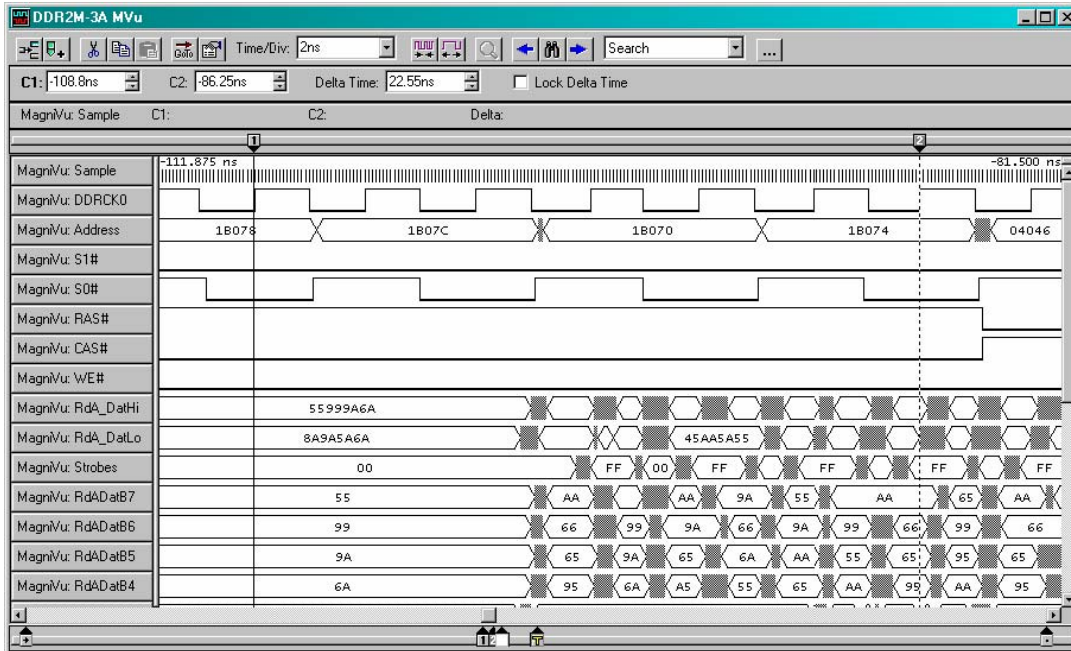
Mechanical Outline

Approximately 0.37" between DIMM-to-DIMM centers is required for probe clearances. Logic Analyzer connection is provided by probes that are permanently connected to both sides of the adapter.



NEX- DDR11400DC Mechanical Outline

Timing Display



DIMM DDRII 400 Timing Display

State Display

Sample	DDR2M-3A Address	Cmd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChckBits	DDR2M-3A DataMasks	Timestamp
42	04047	1A3	ACTV - ROW ADDRESS STROBE (S0#)	-----	-----	-----	-----	3.750 ns
43	-----	1AC	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
44	-----	1AC	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
45	-----	1AC	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (S0#)	-----	-----	-----	-----	3.750 ns
47	-----	1AC	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (S0#)	-----	-----	-----	-----	3.750 ns
49	-----	1AA	WRITE DATA	9A995A6A	8A65A595	40	00	3.750 ns
50	-----	1AA	WRITE DATA	9A995A6A	8A65A595	40	00	3.750 ns
51	-----	1AA	WRITE DATA	659995AA	8AA5A555	40	00	3.750 ns
52	-----	1AA	WRITE DATA	659995AA	8AA5A555	40	00	3.750 ns
53	-----	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
54	-----	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
55	-----	1AA	WRITE DATA	9A9AGAG5	45AA5A55	80	00	3.750 ns
56	-----	1AA	WRITE DATA	9A9AGAG5	45AA5A55	80	00	3.750 ns
57	04247	1A2	PRE - PRECHARGE SELECT BANK (S0#)	-----	-----	-----	-----	3.750 ns
58	-----	1AB	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
59	-----	1AB	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
60	-----	1AB	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
61	04247	1A3	ACTV - ROW ADDRESS STROBE (S0#)	-----	-----	-----	-----	3.750 ns
62	-----	1AD	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
63	-----	1AD	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
64	-----	1AD	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
65	1495F	1A5	READ - COL ADDR READ (S0#)	-----	-----	-----	-----	3.750 ns
66	-----	1AD	DESL - IGNORE COMMAND	-----	-----	-----	-----	3.750 ns
67	1495B	1A5	READ - COL ADDR READ (S0#)	-----	-----	-----	-----	3.750 ns
68	-----	1AD	READ DATA	00000180	00000022	00	-----	3.750 ns
69	14950	1A5	READ - COL ADDR READ (S0#)	-----	-----	-----	-----	3.750 ns
70	-----	1AD	READ DATA	659995AA	45AA5A55	90	-----	3.750 ns
			READ DATA	659995AA	45AA5A55	90	-----	3.750 ns
			READ DATA	55999A6A	4565A595	90	-----	3.750 ns
			READ DATA	55999A6A	4565A595	90	-----	3.750 ns

DIMM DDRII 400 State Display – Software Mode, Address, Data and Command Cycles Only

Ordering / Contact Information

Part Number NEX-DDR2DC400DC

Includes: NEX-DDR2DC400DC Adapter
Setup Software
Built in Logic Analyzer probes
Manual

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techsupport@nexustechnology.com

Website: www.nexustechnology.com

Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

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