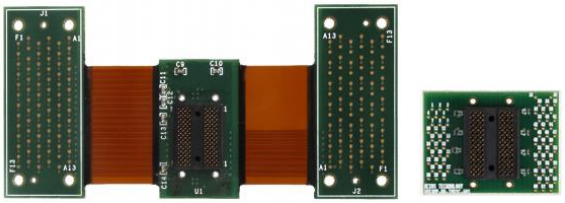
Target Socketed DDR3 Component Interposers

Premier DDR3 Component Digital & Analog Validation



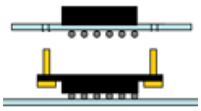
Nexus Technology recommends DDR3 component interposers for applications requiring optimal digital validation of speeds up to DDR3-2133, and analog validation of speeds up to DDR3-2133.

These interposers allow for logic analyzer and/or oscilloscope acquisition of command, address, read, and write data of x4, x8 and/or x16 DDR3 memory components at speeds up to DDR3-2133 for digital validation, and DDR3-2133 . Multiple logic analyzer component interposers can be used together to reconstruct up to 32-bit data buses.

Premier Component Interposer Design

Optimal DDR3 validation requires analysis of the DDR3 signals, as seen by the memory components. This allows for the highest confidence that the signals captured are representative, contain little interference, and present the maximum possible data eye size. Nexus Technology component interposers allow for logic analyzer and/or oscilloscope probing of the DDR3 signals extremely close to the memory components.

Probe Installation



The process of attaching the interposer to your target has been greatly simplified using Nexus Technology's patented, high-bandwidth, component interposer sockets. These patented sockets **completely remove the need to contract specialized rework houses** to perform the installation. Instead, our customers can use standard BGA assembly practices to install the component interposer socket. Further, Nexus Technology can perform the attachment service for a nominal fee.

Once the interposer socket is installed on the target, logic analyzer or oscilloscope interposers can easily be inserted or removed from the socket. This provides a reusable interface to your target system and completely removes any need to rework customer targets or our component interposers. Note that the interposer socket elevates the interposer above the adjacent BGAs to provide the mechanical clearance necessary for easy probe attachment.

DDR3 BGA Component Installation

A second socket for easy BGA memory component installation is also available for all Nexus Technology component interposers. These sockets are industry standard DDR3 BGA sockets and allow for the quick swapping & testing of different memory components on the interposer. The NEXVu Sockets Quick Start Guide provides more information and is available on our website.

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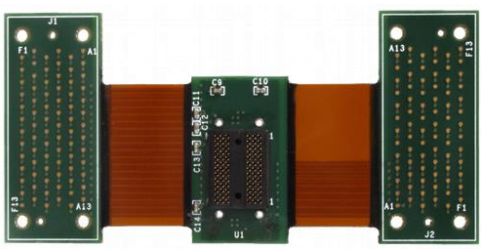
Logic Analyzer Component Interposers

Logic Analyzer Component Interposer Hardware



Connectivity and analysis to a logic analyzer are provided through x4, x8, and/or x16 logic analyzer memory component interposers. These controlled impedance, matched trace length interposers provide visibility up to 2,133MT/s (DDR3-2133) for digital validation using a logic analyzer. The rigid/flex/rigid design allows the interposer to be used in targets with little mechanical clearance around the target component. Two or four x4/x8 interposers can be used together to reconstruct 8-, 16-, or 32-bit data buses. Two x16 interposers can be used together to reconstruct 32-bit data buses.

Memory Compliance Analysis

Nexus Technology's Logic Analyzer Interposers are fully compatible with the Nexus Memory Compliance Analyzer (MCA) Instrument. Please contact Nexus for more information regarding the MCA Instrument.

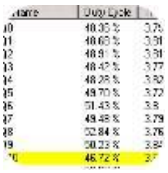
Logic Analyzer Component Interposer Software

All Nexus Technology logic analyzer component interposers come with the required logic analyzer setup software, DDR3 protocol decode software, DDR3 data eye sample point analysis software, and a limited version of the protocol violation software. Optional full protocol analysis is available separately. Optional software to decode multiple interposers is also available.

Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions for easy display and logic analyzer triggering/filtering.

Data Sample Point Analysis Software



In order for the logic analyzer to capture data, the DDR3 signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDR3 data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes are purposely skewed - as per the DDR3 specification - on a byte basis relative to the DDR clock. The valid eyes also contain skew (again relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

These, among other factors, make reliable and accurate DDR3 read and write data bus acquisition extremely difficult - if done manually. NEX-DDR3-SPA, provided free, automates this process enabling quick and reliable DDR3 read and write data bus acquisition in only minutes. For more information, please see the NEX-DDR3-SPA product page on our website.

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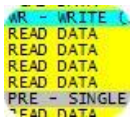
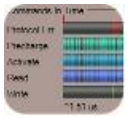
Protocol Violation Software

There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Full protocol violation analysis is available separately. Please see the NEX-DDR-PROTOCOL product for more information.

Logic Analyzer for Digital Validation



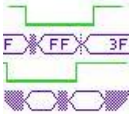
Logic analyzer setup software (TLA support package) is included with these products. This setup software acquires/reconstructs the 933MHz command/address bus and acquires/reconstructs the 2,133MT/s read write data from the data bus. The software also decodes and displays the bus protocol, shows the valid read/write data and provides easy DDR protocol triggering to quickly capture relevant data.



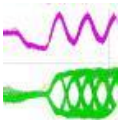
These products also come with a limited version of the NEX-DDR-PROTOCOL software tool. This software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs basic protocol violation checking. Advanced protocol violation checking is available for purchase separately. Please see the NEX-DDR-PROTOCOL product for more information on this powerful tool.

Logic Analyzer for Analog Validation

Although these logic analyzer interposers are designed for optimal digital validation, there are a number of useful features and tools available to assist in the analog validation process.



The most readily available tool is the Tektronix Logic Analyzer's 20ps (50GHz) MagniVu timing. This 2.5us deep acquisition space, separate from state acquisition memory is simultaneously acquired with state data, and is typically filled with bus activity that occurred around the state trigger. A wealth of analog information can be found in this data, including: positive/negative pulse widths, signal skew, and data glitches. Activity that appears too short, too long, unreasonably skewed relative to another signal, or that contains glitches are indications that there is an analog characteristic of that signal that deserves further attention.



Another powerful analog validation feature is the Tektronix Logic Analyzer's Analog Mux capability. When paired with an oscilloscope, this feature enables analog visibility of every DDR3 signal probed by the interposer. Any of the ten or so command bits, sixteen-plus address bits and any of the 4,8,16, or 32 data bits can be viewed on an oscilloscope in seconds and - literally - with a touch of a button. This feature comes with two significant limitations. First, there is no calibration specification for the channel-to-channel skew through the Analog Mux. Second, the signals are bandwidth limited to 3GHz. This limitation acts as a high speed filter, limiting the visibility of the signal's harmonics that are over 3GHz. For DDR3-2133, this filtering will cause artificial increases in the slew rates which appear as rising/falling edges that take longer to transition. The effect on the data eyes will be similar, showing a rounding effect. Although these limitations force the user to find alternate methods for accurate DDR3-2133 analog validation, the importance of this tool for preliminary analog validation cannot be understated. The ability of a digital validation engineer to

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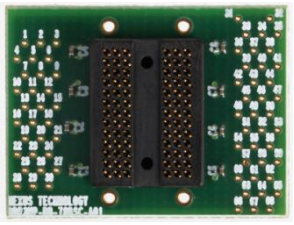
quickly and easily assess the general analog health of a target can save an enormous amount of time and resources.

Tektronix discusses some of these topics in more detail in the application note, Debugging Timing Problems with a Logic Analyzer available for download from tek.com. Nexus Technology recommends these products for the debugging methods and practices described in this application note.

Oscilloscope Component Interposers

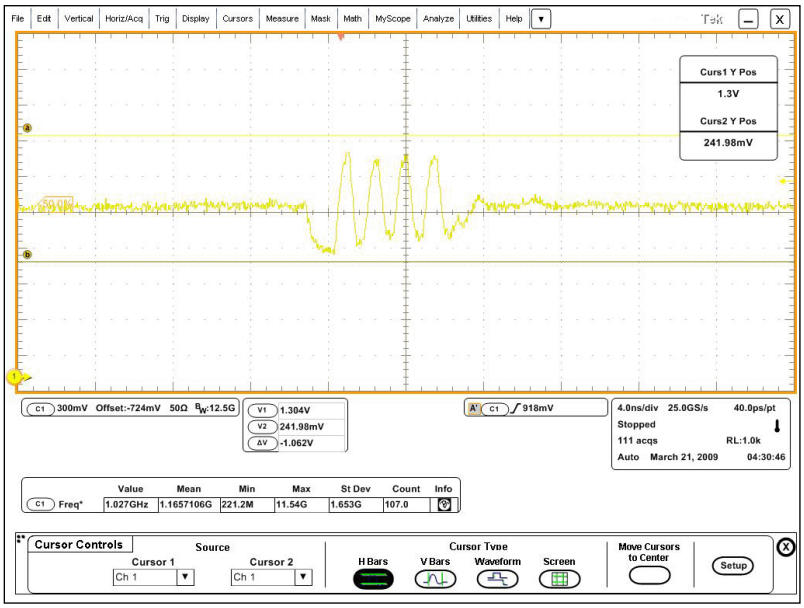
Oscilloscope Component Interposer Hardware



Connectivity and analysis to an oscilloscope are provided through x4, x8, and/or x16 oscilloscope memory component interposers. These controlled impedance, matched trace length interposers provide visibility up to 2,133MT/s (DDR3-2133) for analog validation using a oscilloscope. All signals are brought out to pads that are designed to accommodate Tektronix solder down probe tips. Probe adapters can also be used to easily move the oscilloscope probe between signals for quick and accurate measurement.

Oscilloscope Analog Validation

Filter software, available from Tektronix for use with select Tektronix oscilloscopes, removes the effect of the oscilloscope interposer. Although these interposers are designed to optimize signal integrity, this feature removes even the slightest effect the adapter has from the oscilloscope display.



Strobe as Seen using the Oscilloscope Component Interposer

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Nexus Technology's Component Interposer Advantages

Probed at the BGA Balls

The best place to probe to eliminate reflections associated with standard embedded DDR3 mid bus probing or other methods. Interposers require no target footprints or special routing requirements that mid-bus probing requires.

Use with Existing Embedded Designs or DIMMs

No need to change existing designs. Simply add the interposer to your embedded target or DIMM with no re-design or added probe points.

Socket Design

The interposers are reusable. Once an interposer socket is installed, the interposer can be attached and removed by hand - allowing the interposer to be used on multiple targets quickly or allowing quick swapping of logic analyzer and oscilloscope interposers on the same target.

Support for DDR3 x4, x8, and x16 Memory Devices

Full coverage for DDR3 applications at speeds up to 2,133MT/s (DDR3-2133) for digital validation, and 2,133MT/s(DDR3-2133) for analog validation.

Easy to Install

By either adding the interposer socket using industry standard BGA attachment methods or by using Nexus Technology's attachment service.

Separate Oscilloscope & Logic Analyzer Products

Each interposer is designed for optimal signal integrity for use with an oscilloscope or logic analyzer.

Simple Digital & Analog Validation Via Standard Interposer Socket

The easy to install interposer socket can be used with both the oscilloscope and logic analyzer interposers for maximum flexibility and very quick analog and digital validation.

Oscilloscope Interposer Software

Oscilloscope filter software removes effects of the interposer. Available from Tektronix.

Logic Analyzer Software

Standard logic analyzer software includes: setup software, DDR3 protocol decode software, DDR3 data eye sample point analysis software, and protocol violation software.

Interposer Retention to the Target

The interposer socket has four posts that are soldered to four mounting holes on the interposer. This ensures the interposer will not be mistakenly pulled off the socket attached to the target.

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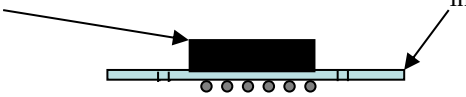
Attaching & Reusing Interposers

Standard DDR3 socket on interposer, ready for memory component insertion. Also available without this socket.

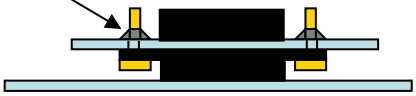
Memory component interposer. Balls on the bottom simply push into the custom socket on the target.



Component interposer socket installed.

Target board

After pressing the socket to the interposer, solder should be added to mechanically retain the interposer to the custom socket



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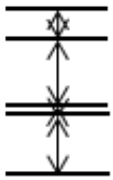
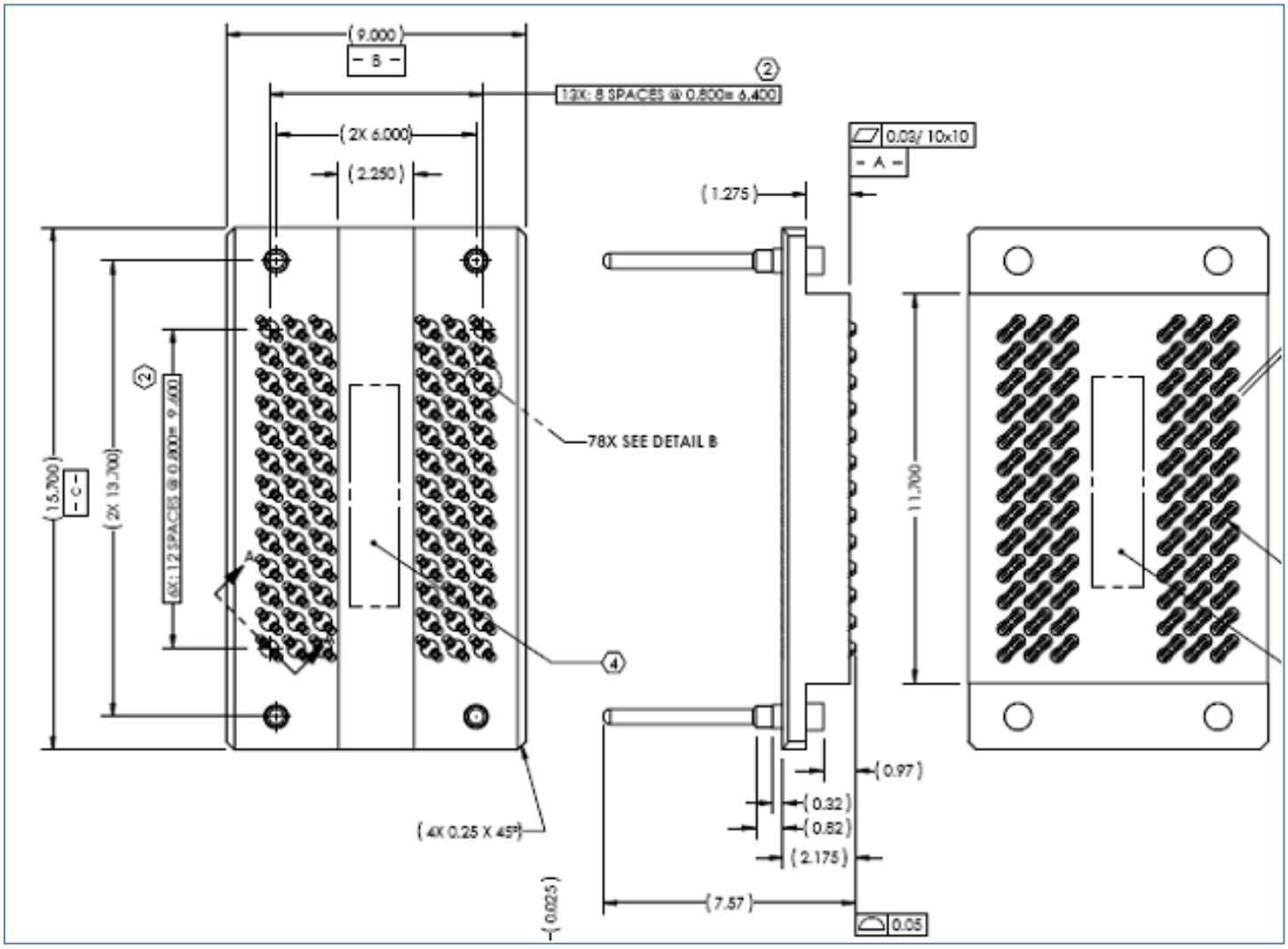
Product Dimensions



0.033" (0.84mm) Memory Component (ave)
0.08" (2.03mm) Memory Socket
0.066" (1.68mm) Interposer Board
0.086" (2.18mm) from board under test to bottom of Interposer

DDR3 Full Installation Height



DDR3 x4/x8 Target Socket Dimensions

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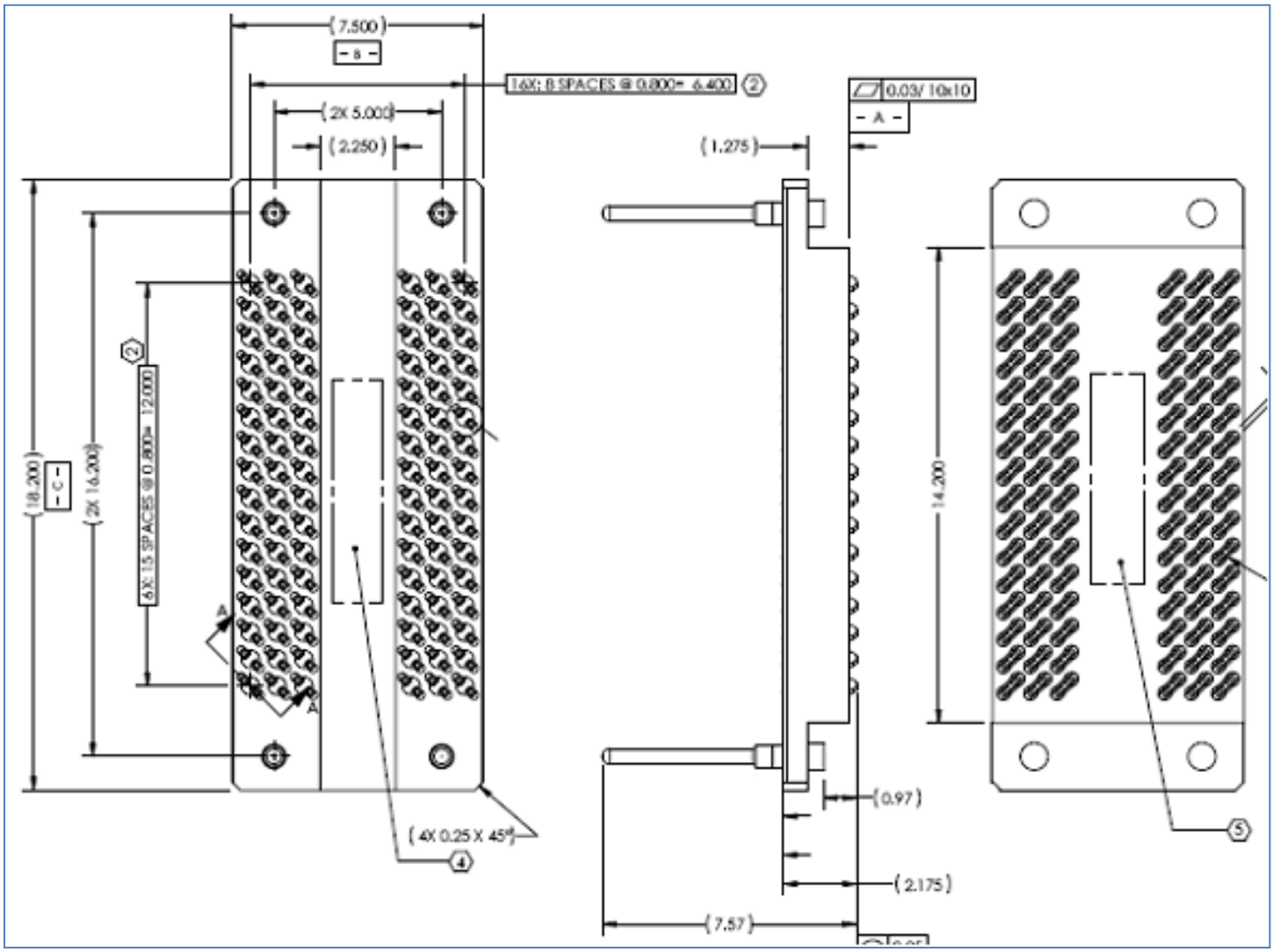

DDR3 x16 Target Socket Dimensions

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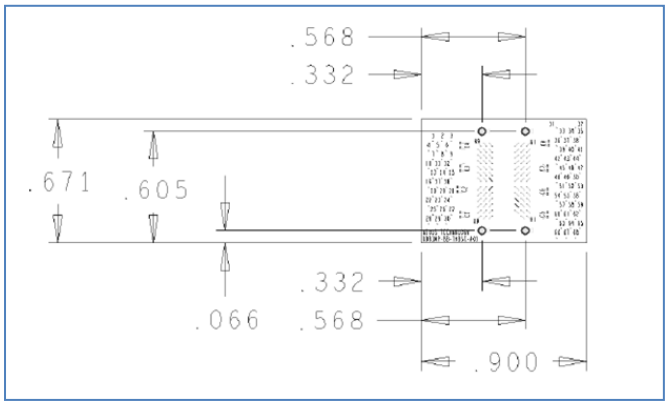
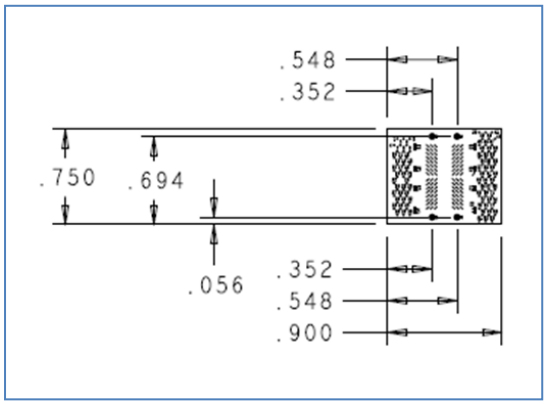
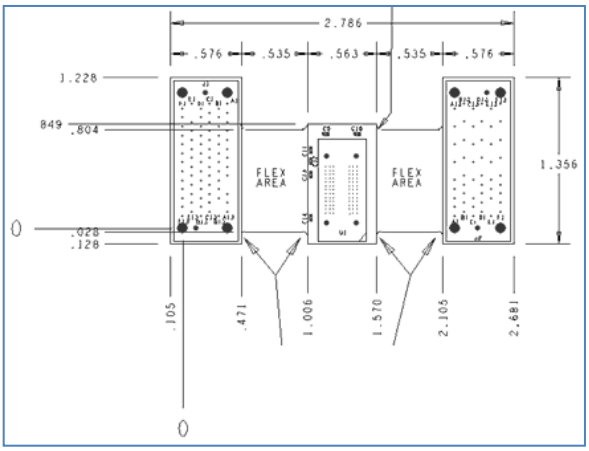


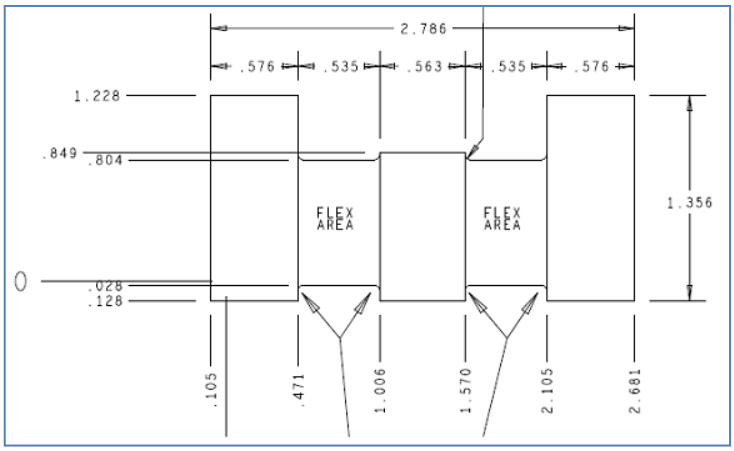
DDR3 x4/x8 Socketed Oscilloscope Interposer Dimensions



DDR3 x16 Socketed Oscilloscope Interposer Dimensions



DDR3 x4/x8 Socketed Logic Analyzer Interposer Dimensions



DDR3 x16 Socketed Logic Analyzer Interposer Dimensions

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Product Configuration Tables

DDR3 Oscilloscope Interposers

Nomenclature	Interposer Type	Data Width	DDR Speed	Component Socket Included	Installation Service Included
NEX-DDR3MP78BSCSK	Oscilloscope	x4/x8	DDR3-2133	Yes	No
NEX-DDR3MP78BSCSK-AT	Oscilloscope	x4/x8	DDR3-2133	Yes	Yes
NEX-DDR3MP78BSC	Oscilloscope	x4/x8	DDR3-2133	No	No
NEX-DDR3MP78BSC-AT	Oscilloscope	x4/x8	DDR3-2133	No	Yes
NEX-DDR3MP96BSCSK	Oscilloscope	x16	DDR3-2133	Yes	No
NEX-DDR3MP96BSCSK-AT	Oscilloscope	x16	DDR3-2133	Yes	Yes
NEX-DDR3MP96BSC	Oscilloscope	x16	DDR3-2133	No	No
NEX-DDR3MP96BSC-AT	Oscilloscope	x16	DDR3-2133	No	Yes

DDR3 Logic Analyzer Interposers

Nomenclature	Interposer Type	Data Width	DDR Speed	Component Socket Included	Nexus Probes Included Note 1	Installation Service Included	Hardware Requirements
NEX-DDR3MP78BLASK	Logic Analyzer	x4/x8	DDR3-2133	Yes	No	No	1- TLA7000 Series Mainframe 1- TLA7BB4 1.4GHz (or 1-TLA7BB2/4 750MHz for up to DDR3-1333) See Note 2
NEX-DDR3MP78BLASK-AT	Logic Analyzer	x4/x8	DDR3-2133	Yes	No	Yes	
NEX-DDR3MP78BLASKPR	Logic Analyzer	x4/x8	DDR3-2133	Yes	Yes	No	
NEX-DDR3MP78BLASKPR-AT	Logic Analyzer	x4/x8	DDR3-2133	Yes	Yes	Yes	
NEX-DDR3MP78BLA	Logic Analyzer	x4/x8	DDR3-2133	No	No	No	
NEX-DDR3MP78BLA-AT	Logic Analyzer	x4/x8	DDR3-2133	No	No	Yes	
NEX-DDR3MP78BLAPR	Logic Analyzer	x4/x8	DDR3-2133	No	Yes	No	
NEX-DDR3MP78BLAPR-AT	Logic Analyzer	x4/x8	DDR3-2133	No	Yes	Yes	
NEX-DDR3MP96BLASK	Logic Analyzer	x16	DDR3-2133	Yes	No	No	
NEX-DDR3MP96BLASK-AT	Logic Analyzer	x16	DDR3-2133	Yes	No	Yes	
NEX-DDR3MP96BLASKPR	Logic Analyzer	x16	DDR3-2133	Yes	Yes	No	
NEX-DDR3MP96BLASKPR-AT	Logic Analyzer	x16	DDR3-2133	Yes	Yes	Yes	
NEX-DDR3MP96BLA	Logic Analyzer	x16	DDR3-2133	No	No	No	
NEX-DDR3MP96BLA-AT	Logic Analyzer	x16	DDR3-2133	No	No	Yes	
NEX-DDR3MP96BLAPR	Logic Analyzer	x16	DDR3-2133	No	Yes	No	
NEX-DDR3MP96BLAPR-AT	Logic Analyzer	x16	DDR3-2133	No	Yes	Yes	

Note 1: Two Nexus Technology NEX-PRB1XL probes can be used at/up to DDR3-1333 and can be ordered as a complete package as shown in the table above. One Tektronix P6960HCD probe and One NEX-PRB1XL proe are required for DDR3>1333. The P6960HCD probe must be purchased from Tektronix.
Note 2: When using TLA7BB2 or TLA7BB4 module(s) to acquire DDR3 data up to DDR3-1333, the module can have either the 750MHz or 1.4GHz state speed option. When acquiring DDR3>1333, the TLA module must have the 1.4GHz state speed option.

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DDR3 Logic Analyzer Interposers – Optional Extended Data Bus (Multi-Interposer) Support

Nomenclature	Interposer Type	Data Width	DDR Speed (max)	Component Interposer Count	Data Bus Width	Tektronix Hardware Requirements	Nexus Hardware Requirements
NEX-MCI13x8-16-16SW	Logic Analyzer	x8	DDR3-2133	2	16-bit	1- TLA7000 Series Mainframe 2- TLA7BB4 1.4GHz 3- P6960HCD	2- x4/x8 TLA Component Interposers See Note 3
NEX-MCI13x8-32-16SW	Logic Analyzer	x8	DDR3-2133	4	32-bit	1- TLA7000 Series Mainframe 3- TLA7BB4 1.4GHz 5- P6960HCD	4- x4/x8 TLA Component Interposers See Note 3
NEX-MCI13x8-16-13SW	Logic Analyzer	x8	DDR3-1333	2	16-bit	1- TLA7000 Series Mainframe 1- TLA7BB4 750MHz/1.4GHz	2- x4/x8 TLA Component Interposers 3- NEX-PRB1XL See Note 3
NEX-MCI13x8-32-13SW	Logic Analyzer	x8	DDR3-1333	4	32-bit	1- TLA7000 Series Mainframe 3- TLA7BB4 750MHz/1.4GHz	4- x4/x8 TLA Component Interposers 5- NEX-PRB1XL See Note 3
NEX-MCI13x16-32-16SW	Logic Analyzer	x16	DDR3-2133	2	32-bit	1- TLA7000 Series Mainframe 2- TLA7BB4 1.4GHz 3- P6960HCD	2- x16 TLA Component Interposers See Note 3
NEX-MCI13x16-32-13SW	Logic Analyzer	x16	DDR3-1333	2	32-bit	1- TLA7000 Series Mainframe 1- TLA7BB4 750MHz/1.4GHz	2- x16 TLA Component Interposers 3- NEX-PRB1XL See Note 3

Note 3: Optional support for multiple logic analyzer component interposers requires different hardware requirements than may be included with the DDR3 Logic Analyzer Interposer packages listed. Please review the included hardware for the package(s) selected and ensure that the packages include the hardware needed. We are available to help determine the correct configuration for your application. Please contact us if you need assistance.

Optional Additional Component Interposer Sockets

Nomenclature	Data Width	Solder Balls Added	Quantity of Sockets
NEX-DDR378BGASKBA	x4/x8	Yes	1
NEX-DDR378BGASKBA-3	x4/x8	Yes	3
NEX-DDR396BGASKBA	x16	Yes	1
NEX-DDR396BGASKBA-3	x16	Yes	3

Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST.

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