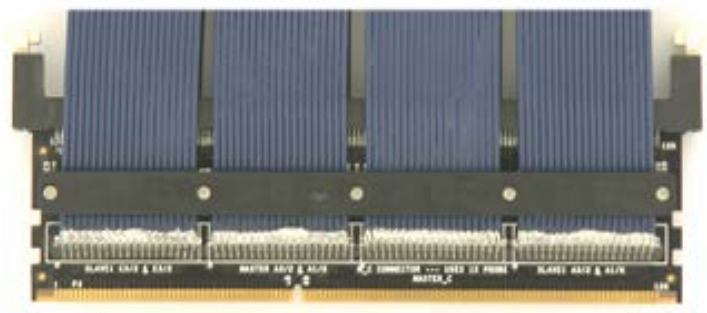
DDR3-1333 DIMM Slot Interposer

Flexible Digital Validation

- Passive 240-pin DIMM Slot Interposer
- Supports up to DDR3-1333
- Passive 50% Module Reduction w/MR Technology™
- Automated Logic Analyzer Setup
- DDR3 Protocol Violation Analysis
- Supports JEDEC PC3-10600, PC3-8500, and PC3-6400 DDR3 modules



Passive Module Reduction (MR) Technology™

Nexus Technology's Module Reduction Technology™ is available with this interposer. Products implementing MR Technology™ allow for full acquisition, including read and write data, while cutting the hardware requirements in half.

Module Reduction Technology™ is a software solution. No qualifier sideband signals are required and no active circuitry is implemented in MR Technology™ which would otherwise force double-probing and increase the load on the DDR3 target.

Interposer Design

Nexus Technology recommends DDR3 slot interposers for applications where the customer must have the greatest flexibility in the probing of different DDR3 DIMMs.

This interposer is an extender design and does not require a dedicated DIMM slot. The logic analyzer connects above the normal DIMM height so that there is no mechanical interference with adjacent DIMMs.

This is a passive interposer with no added buffers to conceal system performance.

Software

This DDR3-1333 DIMM slot interposer comes with logic analyzer setup software, DDR3 protocol decode software, DDR3 data eye sample point analysis software, and protocol violation software.

Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions for easy display and logic analyzer triggering/filtering.

Data Sample Point Analysis Software

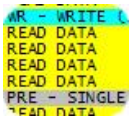
In order for the logic analyzer to capture data, the DDR3 signals must be digitized. For the command and address bus, this process is relatively straightforward as the center of the valid data eyes align with rising edge of the DDR clock. For the DDR3 data bus signals, the process of determining the optimal sample position for digitization is much more complicated. The valid eyes are purposely skewed - as per the DDR3 specification - on a byte basis relative to the DDR clock. The valid eyes also contain skew (again relative to the DDR clock) on a bit basis due to unavoidable artifacts of high-speed designs and the timing variations caused by the digitizing of the signals based on the threshold.

These, among other factors, make reliable and accurate DDR3 read and write data bus acquisition extremely difficult - if done manually. NEX-DDR3-SPA, provided free, automates this process enabling quick and reliable DDR3 read and write data bus acquisition in only minutes. For more information, please see the NEX-DDR3-SPA product for more information.

Protocol Violation Software

There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Please see the NEX-DDR-PROTOCOL product for more information.

Digital Validation

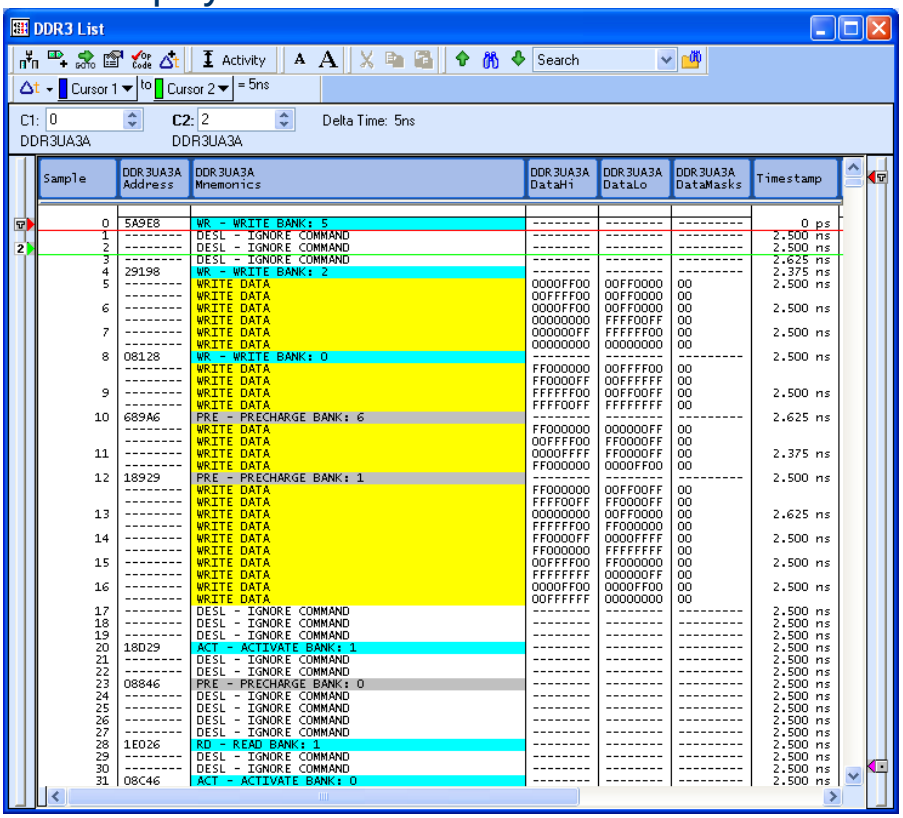


Logic analyzer setup software (TLA support package) is included with these products. This setup software acquires/reconstructs the 667MHz command/address bus and acquires/reconstructs the 1,333MT/s read write data from the data bus. The software also decodes and displays the bus protocol, shows the valid read/write data and provides easy DDR protocol triggering to quickly capture relevant data.

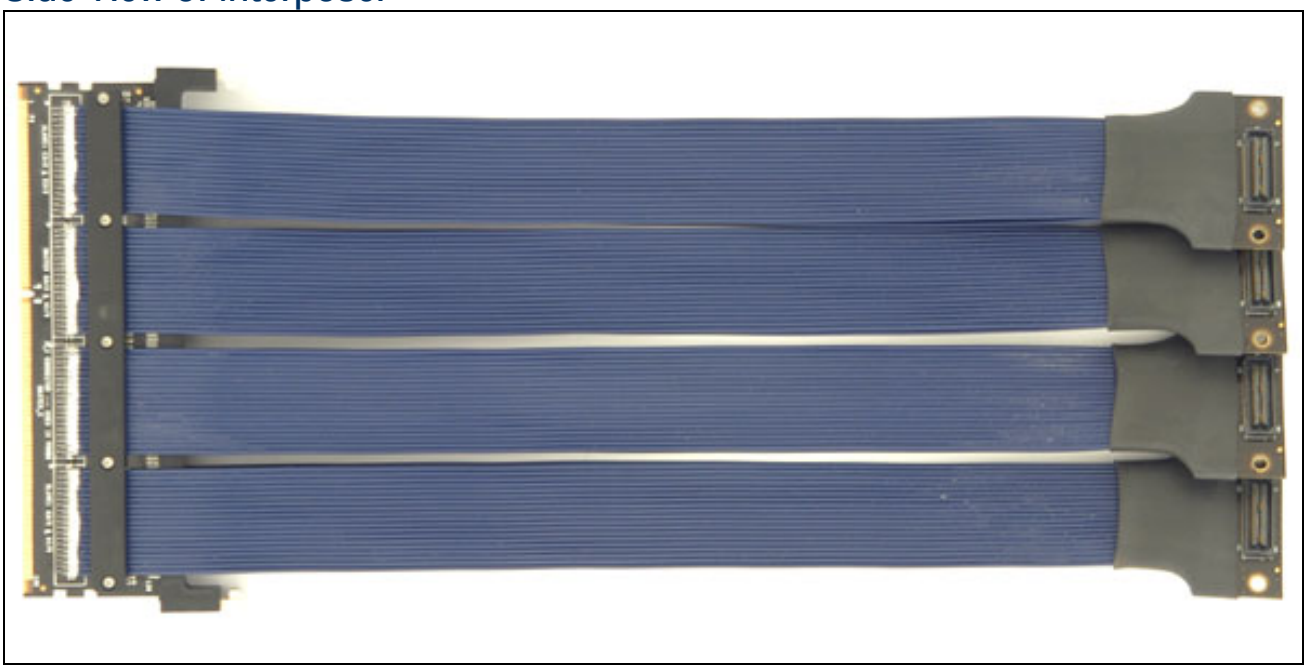
These products also come with the NEX-DDR-PROTOCOL software tool. This software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs basic protocol violation checking. Advanced protocol

violation checking is available for purchase separately. Please see the NEX-DDR-PROTOCOL product for more information on this powerful tool.

State Display of DDR3 Protocol & Data



Side View of Interposer



Hardware/Software Configurations

DDR Speed	Acquisition	Mainframe Required	Module(s) Required	Probes Required
DDR3-1333 DDR3-1067 DDR3-800	Cmd/Address Read **and** Write	TLA7000	1- TLA7BB4 750MHz (or 1.4GHz)	4- Nexus NEX-PRB1X-T

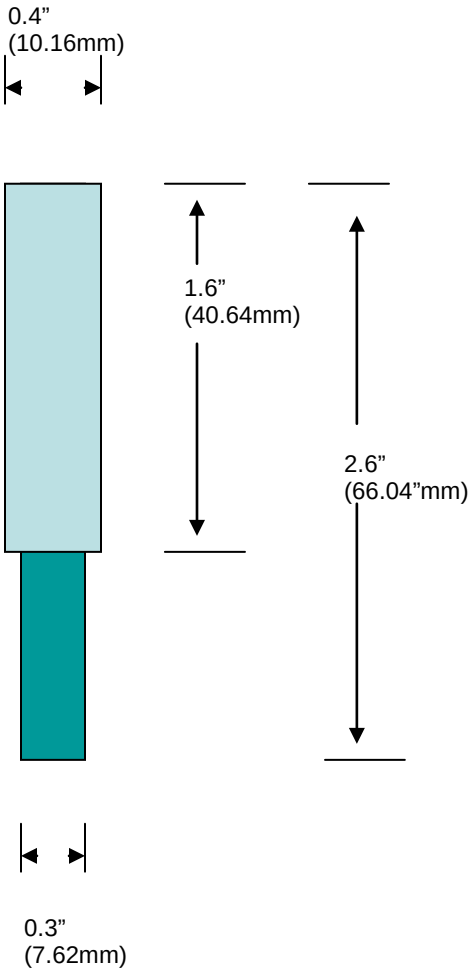
Product Configuration Table

Nomenclature	Nexus Probes Included	Nexus Hardware Included	Nexus Software Included
NEX-DDR3INTR-THIN	No – Note 1	1- DDR3-1333 DIMM Slot Interposer	1- TLA Setup & Protocol Decode Support Packages w/MR™ Technology 1- NEX-DDR3SPA Data Threshold & Sample Point Analysis 1- NEX-DDR-PROTOCOL Protocol Violation
NEX-DDR3INTR-THIN-PR2	Yes – Note 1	1- DDR3-1333 DIMM Slot Interposer 4- NEX-PRB1X-T	1- TLA Setup & Protocol Decode Support Packages w/MR™ Technology 1- NEX-DDR3SPA Data Threshold & Sample Point Analysis 1- NEX-DDR-PROTOCOL Protocol Violation

Note 1: Four Nexus Technology NEX-PRB1X-T are required and can be ordered as a complete package as shown in the table above.

Product Keep-out Area

Does not include user DIMM height.



Further Information

Please contact us by telephone, email or mail as listed below. Email is preferred. Normal business hours are 9:00 - 5:00 EST.

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NEXUS TECHNOLOGY

Tektronix Embedded Systems Tools Partner