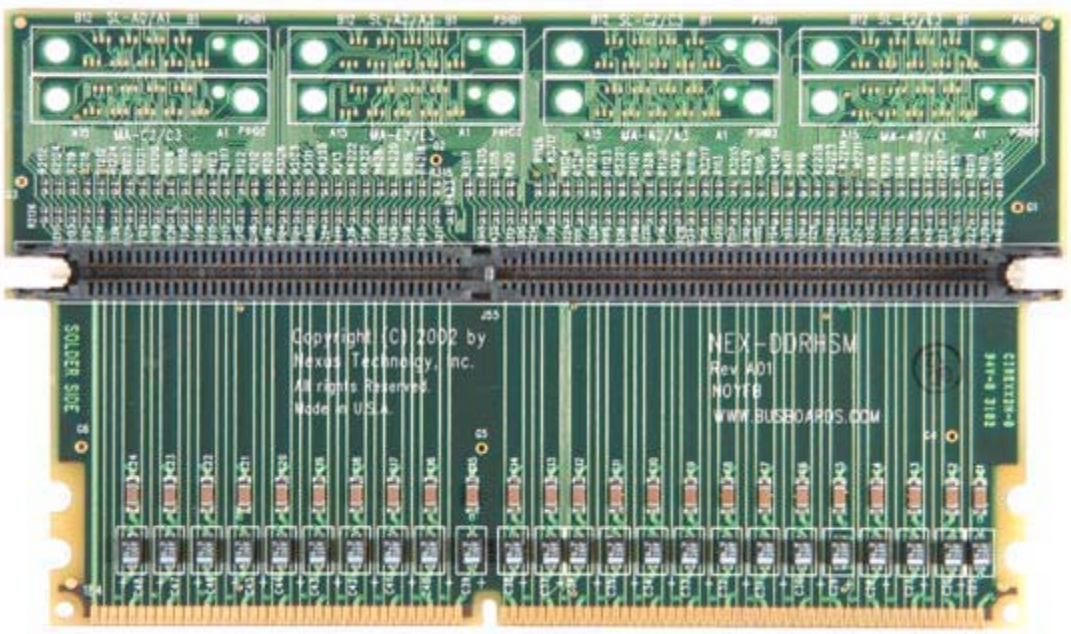
NEXUS TECHNOLOGY

DDR 400MHz Bus Analysis Probe and Software

NEX-DDRHSM



- Mirrored design of NEX-DDRHS product that provides the ability to simultaneously monitor two DDR sockets in a target
- Acquisition of DDR400/333/266/200, Address/Command, Read and Write data
- Quick and easy connection between the DDR bus and a Tektronix Logic Analyzer
- Extender design does not require a dedicated slot
- Selective Clocking reduces acquisition of idle cycles, saving acquisition memory
- Supports 184-pin DDR SDRAM DIMMs
- Impedance controlled, matched trace length design
- No active buffering of the DDR signals
- Accurate 8GHz timing analysis
- Simultaneous State and Timing on every channel of the TLA
- Trigger on Setup/Hold violations
- Correlation with data acquired from other acquisition modules
- Use the TLA's Extended iView capabilities to view any channel on an oscilloscope without re-probing
- Monitor an adjacent DDR socket simultaneously using an NEX-DDRHS adapter.

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General Description

NEX-DDRHSM allows for the acquisition of Address/Command, Read and Write data of 184-pin, unbuffered or registered DDR400/333/266/200 DIMMs.

NEX-DDRHSM is a mirror of the NEX-DDRHS product that places the DDR socket and probe footprints on the solder side of the board. Since the NEX-DDRHS places the DDR socket and probe footprints on the component side of the adapter, the NEX-DDRHS and NEX-DDRHSM can both be used in the target at the same time without mechanical interference. This provides the ability to simultaneously monitor two DDR slots in a design.

8Ghz Timing Analysis available for all DDRII signals

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Oscilloscope Connectivity on any channel without re-probing via the TLA's Enhanced iView Analog Mux capability

Selective Clocking stores data when commands are present and for 13 clock cycles after Column Address Assertion. This results in fewer Idle cycles being stored in acquisition memory.

Pre-Defined Symbols for the following Command Cycles allow for easy Trigger Setup:

- Read Col Address Read
- Write Col Address Write
- Mode Register Set
- Row Address Strobe
- No Operation
- Ignore Command Data
- Burst Stop
- Refresh
- Precharge
- Precharge Select Bank

No Dedicated Slot Required – The logic analyzer connects above the normal DIMM height so that there is no interference with adjacent DIMMs.

LA Support / Configuration

TLA7XX Series Logic Analyzer

- TLA Application Software V4.2 or later
- 1-2 TLA7AA4 or TLA7AB4, 136-channel acquisition modules with the 450 MHz State Clocking Option (see table below)
- 8 P6860 probes

Acquisition Type	200MHz DDR Bus	266MHz DDR Bus	333MHz DDR Bus	400MHz DDR Bus	TLA7xx4 Module Count	Merged Modules
Timing Only	X	X	X	X	1	
Read or Write	X	X	X	X	1	
Read and Write	X	X	X	X	2	X

8 GHz MagniVu timing and Enhanced iView Analog Mux capabilities are available.

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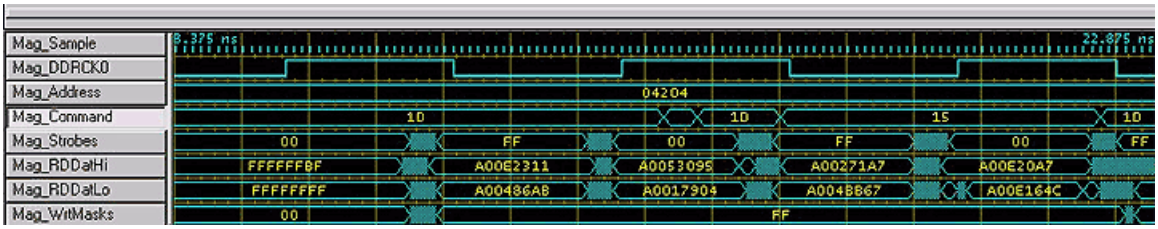
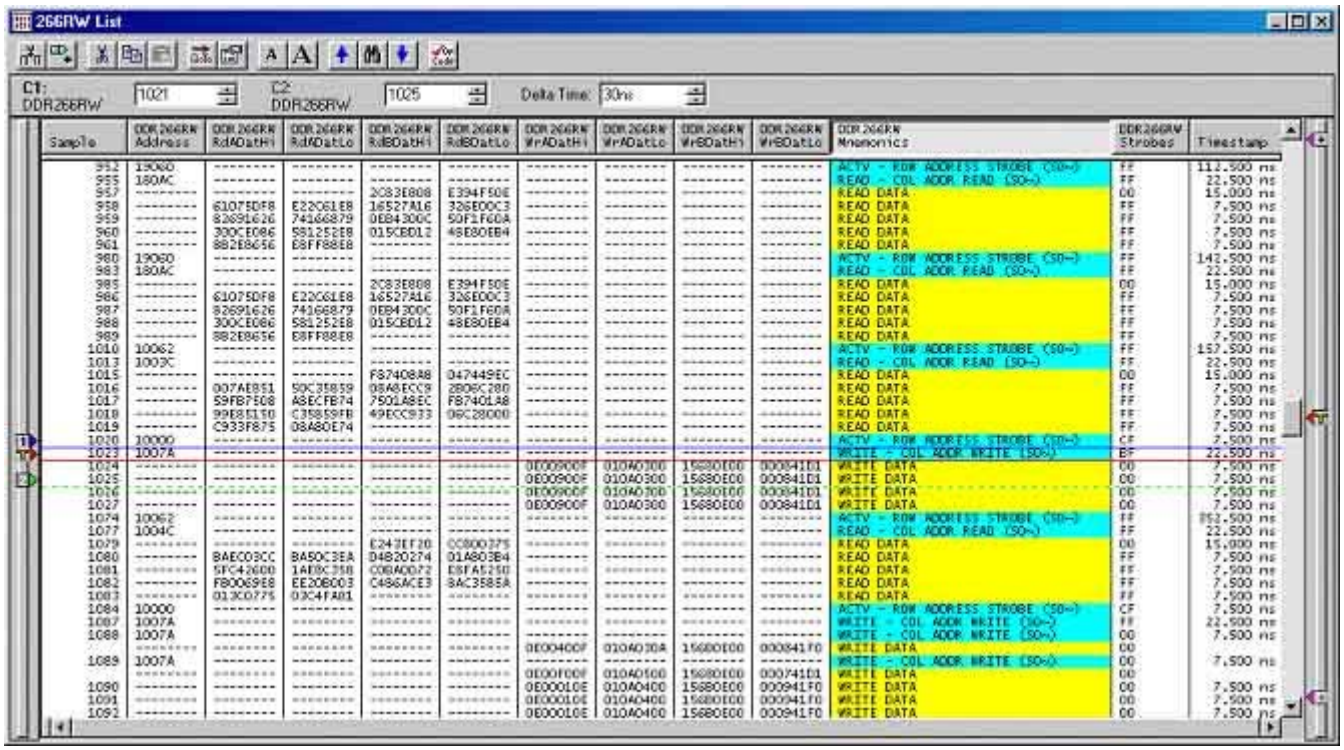
Timing Display



DDR Timing Display at 400MHz

State Display



DDR State Display

Sample	DDRHSMRW Address	DDRHSMRW RDDatHi	DDRHSMRW RDDatLo	DDRHSMRW WRDatHi	DDRHSMRW WRDatLo	DDRHSMRW Mnemonics
	00000	00000000	00000000	00000000	00000000	Normal Operation
	00000	00000000	00000000	00000000	00000000	Latency = Reserved
	00000	00000000	00000000	00000000	00000000	Burst Type = Sequential
	00000	00000000	00000000	00000000	00000000	Burst Length = Reserved
7534	04000	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	MRS - MODE REGISTER SET (SO~)
	04000	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Reserved
7535	00100	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	MRS - MODE REGISTER SET (SO~)
	00100	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Normal MRS
	00100	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Normal Operation / Reset DLL
	00100	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Latency = Reserved
	00100	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Burst Type = Sequential
	00100	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Burst Length = Reserved
7536	0006A	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	MRS - MODE REGISTER SET (SO~)
	0006A	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Normal MRS
	0006A	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Normal Operation
	0006A	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Latency = 2.5
	0006A	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Burst Type = Interleaved
	0006A	FFFFFFBF	FFFFFFFF	FFFFFFBF	FFFFFFFF	Burst Length = 4

DDR400 MRS Cycle

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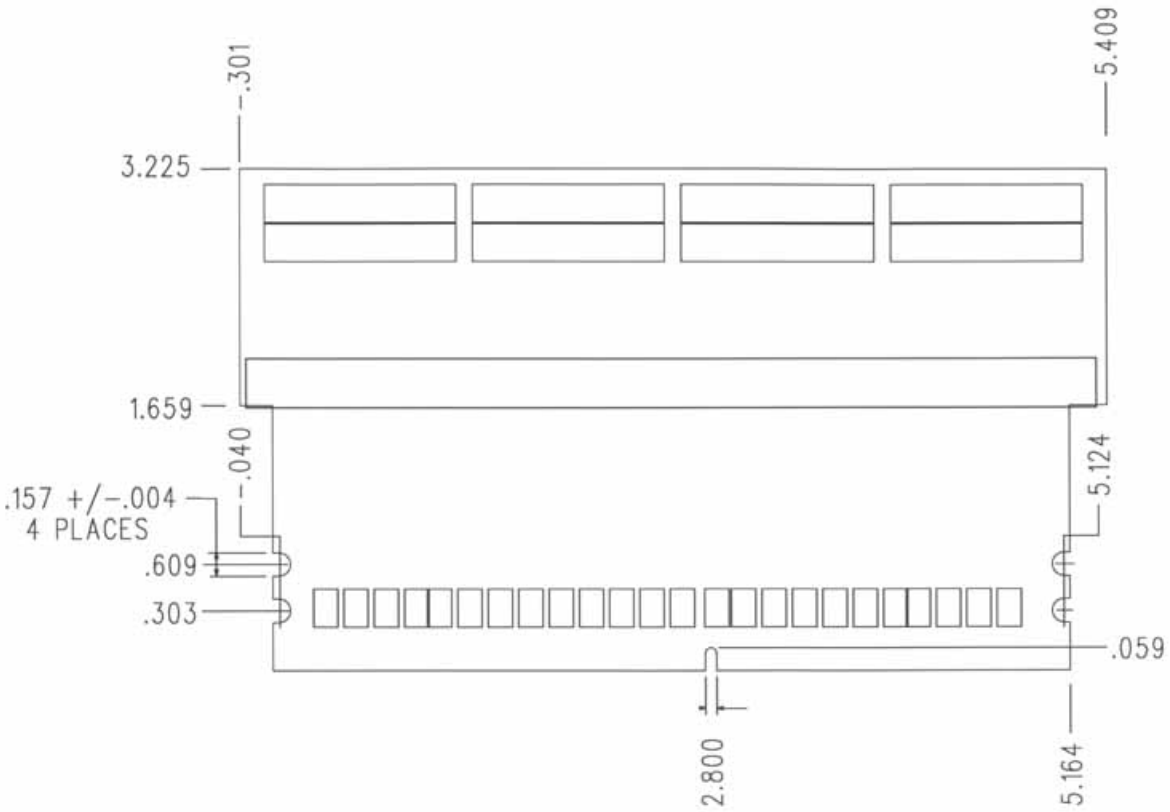
Mechanical Outline



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Ordering / Contact Information

Part Number NEX-DDRHSM
Includes: NEX-DDRHSM adapter
DDRHS-RW & DDRHS Support Software
NEX-DDRSPA software
Manual

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Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

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