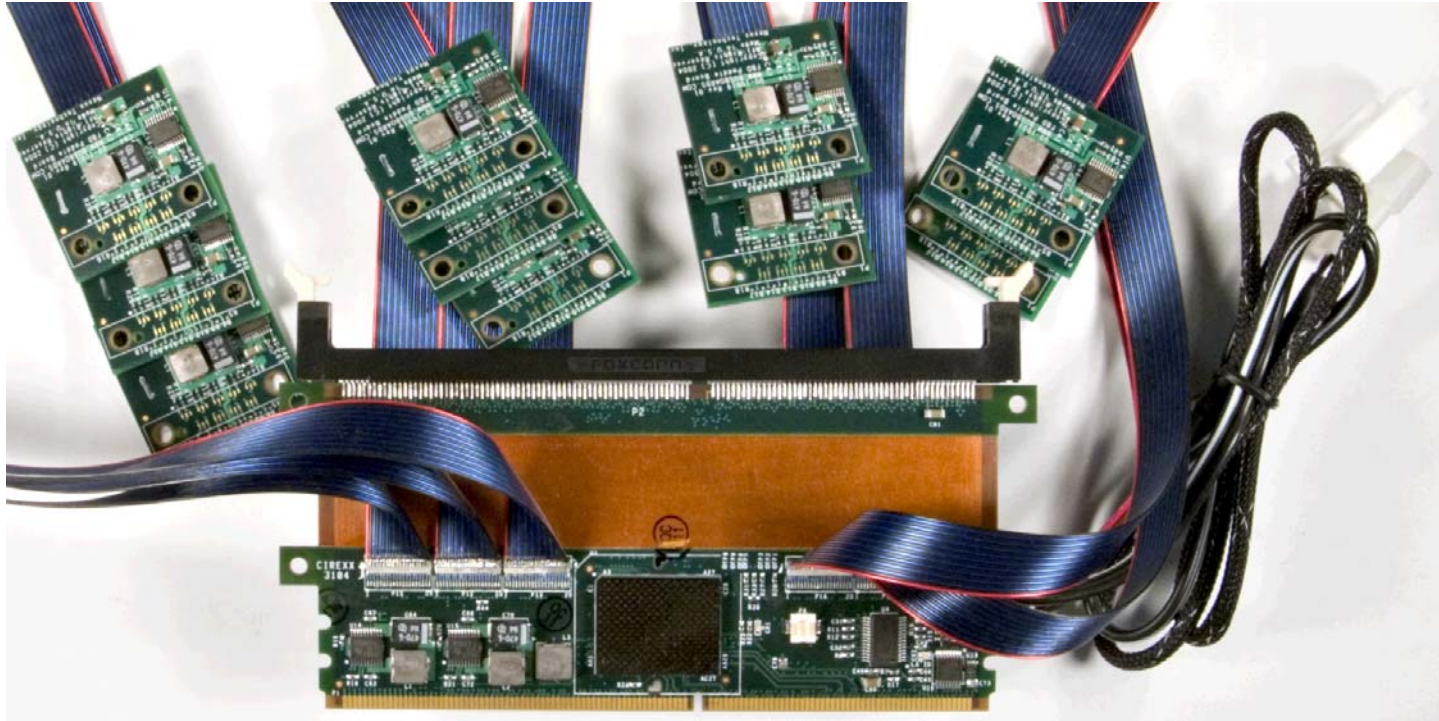

NEX-FBDLAI_x

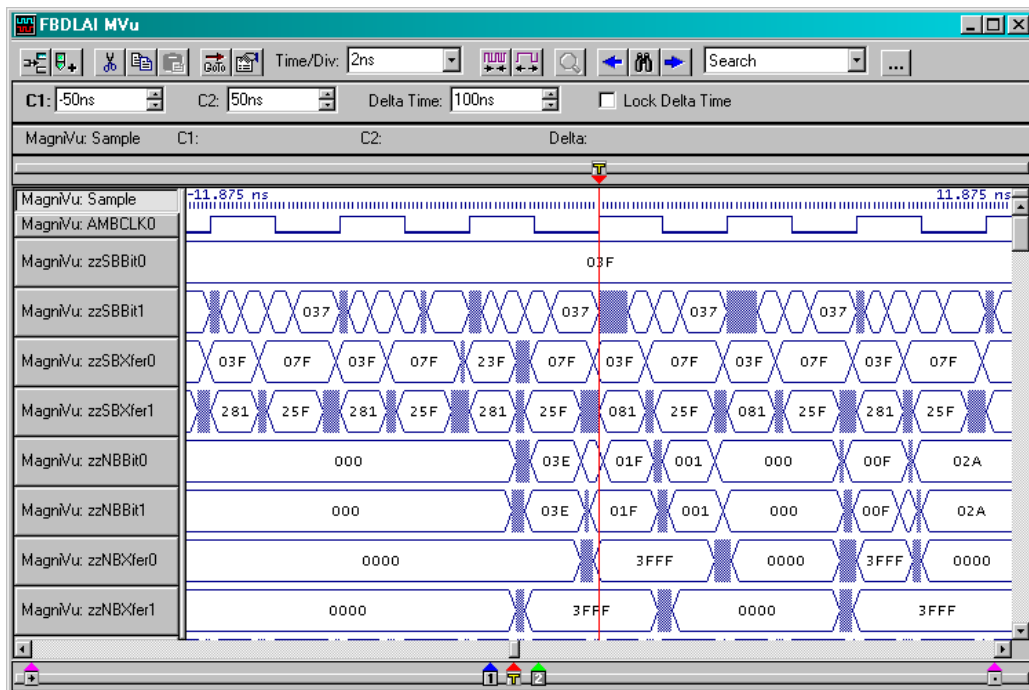


- The NEX-FBD-LAI product is designed to capture and decode Northbound and Southbound FBD traffic for a bank of FB DIMMs
- An AMB is used in LAI mode to decode serial data, and then present this as raw Frame data to the Logic Analyzer
- The AMB also echoes the SB serial traffic to the FB DIMM plugged into the straddle-mount connector on the LAI, and the NB traffic to the target's memory controller
- Acquisition of FBD Address / Command, Read and Write data
- Interposer Design so that no valuable memory slots are lost
- NEX-FBD-LAI design does not require a dedicated slot
- NEX-FBD-LAI brings the logic analyzer probe point two feet away via the blue coax cables shown in the picture above, reducing required keep out volume
- Accurate 8GHz timing analysis on every channel
- Time correlation with data from other acquisition modules
- Acquisition of DDR activity up to 667MT/s. This equates to a serial speed of 4Gb/s.

General Description

- The NEX-FBDLAI product is an interposer design. The interposer is a rigid-flex-rigid board arrangement with one rigid board that plugs into the target FB DIMM connector with a short length of flex that attaches to a second small rigid board that has the target FB DIMM connector on it.
- Ten 20-conductor micro coax cables connect to the first rigid board (plugged into the target's FB DIMM connector), and each of these cables terminate in a small PCB where the TLA P6860 probes connect.
- Each NEX-FBDLAI has Event Bus connectors on it so that the Event Bus can be daisy-chained from one FBD LAI interposer to another. The Event Bus would be used in a target system that is using multiple FBD LAI interposers to debug at a system level. The Event Bus allows the AMB device on each LAI to "communicate" with other AMB devices and permit cross-triggering between the AMB devices. The Event Bus would not be used in a single NEX-FBDLAI debug situation.
- The AMB device on the NEX-FBDLAI product has 11 Trigger signals that can be used to inform the TLA when a specific event has been recognized by the AMB device.
- The SMBus interface on the NEX-FBDLAI provides the means to program the internal trigger capability of the AMB chip. This is done via software provided with the FBDLAI that runs on the TLA or on another stand-alone PC. An adapter is provided to convert the TLA's or PC's USB connection to SMBus.
- Pre-Defined Symbols for easy trigger setup based on the DRAM and Channel commands defined in the JEDEC specification.
- No Dedicated Slot Required – The logic analyzer connects above the normal FB DIMM height so that there is no interference with adjacent DIMMs.

Timing Display



NEX-FBD-LAI-x Timing Display

State Display

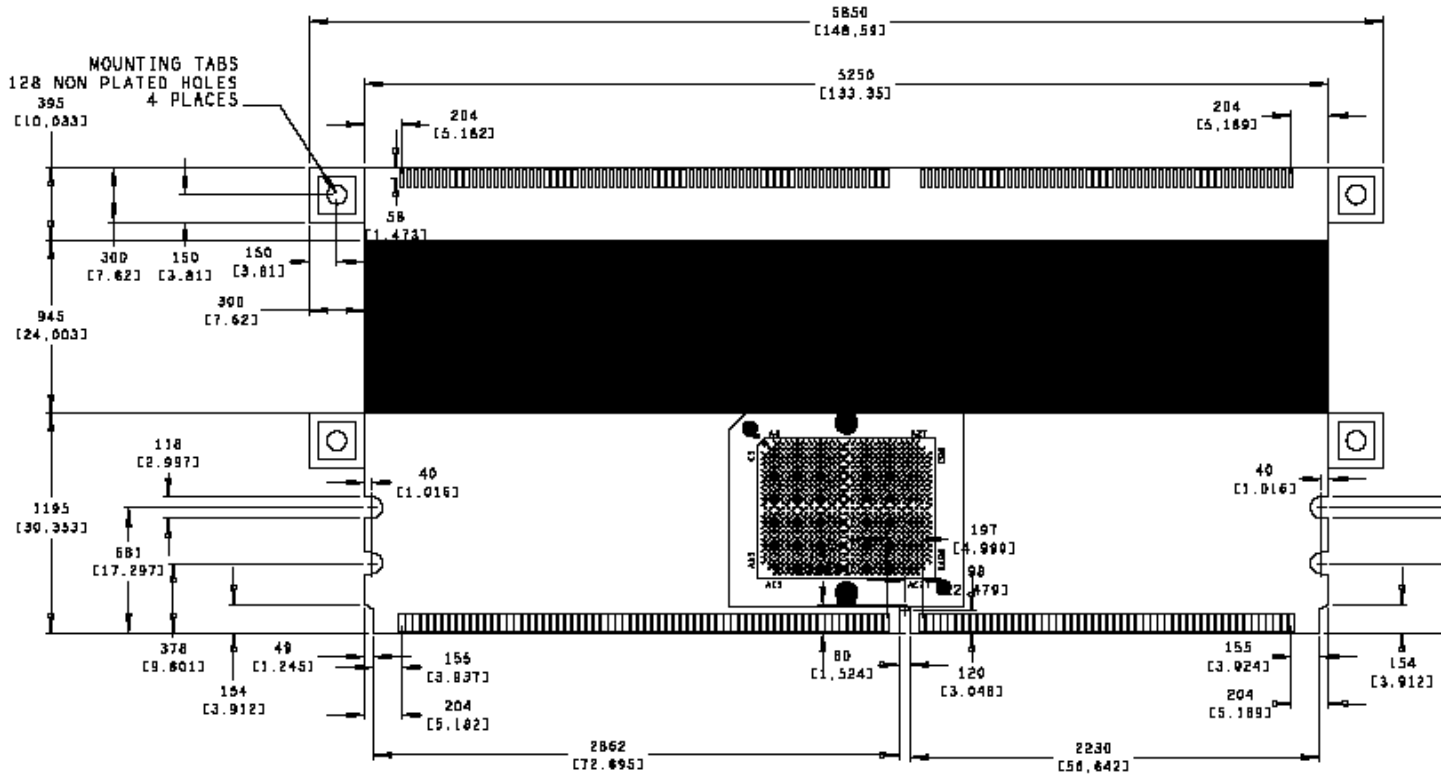
Sample	FBDLAI Mnemonics	zzSBBit0	zzSBBit1	zzNBBit0	zzNBBit1
1348	Transfer SB 0: 0001111111 NB 0: 00000000000000 1: 0001011111 1: 11111111111111 2: 0000011111 2: 00000000000000 3: 0001000001 3: 11111111111111 4: 0000101111 4: 00000000000000 5: 0001001111 5: 11111111111111 6: 0000111111 6: 00000000000000 7: 0011000001 7: 11111111111111 8: 1000101111 8: 00000000000000 9: 0100011111 9: 11111111111111 10: 1000001111 10: 00000000000000 11: 0000100001 11: 11111111111111	FFF	777	AAA	AAA
1349	Transfer SB 0: 0001111111 NB 0: 00000000000000 1: 0001011111 1: 11111111111111 2: 0000011111 2: 00000000000000 3: 0001000001 3: 11111111111111 4: 0000101111 4: 00000000000000 5: 0001001111 5: 11111111111111 6: 0000111111 6: 00000000000000 7: 0011000001 7: 11111111111111 8: 1000101111 8: 00000000000000 9: 0100011111 9: 11111111111111 10: 1000001111 10: 00000000000000 11: 0000100001 11: 11111111111111	FFF	777	AAA	AAA
1350	Transfer SB 0: 0000000000 NB 0: 00000000000000 1: 0000000000 1: 11111111111111 2: 0000000000 2: 00000000000000 3: 0000000000 3: 11111111111111 4: 0000000000 4: 00000000000000 5: 0000000000 5: 11111111111111 6: 0000000000 6: 00000000000000 7: 0000000000 7: 11111111111111 8: 0000000000 8: 00000000000000	000	000	AAA	AAA

NEX-FBD-LAI-x State Display - Hardware Mode (raw Frame data displayed)

Sample	FBDLAI Mnemonics	zzSBBit0	zzSBBit1	zzNBBit0	zzNBBit1
1344	TRAINING	FFF	777	AAA	AAA
1345	TRAINING	FFF	777	3FE	3FE
1346	TRAINING	FFF	777	001	001
1347	TRAINING	FFF	777	FCF	FCF
1348	TRAINING	FFF	777	AAA	AAA
1349	SB A: Activate DIMM:0 Rank:1 Bank:3 Addr: 0x777F Write Data: ECC: 0x20 0x777777FF 0x080A9524 WS:1	FFF	777	AAA	AAA
1350	NB : Idle SB A: Channel NOP B: Channel NOP C: Channel NOP NB : Idle	000	000	AAA	AAA
1351	SB A: Channel NOP B: Channel NOP C: Channel NOP NB : Idle	000	000	3FE	3FE
1352	SB A: Sync SD:0 IER:0 ERC:0 ELOs:0 Reg:0 Latency:13 NB : Idle	AA0	550	001	001
1353	SB A: Channel NOP B: Channel NOP C: Channel NOP NB : Idle	000	000	FCF	FCF
1354	SB A: Channel NOP B: Channel NOP C: Channel NOP NB : Idle	000	000	AAA	AAA
1355	SB A: Channel NOP B: Channel NOP C: Channel NOP NB : Idle	000	000	AAA	AAA
1356	SB A: Activate DIMM:0 Rank:0 Bank:0 Addr: 0x0000 NB : Idle SB A: Channel NOP B: Channel NOP C: Channel NOP	000	000	AAA	AAA
1357	SB A: Channel NOP Write Data: ECC: 0x11 0x11111111 0x11111111 WS:0 NB : Idle SB A: Channel NOP	110	110	000	000
1358		220	220	000	000

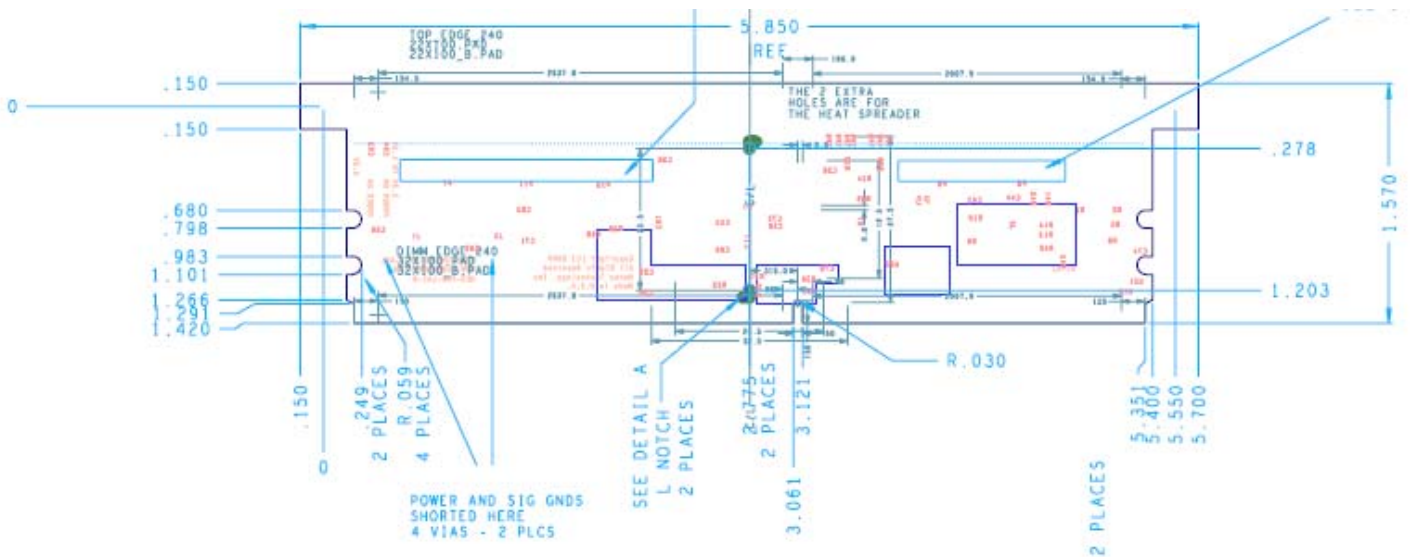
NEX-FBD-LAI-x State Display - Software Mode (Frame data decoded)

Mechanical Outline NEX-FBD-LAI Front VIEW



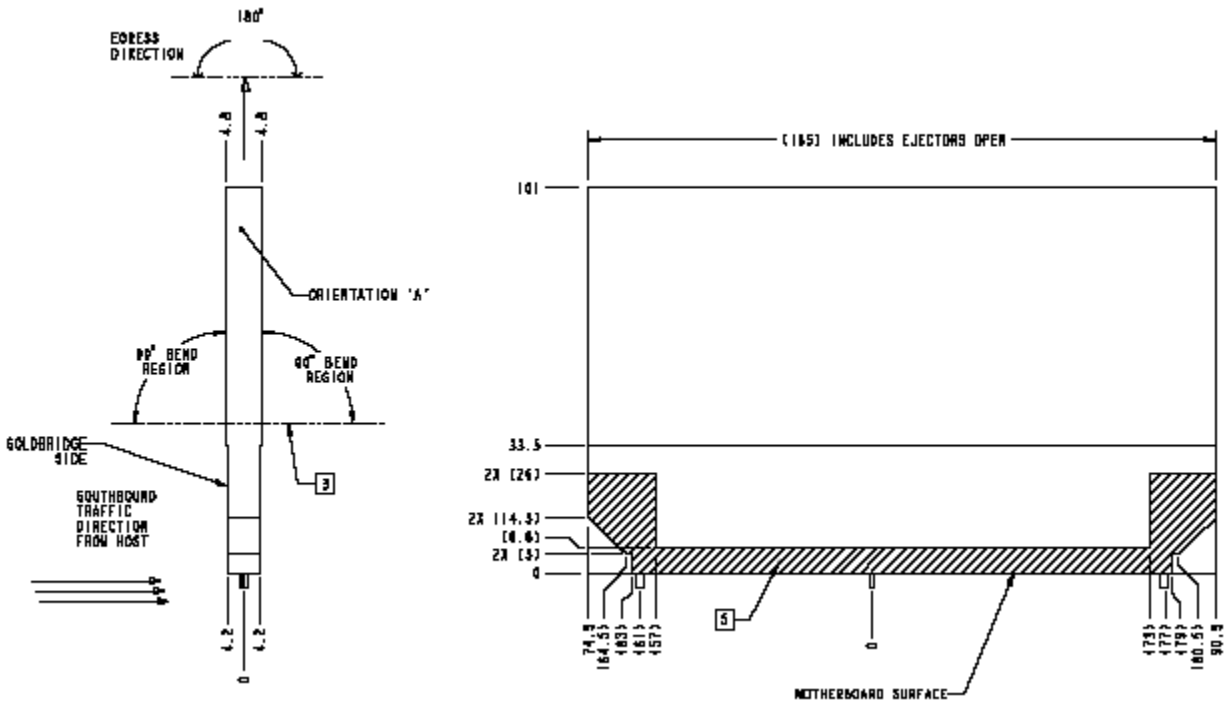
Note: This mechanical drawing of the NEX-FBD-LAI does not show the coax cables and the small boards that interface to the Tektronix Logic Analyzer

Mechanical Outline NEX-FBDLAI-RG Front VIEW (Rigid Version)

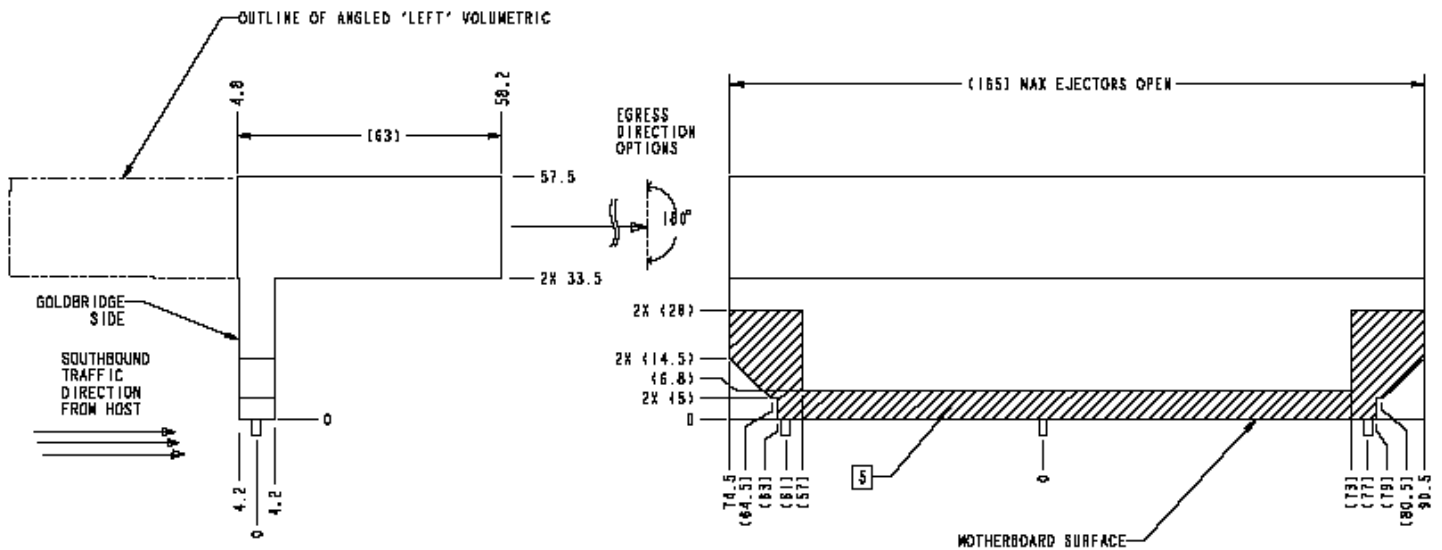


Keep out Volumes (Flex version)

The probe is designed to fit within a minimum DIMM pitch of 0.375" for non-stacked DIMMs and 0.4" for stacked SIMMs. The KOV is based on the current FDB size SIMMs which is 1.2" tall and does not account for other "Custom" DIMMs.



Vertical Orientation (Courtesy Intel)



Horizontal Orientation (Courtesy Intel)

The keep out volume shown in the left half of the above diagram represents two FBD-LAI products plugged into adjacent DIMM slots and both using right angle support brackets (included). Both LAIs are angled to the right with the left one bent over the other, with the LA cables exiting to the right.

Tektronix Logic Analyzer Support and Configuration

A TLA700 equipped with three merged 136-channel 450MHz state speed acquisition modules (TLA7AA4 or TLA7AB4 cards) is required. In addition, ten P6860 Tektronix probes are required.

Ordering / Contact Information

Please see the website or contact us for complete solutions.

Part Number NEX-FBDLAI or NEX-FBDLAI-RG

Includes: NEX-FBDLAIx adapter
Software
Manual

Postal: Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

Telephone: 877-595-8116

Fax: 877-595-8118

Email: support@nexustechnology.com
quotes@nexustechnology.com
techsupport@nexustechnology.com

Website: www.nexustechnology.com

Placing an Order

Credit Card orders can be placed directly at 877-595-8116.

Purchase orders can be faxed to 877-595-8118.

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