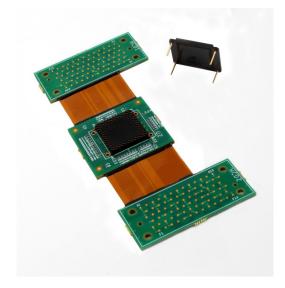
LPDDR2 PoP Logic Analyzer Component Interposer

168 ball Package on Package memory device support

- Optimal Digital Validation
- Easy to Install
- Use with Existing Embedded / Mobile designs
- Designed for speeds of LPDDR2-1067+
- Socket Design also available without a socket
- Support for LPDDR2 Memory Devices
 - Package on Package (PoP)
 - o **12mmX12mm**
 - o x32 data width
 - o 0.5 mm pitch
- Probed at the BGA Pads
- TLA setup software(iCiS) included
- Optional Compliance Analysis software available
- Compatible with Nexus Memory Compliance Analyzer(MCA) Instrument



Nexus Technology recommends LPDDR2 component interposers for applications requiring optimal digital validation of LPDDR2 targets. These interposers allow for logic analyzer acquisition of command, address, and data of 168-ball LPDDR2 components. These interposers are also compatible with the Nexus MCA Instrument.

The PoP Challenge

Low Power DDR2 (LPDDR2) memory components are expanding rapidly in the market providing low power, high bandwidth, high density memory solutions. The Package on Package version results in target space saving but introduces significant roadblocks for test/debug and analysis of the memory interface.



Figure 1 - Side view (photo) of PoP memory soldered on to a processor

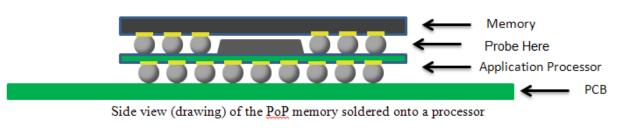
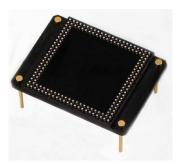


Figure 2 - Side view (drawing) of the PoP memory soldered onto a processer

Premier Component Interposer Design

Optimal LPDDR2 validation requires analysis of the LPDDR2 signals, as seen by the memory components. This allows for the highest confidence that the captured signals are representative of the signals on the target. Nexus Technology component interposers allow for logic analyzer probing of the LPDDR2 signals at the memory components BGA balls.



Memory Component Interposer Installation

The process of attaching the interposer to your target has been greatly simplified using Nexus Technology's patented, high-bandwidth, component interposer sockets. These patented sockets remove the need to contract specialized rework houses to perform the installation. Instead, you can use standard BGA assembly practices to install the component interposer socket. Nexus Technology can perform the attachment service for a nominal fee.

Once the interposer socket is installed on the target, logic analyzer or oscilloscope interposers can be easily inserted or removed from the socket. Note that the interposer socket elevates the interposer above the adjacent components to provide the mechanical clearance necessary for easy probe attachment.

LPDDR2 BGA Component installation

The interposer can be ordered with a socket on the interposer for easy BGA memory component installation and removal. These sockets allow for the quick swapping and testing of different memory components on the interposer. The Sockets quick Start Guide provides more information.

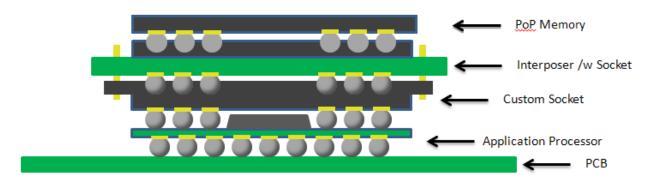


Figure 3 - Side view of the complete interposer installation

LPDDR2 PoP Logic Analyzer Component Interposer

Logic Analyzer Component Interposer Hardware

Connection to a logic analyzer is enabled by using LPDDR2 Memory Component Interposers. These controlled impedance; matched trace length interposers provide visibility for digital validation using a logic analyzer. The rigid / flex / rigid design allows for the interposer to be used in targets with minimal mechanical clearance around the target component. These interposers are also compatible with the Nexus MCA Instrument.

Logic Analyzer Component Interposer Software

Nexus Technology component interposers come with the required logic analyzer setup software and iCiS setup tool. Optional full compliance analysis software is available separately.

Logic Analyzer Setup Software

The Logic analyzer setup software provides a quick setup of the clocking / acquisition parameters. This software also includes protocol decoding of the LPDDR2 transactions for easy display

and analysis. Setup is fast and easy using the graphical iCiS Tool.

- Load the TLA Software
- Load the Support Package
- Run the calibration tools
- Ready to Acquire!

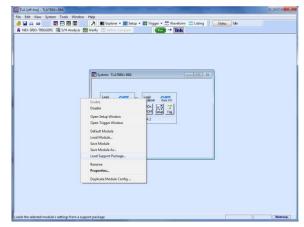


Figure 4 - TLA Setup Software

TLA Data Analysis

Synchronous state data correlated with 50GHz MagniVu timing data, iCapture Analog Mux, and Compliance Analysis tools provide analysis capability that is best in industry.

Bus Decode and Timing

The logic analyzer provides listing and timing displays of the synchronous state and asynchronous MagniVu timing data. The MagniVu timing data is acquired simultaneously with and correlated to the state acquisition data with no skew. In fact, the state acquisition data is derived from the MagniVu timing data. This provides much more information on the acquired data and, most importantly, it provides an extra level of confidence that the data acquired was correct.

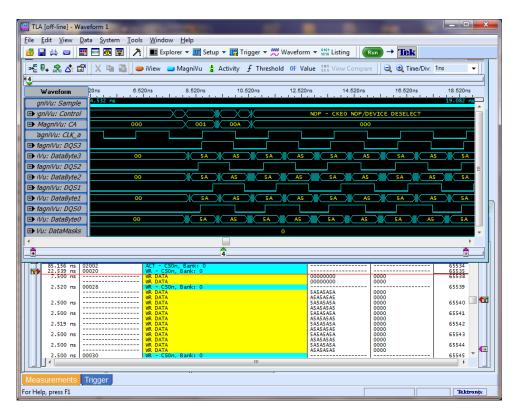


Figure 5 - State & 50GHz MagniVu Timing

The asynchronous, 50GHz (20ps) MagniVu timing data provides extremely accurate timing analysis of the LPDDR2 bus and is simultaneously acquired and correlated with the state acquisition data.

_	TLA [off-line]		Real Concerns				10 10
			Tools Window Help				- 8 >
			Explorer - Market Setup - R Trigger - Wavef		Run → Tek		
n [¥] n			🖌 🕈 Threshold 🔡 View Compare 🛛 A A 🗙 🗈	🚨 🕈 🕅 🕹 Se	arch 🔻 💆	<u> </u>	
	t 👻 Cursor 1	✓ to Cursor 2	078ns				
	Timestamp	B_32LPDDR2E13 Address	B_32LPDDR2E13 Mnemonics	B_32LPDDR2E13 Data	B_32LPDDR2E13 DataMasks	Sample	^ 🖸
J.	85.156 ns 22.539 ns	02002 00020	ACT - CSOn, Bank: 0 WR - CSOn, Bank: 0			65534 65535	
Ĩ	7.500 ns		WR DATA	00000000	0000	65538	
	2.520 ns	00028	WR - CSOn, Bank: 0 WR DATA	5A5A5A5A	0000	65539	
	2.500 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65540	
	2.500 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65541	
	2.519 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65542	
	2.500 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65543	
	2.500 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65544	
	2.500 ns	00030	WR DATA WR - CSOn, Bank: 0	A5A5A5A5	0000	65545	
			WR DATA WR DATA	5A5A5A5A A5A5A5A5	0000		
	7.520 ns		WR DATA WR DATA	A5A5A5A5 A5A5A5A5	0000	65548	1
	2.480 ns		WR DATA WR DATA	5A5A5A5A A5A5A5A5	0000	65549	
	2.500 ns		WR DATA WR DATA	5A5A5A5A A5A5A5A5	0000	65550	
	2.520 ns		WR DATA WR DATA	5A5A5A5A A5A5A5A5	0000	65551	
	15.020 ns 7.519 ns	00038	WR - CSOn, Bank: 0 WR DATA	A5A5A5A5	0000	65557 65560	
	2.500 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65561	
	2.500 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65562	
	2.520 ns		WR DATA WR DATA	A5A5A5A5 5A5A5A5A	0000	65563	
	15.039 ns	00040	WR DATA WR - CSOn, Bank: 0	A5A5A5A5	0000	65569	
	7.500 ns		WR DATA WR DATA	A5A5A5A5 A5A5A5A5	0000	65572	
	2.500 ns		WR DATA WR DATA	5A5A5A5A A5A5A5A5	0000	65573	
	2.519 ns		WR DATA WR DATA	5A5A5A5A A5A5A5A5	0000	65574	
	2.500 ns		WR DATA WR DATA	5A5A5A5A A5A5A5A5	0000	65575	
	15.020 ns 7.500 ns	00060	WR - CSOn, Bank: 0 WR DATA	ASASASAS	0000	65581 65584	
	2 500		WR DATA	A5A5A5A5 E A E A E A E A	0000	CCC 00	T
			m			•	
<u> </u>	easuremen	ts Trigger					
For	Help, press F1					Tektr	onix

Figure 6 - State Data

TLA [off-line] - [Wavefo	
🞬 File Edit View D	Data System Tools Window Help
🚳 📑 📇 📼 📰 🖻	🔤 🐼 😰 📝 者 📧 Explorer 🕶 🜆 Setup 👻 🌆 Trigger 🗸 🗮 Waveform 👻 🔛 Listing 🛛 🕼 🔤 🛨 Teck
>E ₽₊ 🔝 🖄 🖆 🗴	🗶 🗈 🚰 🛑 iView 🔲 MagniYu 🛔 Activity 🖌 Threshold OF Value 👯 View Compare 🛛 🗨 🍳 Time/Div. 500ps 🔹 🗸 🔶 🦍 🗢 Search 👥 🖤
	-1.500 ns -1.ns -500 ps 0 ps 500 ps 1 ns 1.500 ns 2 ns 2.500 ns 3 ns 3.500 ns 4 ns 4.500 ns 5 ns 5.500 ns 6 ns 6.500 ns 7 ns 7.500 ns 8 ns 8.500 ns 9 ns 9.500 ns 1 ns
	.836 ns
🕀 gniVu: Control	R - CSOT WRITE) X X NOP - CKEO NOP/DEVICE DESELECT X X 🛒
MagniVu: CA ■ MagniVu: CA ■	001 X 008 X 001 X 001
'agniVu: CLK_a	
<i>iVu: DataByte3</i>	00 5A
■ 1agniVu: DQS2	
	00 5A
	00 💥 5A 💥
■ 1agniVu: DQS0 ■	
	00 SA X
<i>Vu: DataMasks</i>	0
_ <u>_</u>	
Measurements Trig	gger
For Help, press F1	Taktronic .

Figure 7 - MagniVu Timing Data

iCapture Analog Mux

A powerful analog validation feature is the Tektronix Logic Analyzer's unique Analog Mux capability. This provides the ability to see *any* channel of the LPDDR2 bus in seconds on an oscilloscope. This is invaluable information which allows analysis within minutes as to the status and behavior of the LPDDR2 bus. No extra probing is required! This information can be pushed back into the logic analyzer, correlated and viewed in a wave form window along with the state or timing data using the iView Feature.

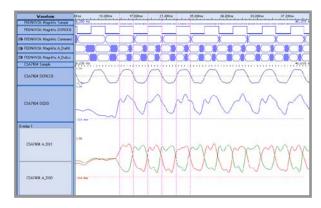


Figure 8 - Example Representation of iView

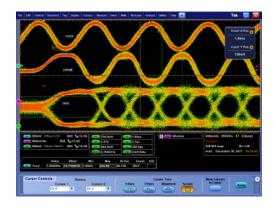


Figure 9 - Example iCapture Analog Mux

Taking advantage of the ultra-high fidelity "Scope Probe per Signal" capability of the LPDDR2 Interposer, iCapture enables focused analog level analysis and validation.

Sample Point Setup

In order for the logic analyzer to capture signals accurately, the sample points must be properly set. iCiS provides a graphical display of the signal eyes on a per group or per signal basis(See Figure 6). You easily select the optimum sample point.

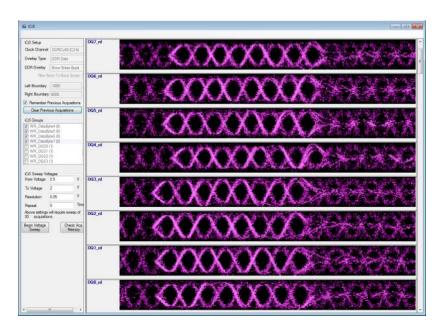


Figure 10 - Example iCiS DQ Data Setup

Setting up the logic analyzer is easy! Load the TLA software, load the support package, and click Run. It's as simple as that for compliance analysis (CMD/ADDR/CTRL acquisition). Acquiring the DQ read and write data is easily done with the graphical iCiS tool.

Compliance Analysis Software

These products optionally include the LPDDR2 Memory Compliance Analysis software package. This software performs advanced command sequence & timing compliance analysis. It also provides statistical information and global bus activity to quickly give the user an overview of the LPDDR2 bus activity without having to revert to a listing or waveform window.

- Extensive JEDEC LPDDR2 Compliance Analysis
- Quick and Easy Setup w/No Calibration Required
- Automated Acquisition and Measurement
- Powerful in-application graphical and tabular analysis results
- Memory controller & JEDEC parameters predefined
- Quickly navigate through multiple acquisitions



	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec.
R2 R1 R0	NA	NA	NA	NA	959,880
5 R2 R1 R0	28,007	10,273,985	2,106,353		26,250
B R2 R1 <mark>R0</mark>	7,441	878,808	123,227	3.3	7,200
5 R2 R1 R0					5,625
B R2 R1 R0	NA	NA	NA	NA	70,200,000
3 R2 R1 R0	1,855	8,189,726	945,496	-85.9	13,125
B R2 R1 <mark>R0</mark>	114,121	8,169,101	6,001,631	3.7	110,000
8 R2 R1 <mark>R0</mark>	42,969	2,839,180	267,945	14.6	37,500
e re ri <mark>ro</mark>	42,969	2,839,180	267,945	-99.9	70,200,000
3 R2 R1 <mark>R0</mark>	18,652	116,172	20,254	42.1	13,125
R2 R1 R0	13,066	316,308	170,537	16.1	11,250
2 RI RO					20,625
NI RO	37,383	326,054	162,946	10.8	33,750



ile <u>V</u> iev		ndow <u>H</u> e	lp							
	ince Setup 🏼 🧭 S		Check A	cq. Mem	ory					
-	ting, Acquisition					Constraint Con	- 23			
	Timestamp (nS)	Address	Rank #	Bank #		Violation	_			
	929774.100	-	•	7	NOP					
912470	929775.500	3045			NOP					
912472	929777.600	3045			NOP		- 1			
	929778.200	3015	0	3	WR					
	929779.600	0060		3	NOP					
	929780 300	111		7	NOP					
	929781.600	-		7	NOP					
	929782 200	-		7	NOP					
912478	929783.600	-		7	NOP					
	929784.300	1001		7	NOP					
	929785.700	m			NOP					
	929786.300	1995			NOP					
	929787.700	-			NOP					
	929788.400			7	NOP					
	929789.800	-	-	7	NOP					
	929790.400		•	7	NOP		- 1			
912486	929791.800	-		7	NOP					
Data W	weform, Acquisit	tion 3								
Timestan	np (nS)	2977 <mark>5.500</mark>			9297	80.300		929785.700		
Clock							பாப		лп	
Address	111	3045	306	X or	ю Х					
Rank #		X	эχ.	X O	X					
Bank #	7	(1	X	3	X		7			
Comman	d NO	P X A	T NOF	X WR	X		NOP			
Volation		X	X							
			_							
			_							

Figure 12 - Waveform & Timing Displays of Compliance Analysis

Comp	liance Parameters					_					
tat N	um. Name	Occurences	Violations	Status	-	Min.(ps) Max.(ps)	Average(ps)) Margin(%)	Spec. Value(ps)	Description
1	CMD wisSREF Rank	00	00		23 O3 (77	REIG NA	NA	NA	NA	00	Sequential check. A non-NOP/DES command can not occur on a self-refreshing rank.
2	SRE wisACT Rank					RE O NA					Sequential check. A Self-Refresh Entry (SRE) command can not occur on an active rank.
3	MRS wisACT Rank	00	00			SE O NA	NA	NA	NA	00	Sequential check. An Mode Register Set (MRS) command can not occur on an active rank.
4	RD(A)/WR(A) during MRS					RE O NA					Sequential check. A read (RD or RDA) or write (WR or WRA) command can not occur during rank MRS cycle.
5	CMD w/sPD Rank	00	00			RE O NA			NA		Seguential check. A non-NOP/DES command can not occur on a powered-down rank.
6	RD(A)/MR(A) wisREF Bank					RE O NA					Sequential check. A read (RD(A)) or write (WR(A)) command can not occur during bank refresh.
						#E 0 00					Sequential check: A activate (ACT) or refresh (REF) command can not occur on an active bank.
8	REF wisACT Bank					#E 0 00					Sequential check. A refresh (REF) command can not occur on an active bank that is reading or writing.
9	RD(A)/MR(A) to sPRE Bank										Sequential check: A read (RD(A)) or write (WR(A)) command can not occur during on an inactive (precharged) bank.
1	d4ACT					RE 0 20,977					The minimum time between any four activate (ACT) commands to the same rank must meet IFAW.
						SEC NA					Power-Down Exit (PDX/PPX) to any valid command (PRE(A)/REF/ACT/MRS) must meet tXP.
	2 SRX Exit					RE O NA					Self-Refresh Exit (SRXIPRX) to any command not requiring a locked DLL (PRE(A)/REF/ACT/MRS/SRE) must meet XS.
	3 d4CT					RE CO 6.679					The minimum time between two activate (ACT) commands must meet tRRD.
	4 PRE(A) Rank Settle					RE O NA					Minimum time from a PRE(A) command to any valid command on the same rank (MRS/SRE) must meet tRP.
	5 REF Before SRE					RECO NA					Sequential check. At least one refresh (REF) command is required between self refreshed (SRX to SRE).
	SRE Separation from PRE(A)					RE O NA					If the last valid command received before a self-refresh entry (SRE) was any precharge PRE(A), then the separation between these two
	7 SRE Separation from REF					SEC NA					If the last valid command received before a self-refresh entry (SRE) was a refresh (REF), then the separation between these two comma
	8 SRE Separation from ACT					RE O NA					If the last valid command received before a self-refresh entry (SRE) was a activate (ACT), then the separation between these two comm
						SEC NA					If the last valid command received before a self-refresh entry (SRE) was a mode register set(MRS), then the separation between these t
	0 SRE Separation from WR					RE O NA					If the last valid command received before a self-refresh entry (SRE) was a write (WR), then the separation between these two command
						SEC NA					If the last valid command received before a self-refresh entry (SRE) was a write wlauto-precharge (WRA), then the separation between
						RE O NA					If the last valid command received before a self-refresh entry (SRE) was a read (RD(A)), then the separation between these two comman
						SEC NA					Minimum time from an mode register set (MRS) command to any other valid command that is not an MRS must meet tMOD.
						RE O NA					Minimum from the first to the next and subsequent mode register set (MRS) commands must meet tMRD.
						SEC NA					The minimum amount of time in self-refresh must meet ICKESR.
						RE 0 4.024					The minimum amount of time between write (WR(A)) commands must meet tCCD.
						## C 10,156					The minimum amount of time between read (RD) and write (WR(A)) commands must meet tNRTW.
2						RE O NA					Power-Down Exit (PDX/PRX) Slow Exit (MRS_A12 bit low) to read (RD(A) command must meet XPDLL.
						SEC NA					Read (RD(A)) must wait tDLLK after reset.
3						# 3 0 18.835					The minimum amount of time between write (WR) and read (RD(A)) commands must meet tWWTR.
						ME: 0 4,023					The minimum amount of time between read (RD(A)) commands must meet tCCD.
3						RE O NA					The minimum amount of time a rank must stay in power-down (PDE to PDX) must meet tPDmin.
						SEC NA					The maximum amount of time a rank can stay in power-down (PDE to PDX) must meet tPDmax.
3		71,546				ss o 8,710			-26.0		Minimum time from a PRE(A) command to any valid command on the same bank must meet IRP.
3		1,792		ធាយផា		## Co 108,41		3,102,259	20.5	90,000	The minimum amount of time in refresh must meet tRFC.
3						#E 0 24,375					The minimum amount of time a bank must stay active (ACT to PRE(A)) must meet tRASmin.
3		21,624	00	යා යා යා ය		BE 0 24.375			-100.0	70,200,000	The maximum amount of time a bank can stay active (ACT to PRE(A)) must meet tRASmax.
3		44,402	24,699			#E 0 8,711	300,371	20,155	-26.0	11,770	The minimum amount of time from a activate (ACT) command to a read (RD(A)) or write (WR(A)) command must meet tNARW.
3		858	747			RE 0 6.679	128,672	10.282	-27.1	9.162	The minimum amount of time from a read (RD) command to a precharge (PRE(A)) command must meet tNRP.
4		64	00			# 3 0 16 ,288		78,554	23.1	13,234	The minimum amount of time from a read (RD) command to a activate (ACT) command must meet tNRA.
4						## <mark>0</mark> 25,385				27,486	The minimum amount of time from a write (WR) command to a precharge (PRE(A)) command must meet tNWP.
4		237	00			#ELG 35,175			165.8	13,234	The minimum amount of time from a write (WR) command to a activate (ACT) command must meet tWWA.
4	3 CKEx Signal After DLL Reset	00	00	යා යා යා ය	20 GB (A	SEC NA	NA	NA	NA	521,072	Rank CKEx must remain high tDLLK time after a DLL Reset.
		_	_	_	_						
divid	fual Acquisition Details					-				Per Acquis	sition Violation Details
		Occurences N	Taladana fa	in data		Martin	Mandala		dargin(%) D:		Timestamp Rank Bank Offending Cmd Value(ps) Margin(%)

Figure 13 - Detailed Compliance Analysis Results

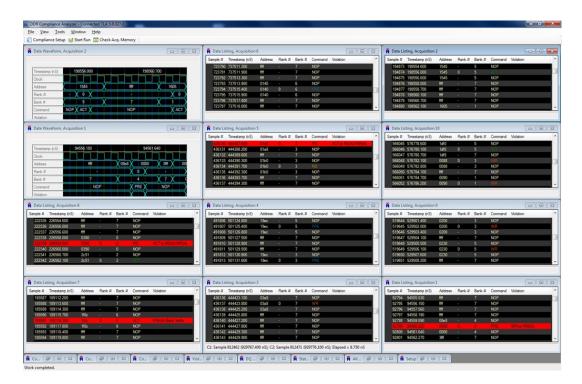


Figure 14 - View Violations in Data Across Many Acquisitions

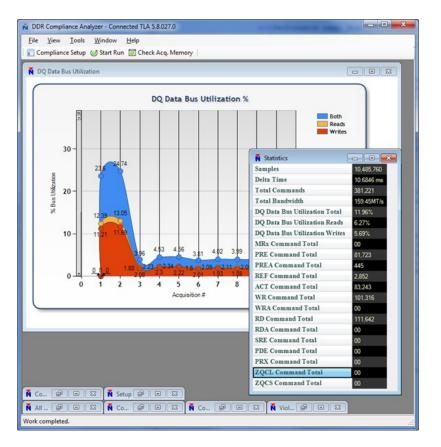


Figure 15 - Bus Utilization Measurements



Figure 16 - Graphical and Tabular Compliance Analysis Examples

Nexus Technology LPDDR2 Component Interposer Advantages

Probed at the BGA Pads

The best place to probe a memory bus is at the BGA balls to eliminate reflections associated with break-out board probing, embedded mid-bus probing or other methods. Nexus Technology's component interposers provide easy access to memory component BGA pads for accurate memory bus analysis.

Use with Existing Package-on-Package or Embedded designs

No need to change existing designs. Simply add the interposer to your embedded target or DIMM with no re-design or added probe points. No Need to add probe points to existing designs. Simply add the interposer to your DIMM or embedded target for easy connectivity to the Logic Analyzer.

Interchangeable Socketed Interposers

The interposers are reusable. Once an interposer socket is installed on a target, the interposer can be attached and removed by hand. This allows an interposer to be used on multiple targets, or enables quick swapping of logic analyzer and oscilloscope interposers on the same target. The interposer socket has four posts that are soldered to four mounting holes on the interposer to retain the interposer to the socket.

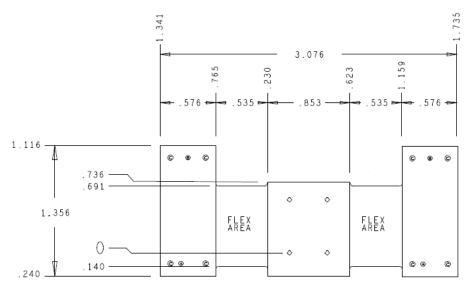
Easy to Install

Install the interposer socket using industry standard BGA attachment methods or by using Nexus Technology's Attachment Service. Contact Nexus Technology for further information on our Attachment Service.

Simple Digital and Analog Validation via Standard Interposer Socket

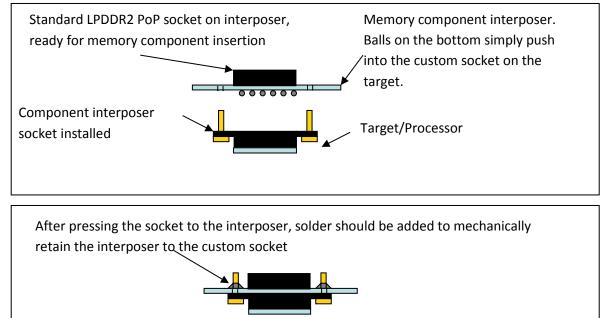
Nexus Technology's Component interposers are designed for optimal signal integrity. Once our custom socket is installed on your target, our interposers can be easily swapped out. We offer Oscilloscope component interposers for analog validation, and Logic Analyzer component interposers for digital validation.

Product Dimensions





Attaching and Reusing Interposers



LPDDR2 PoP 168 Ball Logic Analyzer Component Interposer

Configuration Tables

LPDDR2 PoP 168 Ball Logic Analyzer Interposers

Nomenclature	Interposer Type	Data Width	Component Socket Included	Nexus Probes Included	Installation Service Included	Hardware Requirements
NEX-LPDDR2PoP168BLASK	Logic Analyzer	x32	Yes	No ¹	No	1- TLA7000 Series Mainframe -1- TLA7Bx4 1.4 GHz
NEX-LPDDR2PoP168BLASK-AT	Logic Analyzer	x32	Yes	No ¹	Yes	Acquisition Card 1- NEX-PRB1XL Probe
NEX-LPDDR2PoP168BLASKPR	Logic Analyzer	x32	Yes	Yes ¹	No	& 1- NEX-PRB2XL Probe
NEX-LPDDR2PoP168BLASKPR-AT	Logic Analyzer	x32	Yes	Yes ¹	Yes	-OR 2- NEX-PRB1XL Probes

Optional Additional LPDDR2 PoP 168 Ball Interposer Sockets

Nomenclature	Data Width	Solder Balls Added	Quantity of Sockets
NEX-LP2-168BGASKBA	x32	Yes	1
NEX-LP2-168BGASKBA-3	x32	Yes	3

Product Support

Product Support is critical to your success. Our engineering staff can provide expert training and support tailored to your specific needs. Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

Web	www.nexustechnology.com
Telephone	877.595.8116
International	603.329.3083
Fax	877.595.8118
Address	78 Northeastern Blvd. Unit 2 Nashua, NH 03062
Email	support@nexustechnology.com

