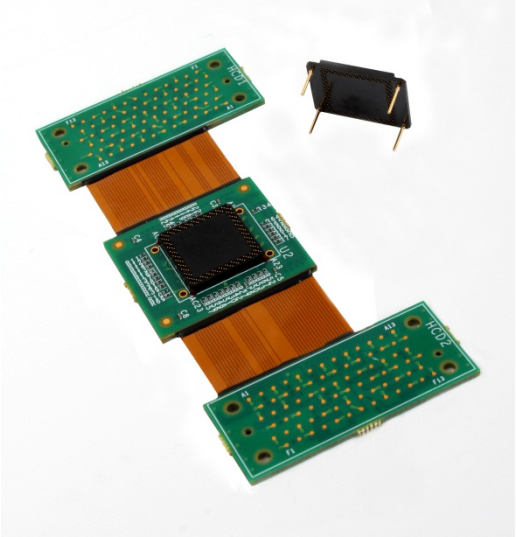
LPDDR2 PoP Logic Analyzer Component Interposer

168 ball Package on Package memory device support

- Optimal Digital Validation
- Easy to Install
- Use with Existing Embedded / Mobile designs
- Designed for speeds of LPDDR2-1067+
- Socket Design – also available without a socket
- Support for LPDDR2 Memory Devices
    - Package on Package (PoP)
    - 12mmX12mm
    - x32 data width
    - 0.5 mm pitch
- Probed at the BGA Pads
- TLA setup software(iCiS) included
- Optional Compliance Analysis software available
- Compatible with Nexus Memory Compliance Analyzer(MCA) Instrument



Nexus Technology recommends LPDDR2 component interposers for applications requiring optimal digital validation of LPDDR2 targets. These interposers allow for logic analyzer acquisition of command, address, and data of 168-ball LPDDR2 components. These interposers are also compatible with the Nexus MCA Instrument.

The PoP Challenge

Low Power DDR2 (LPDDR2) memory components are expanding rapidly in the market providing low power, high bandwidth, high density memory solutions. The Package on Package version results in target space saving but introduces significant roadblocks for test/debug and analysis of the memory interface.

Figure 1 - Side view (photo) of PoP memory soldered on to a processor

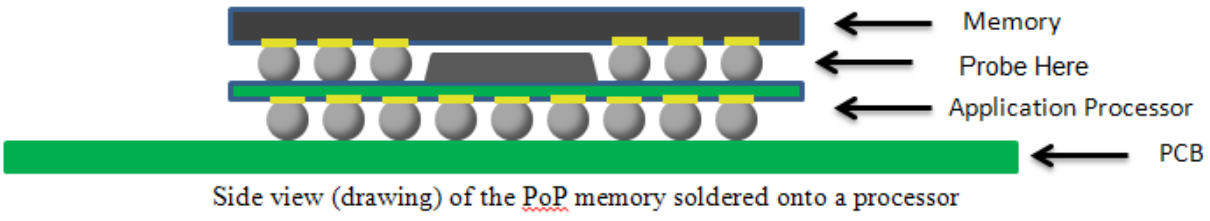
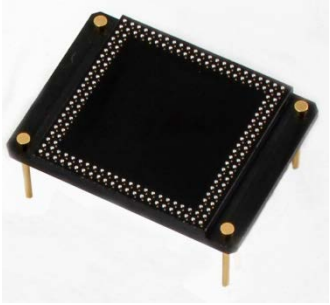


Figure 2 - Side view (drawing) of the PoP memory soldered onto a processer

Premier Component Interposer Design

Optimal LPDDR2 validation requires analysis of the LPDDR2 signals, as seen by the memory components. This allows for the highest confidence that the captured signals are representative of the signals on the target. Nexus Technology component interposers allow for logic analyzer probing of the LPDDR2 signals at the memory components BGA balls.



Memory Component Interposer Installation

The process of attaching the interposer to your target has been greatly simplified using Nexus Technology's patented, high-bandwidth, component interposer sockets. These patented sockets remove the need to contract specialized rework houses to perform the installation. Instead, you can use standard BGA assembly practices to install the component interposer socket. Nexus Technology can perform the attachment service for a nominal fee.

Once the interposer socket is installed on the target, logic analyzer or oscilloscope interposers can be easily inserted or removed from the socket. Note that the interposer socket elevates the interposer above the adjacent components to provide the mechanical clearance necessary for easy probe attachment.

LPDDR2 BGA Component installation

The interposer can be ordered with a socket on the interposer for easy BGA memory component installation and removal. These sockets allow for the quick swapping and testing of different memory components on the interposer. The Sockets quick Start Guide provides more information.

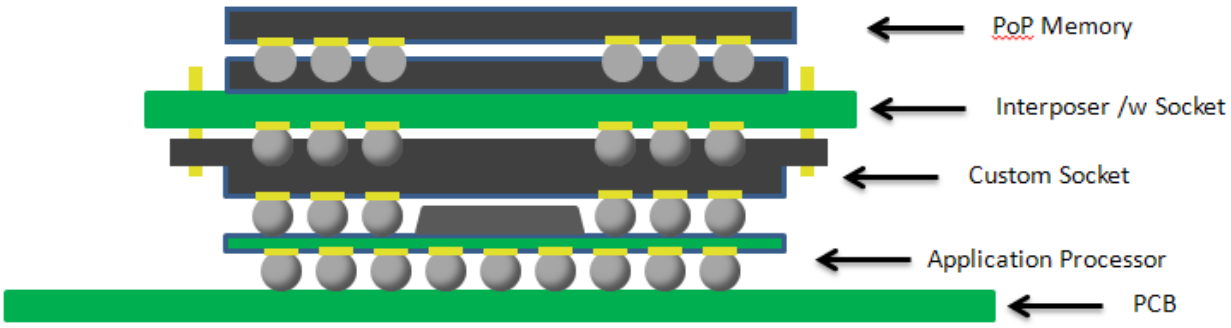


Figure 3 - Side view of the complete interposer installation

LPDDR2 PoP Logic Analyzer Component Interposer

Logic Analyzer Component Interposer Hardware

Connection to a logic analyzer is enabled by using LPDDR2 Memory Component Interposers. These controlled impedance; matched trace length interposers provide visibility for digital validation using a logic analyzer. The rigid / flex / rigid design allows for the interposer to be used in targets with minimal mechanical clearance around the target component. These interposers are also compatible with the Nexus MCA Instrument.

Logic Analyzer Component Interposer Software

Nexus Technology component interposers come with the required logic analyzer setup software and iCiS setup tool. Optional full compliance analysis software is available separately.

Logic Analyzer Setup Software

The Logic analyzer setup software provides a quick setup of the clocking / acquisition parameters. This software also includes protocol decoding of the LPDDR2 transactions for easy display and analysis. Setup is fast and easy using the graphical iCiS Tool.

- Load the TLA Software
- Load the Support Package
- Run the calibration tools
- Ready to Acquire!

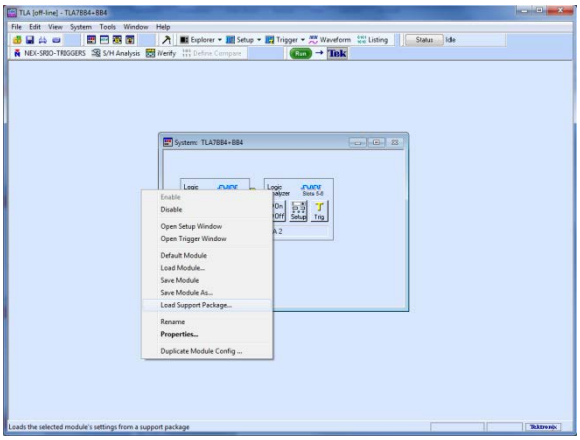


Figure 4 - TLA Setup Software

TLA Data Analysis

Synchronous state data correlated with 50GHz MagniVu timing data, iCapture Analog Mux, and Compliance Analysis tools provide analysis capability that is best in industry.

Bus Decode and Timing

The logic analyzer provides listing and timing displays of the synchronous state and asynchronous MagniVu timing data. The MagniVu timing data is acquired simultaneously with and correlated to the state acquisition data with no skew. In fact, the state acquisition data is derived from the MagniVu timing data. This provides much more information on the acquired data and, most importantly, it provides an extra level of confidence that the data acquired was correct.

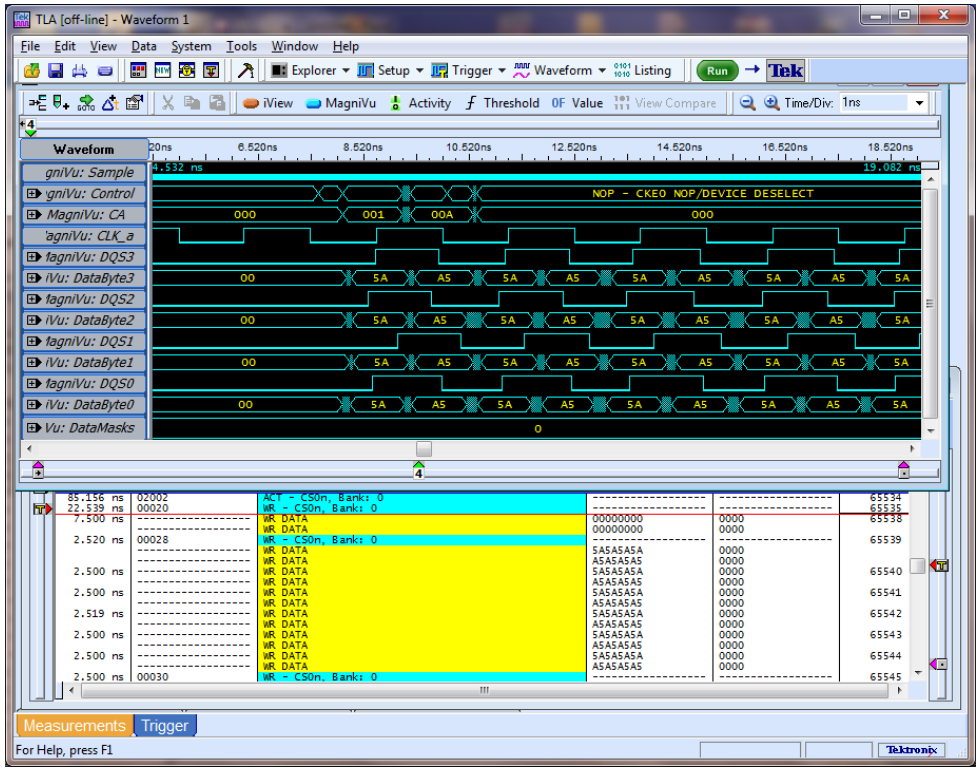


Figure 5 - State & 50GHz MagniVu Timing

The asynchronous, 50GHz (20ps) MagniVu timing data provides extremely accurate timing analysis of the LPDDR2 bus and is simultaneously acquired and correlated with the state acquisition data.

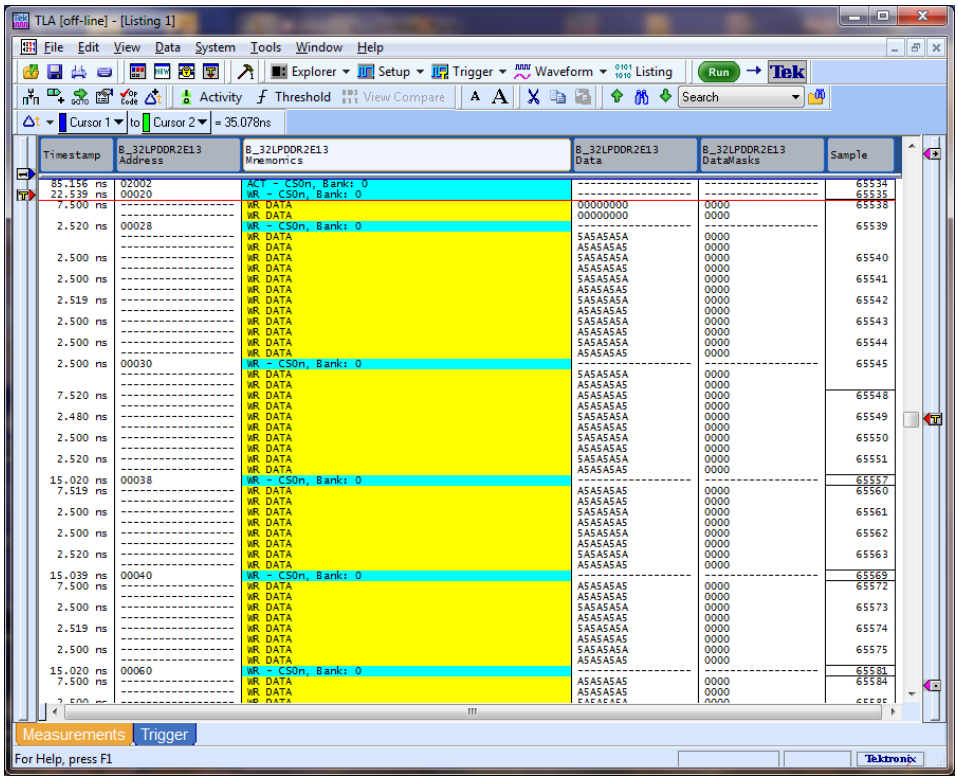


Figure 6 - State Data

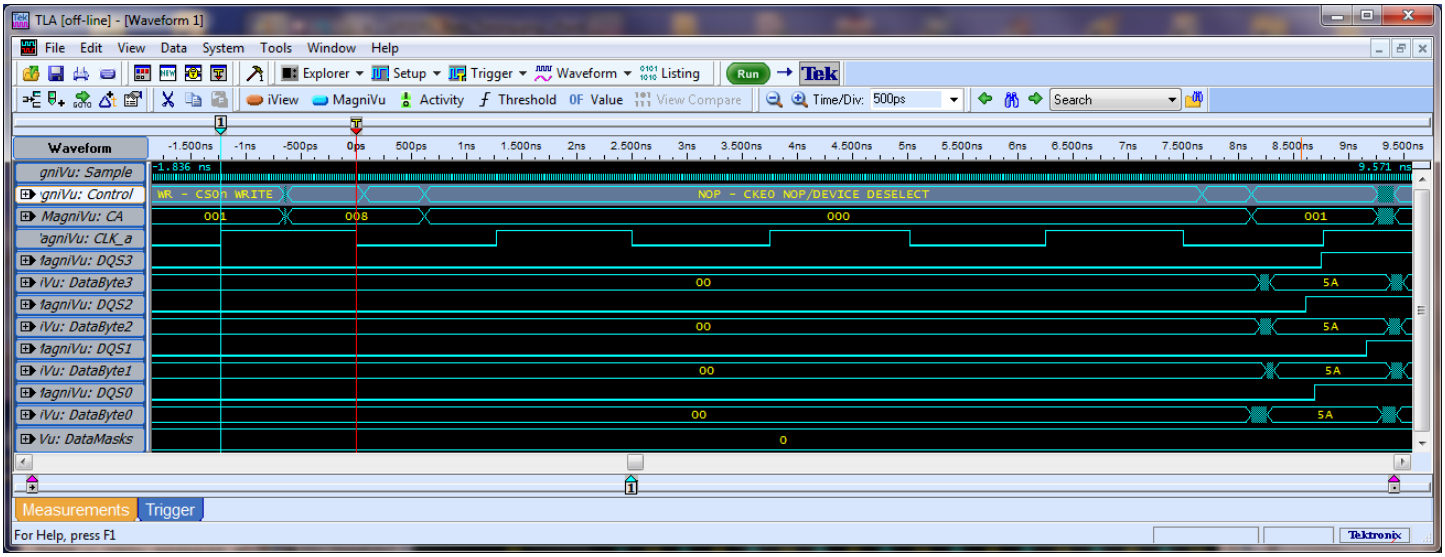


Figure 7 - MagniVu Timing Data

iCapture Analog Mux

A powerful analog validation feature is the Tektronix Logic Analyzer's unique Analog Mux capability. This provides the ability to see *any* channel of the LPDDR2 bus in seconds on an oscilloscope. This is invaluable information which allows analysis within minutes as to the status and behavior of the LPDDR2 bus. No extra probing is required! This information can be pushed back into the logic analyzer, correlated and viewed in a wave form window along with the state or timing data using the iView Feature.

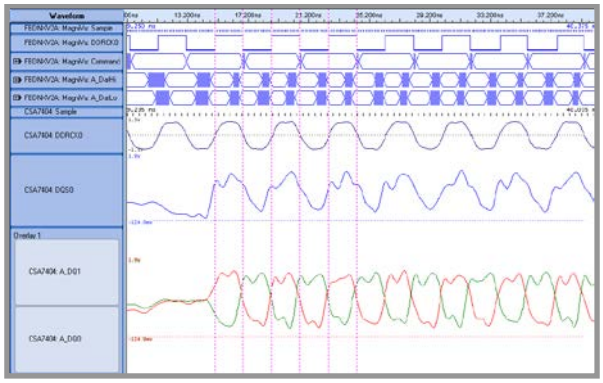


Figure 8 - Example Representation of iView

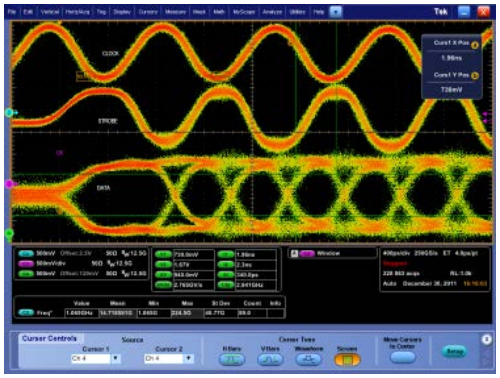


Figure 9 - Example iCapture Analog Mux

Taking advantage of the ultra-high fidelity “Scope Probe per Signal” capability of the LPDDR2 Interposer, iCapture enables focused analog level analysis and validation.

Sample Point Setup

In order for the logic analyzer to capture signals accurately, the sample points must be properly set. iCiS provides a graphical display of the signal eyes on a per group or per signal basis(See Figure 6). You easily select the optimum sample point.

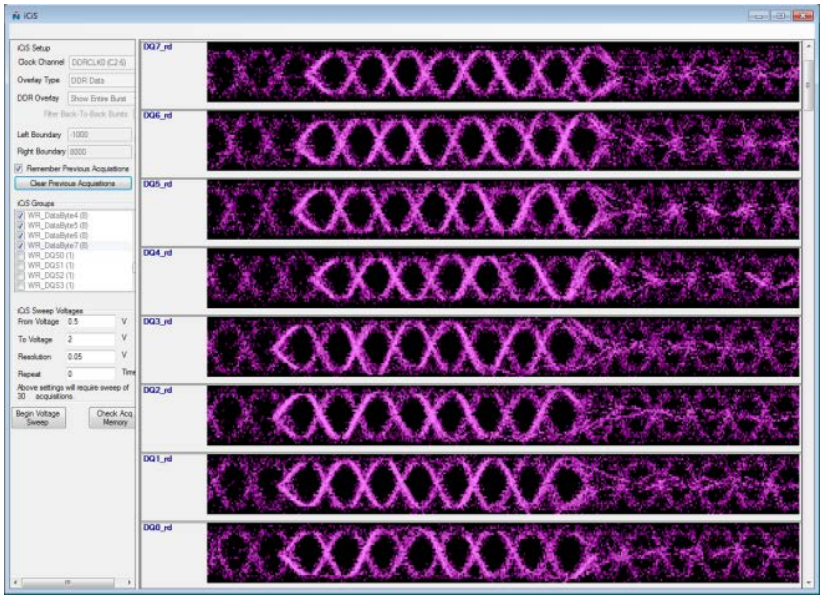


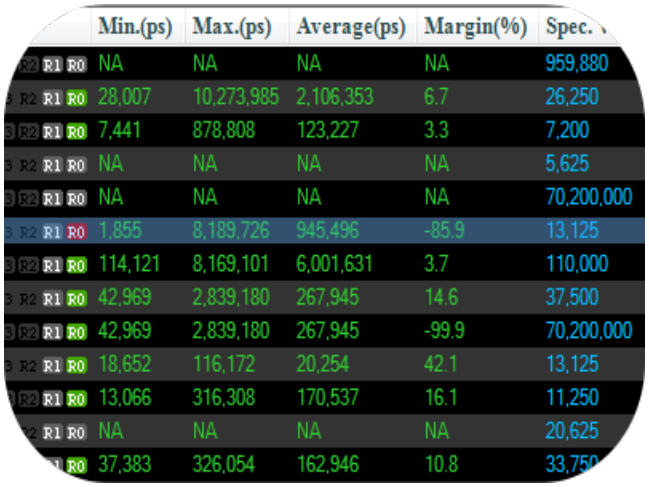
Figure 10 - Example iCiS DQ Data Setup

Setting up the logic analyzer is easy! Load the TLA software, load the support package, and click Run. It's as simple as that for compliance analysis (CMD/ADDR/CTRL acquisition). Acquiring the DQ read and write data is easily done with the graphical iCiS tool.

Compliance Analysis Software

These products optionally include the LPDDR2 Memory Compliance Analysis software package. This software performs advanced command sequence & timing compliance analysis. It also provides statistical information and global bus activity to quickly give the user an overview of the LPDDR2 bus activity without having to revert to a listing or waveform window.

- Extensive JEDEC LPDDR2 Compliance Analysis
- Quick and Easy Setup w/No Calibration Required
- Automated Acquisition and Measurement
- Powerful in-application graphical and tabular analysis results
- Memory controller & JEDEC parameters predefined
- Quickly navigate through multiple acquisitions



	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec.
R2 R1 R0	NA	NA	NA	NA	959,880
R2 R1 R0	28,007	10,273,985	2,106,353	6.7	26,250
R2 R1 R0	7,441	878,808	123,227	3.3	7,200
R2 R1 R0	NA	NA	NA	NA	5,625
R2 R1 R0	NA	NA	NA	NA	70,200,000
R2 R1 R0	1,855	8,189,726	945,496	-85.9	13,125
R2 R1 R0	114,121	8,169,101	6,001,631	3.7	110,000
R2 R1 R0	42,969	2,839,180	267,945	14.6	37,500
R2 R1 R0	42,969	2,839,180	267,945	-99.9	70,200,000
R2 R1 R0	18,652	116,172	20,254	42.1	13,125
R2 R1 R0	13,066	316,308	170,537	16.1	11,250
R2 R1 R0	NA	NA	NA	NA	20,625
R0	37,383	326,054	162,946	10.8	33,750

Figure 11 - Tabular Results Detail of Compliance Analysis

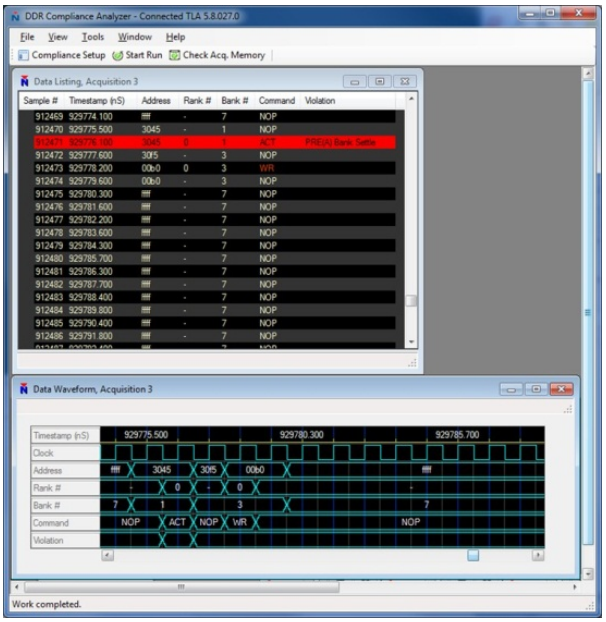


Figure 12 - Waveform & Timing Displays of Compliance Analysis

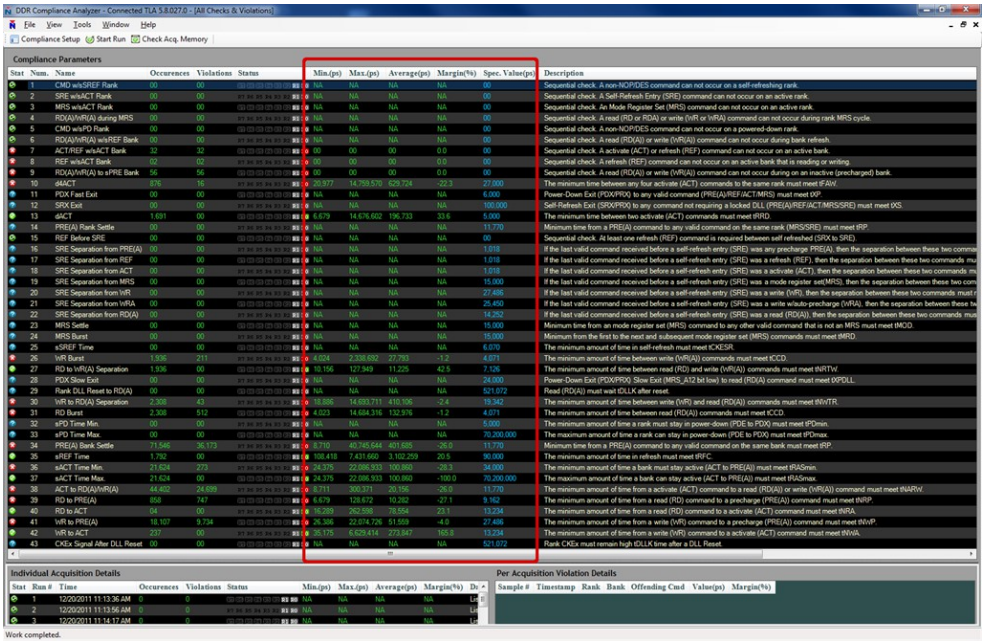


Figure 13 - Detailed Compliance Analysis Results

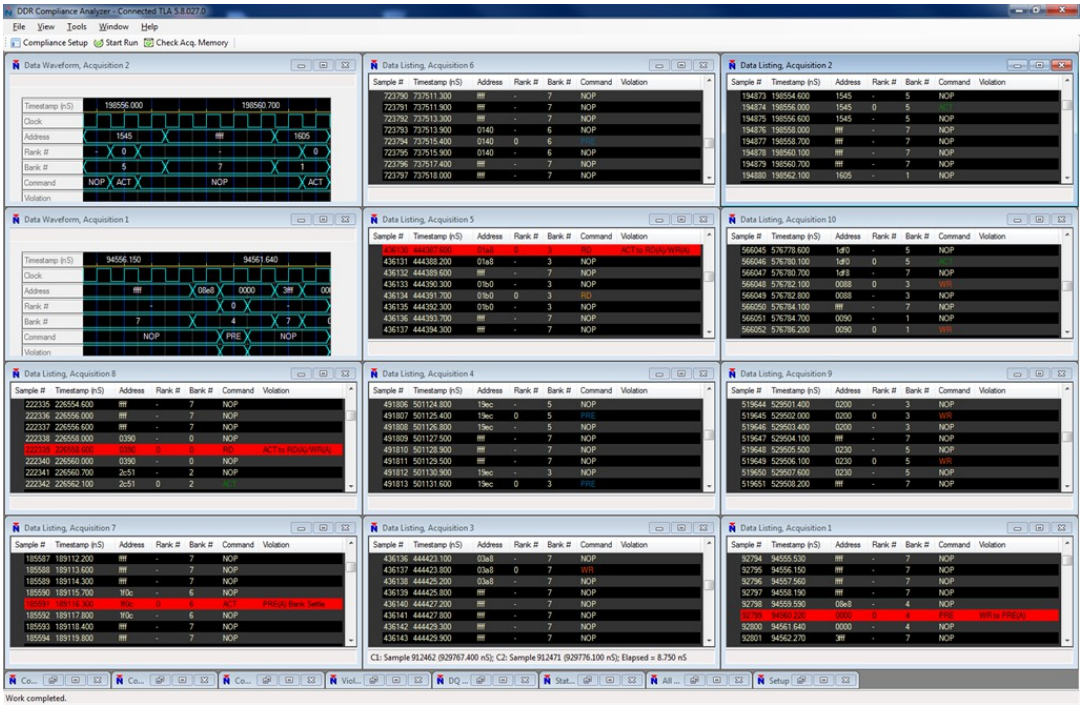


Figure 14 - View Violations in Data Across Many Acquisitions

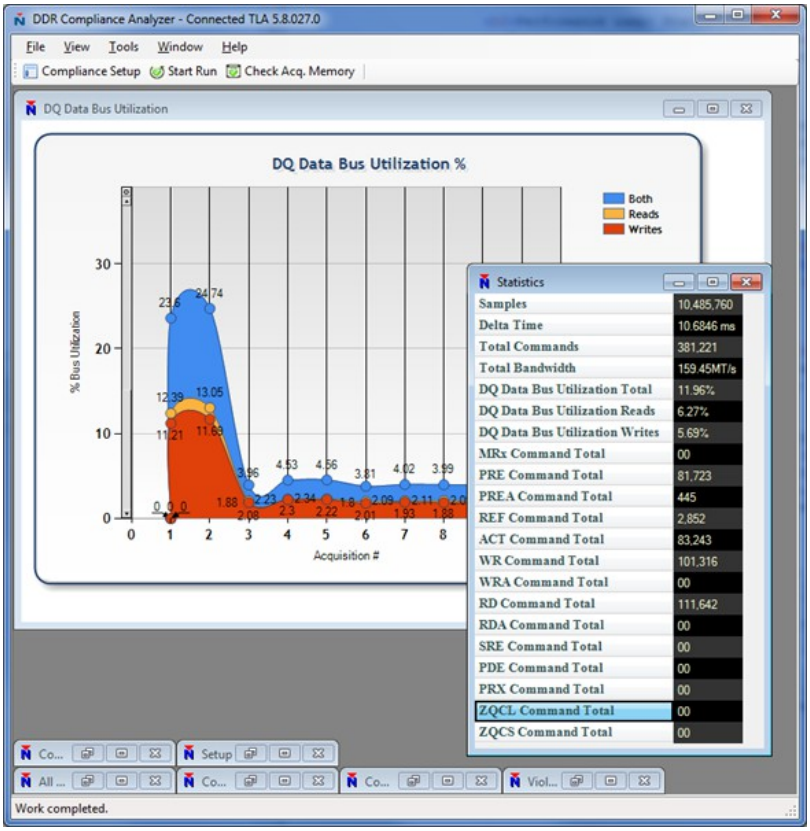


Figure 15 - Bus Utilization Measurements

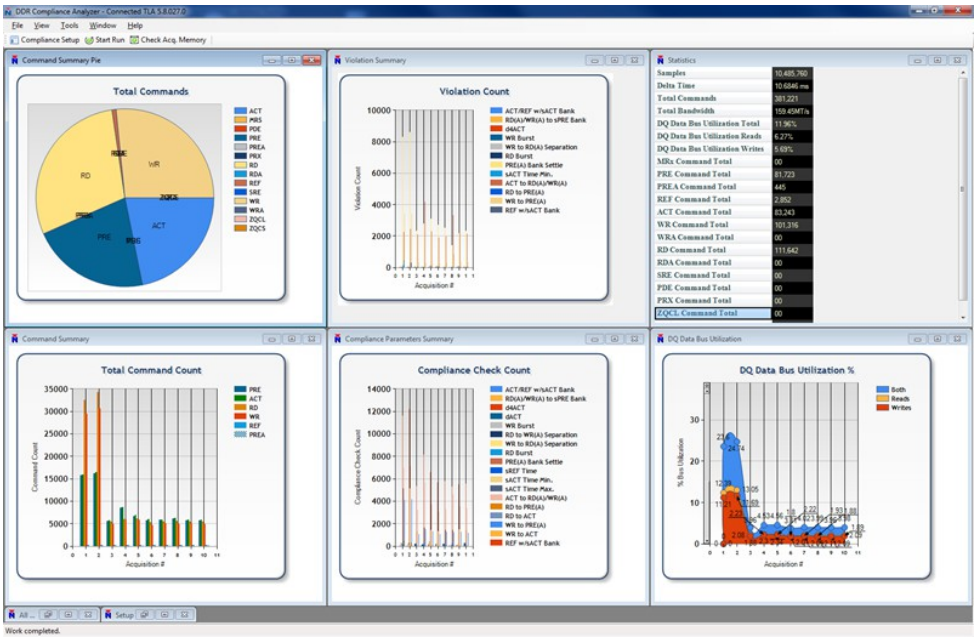


Figure 16 - Graphical and Tabular Compliance Analysis Examples

Nexus Technology LPDDR2 Component Interposer Advantages

Probed at the BGA Pads

The best place to probe a memory bus is at the BGA balls to eliminate reflections associated with break-out board probing, embedded mid-bus probing or other methods. Nexus Technology's component interposers provide easy access to memory component BGA pads for accurate memory bus analysis.

Use with Existing Package-on-Package or Embedded designs

No need to change existing designs. Simply add the interposer to your embedded target or DIMM with no re-design or added probe points. No Need to add probe points to existing designs. Simply add the interposer to your DIMM or embedded target for easy connectivity to the Logic Analyzer.

Interchangeable Socketed Interposers

The interposers are reusable. Once an interposer socket is installed on a target, the interposer can be attached and removed by hand. This allows an interposer to be used on multiple targets, or enables quick swapping of logic analyzer and oscilloscope interposers on the same target. The interposer socket has four posts that are soldered to four mounting holes on the interposer to retain the interposer to the socket.

Easy to Install

Install the interposer socket using industry standard BGA attachment methods or by using Nexus Technology’s Attachment Service. Contact Nexus Technology for further information on our Attachment Service.

Simple Digital and Analog Validation via Standard Interposer Socket

Nexus Technology’s Component interposers are designed for optimal signal integrity. Once our custom socket is installed on your target, our interposers can be easily swapped out. We offer Oscilloscope component interposers for analog validation, and Logic Analyzer component interposers for digital validation.

Product Dimensions

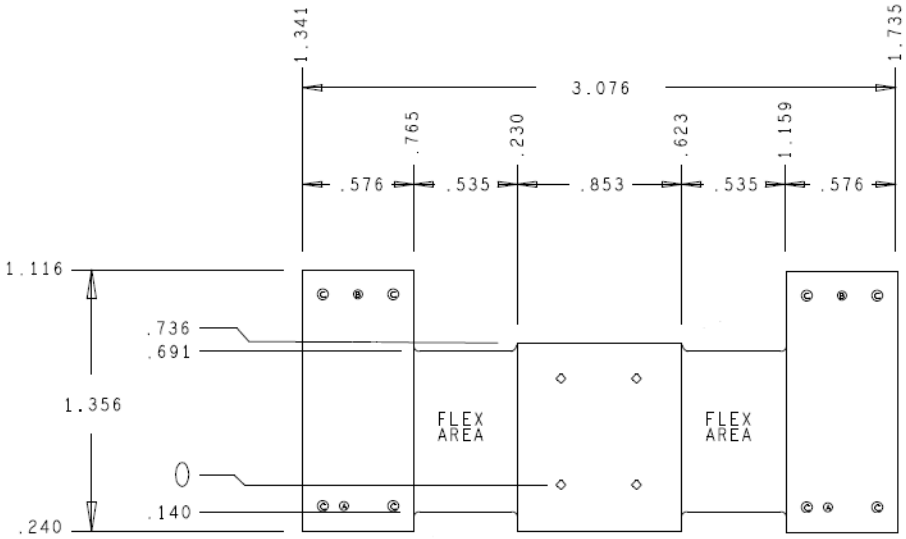
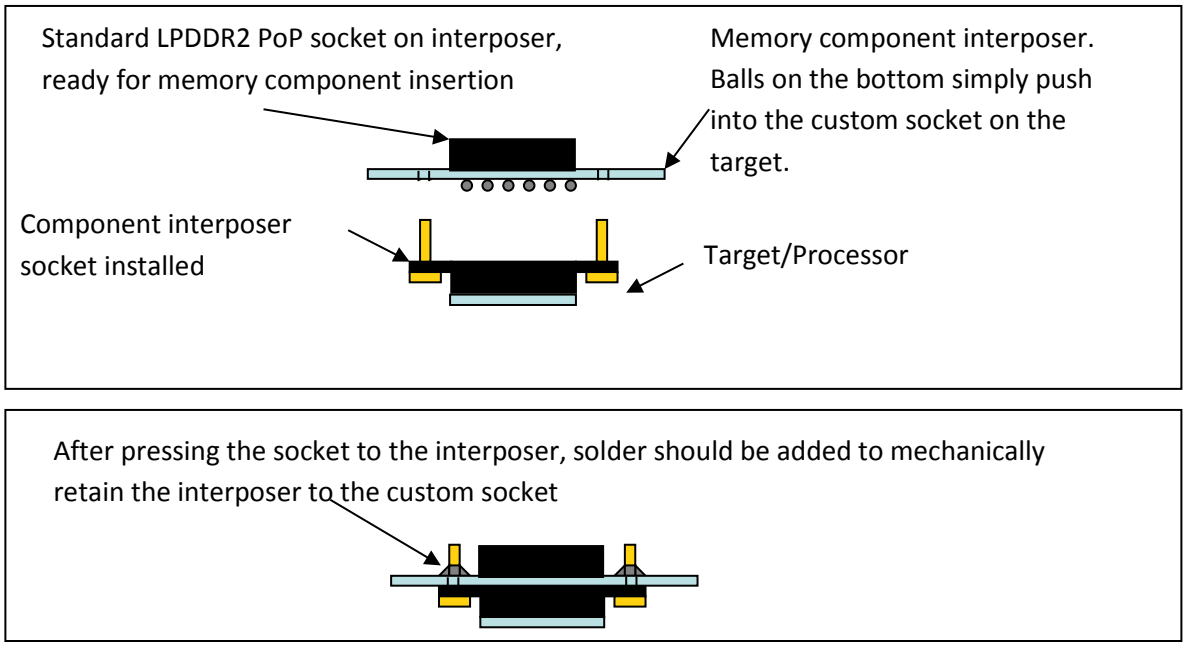


Figure 17 - LPDDR2 168 – ball /4Logic Analyzer Component Interposer Dimensions

Attaching and Reusing Interposers



LPDDR2 PoP 168 Ball Logic Analyzer Component Interposer

Configuration Tables

LPDDR2 PoP 168 Ball Logic Analyzer Interposers

Nomenclature	Interposer Type	Data Width	Component Socket Included	Nexus Probes Included	Installation Service Included	Hardware Requirements
NEX-LPDDR2PoP168BLASK	Logic Analyzer	x32	Yes	No[1]	No	1- TLA7000 Series Mainframe 1- TLA7Bx4 1.4 GHz Acquisition Card 1- NEX-PRB1XL Probe & 1- NEX-PRB2XL Probe OR 2- NEX-PRB1XL Probes
NEX-LPDDR2PoP168BLASK-AT	Logic Analyzer	x32	Yes	No[1]	Yes	
NEX-LPDDR2PoP168BLASKPR	Logic Analyzer	x32	Yes	Yes[1]	No	
NEX-LPDDR2PoP168BLASKPR-AT	Logic Analyzer	x32	Yes	Yes[1]	Yes	

Optional Additional LPDDR2 PoP 168 Ball Interposer Sockets

Nomenclature	Data Width	Solder Balls Added	Quantity of Sockets
NEX-LP2-168BGASKBA	x32	Yes	1
NEX-LP2-168BGASKBA-3	x32	Yes	3

Product Support

Product Support is critical to your success. Our engineering staff can provide expert training and support tailored to your specific needs. Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

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