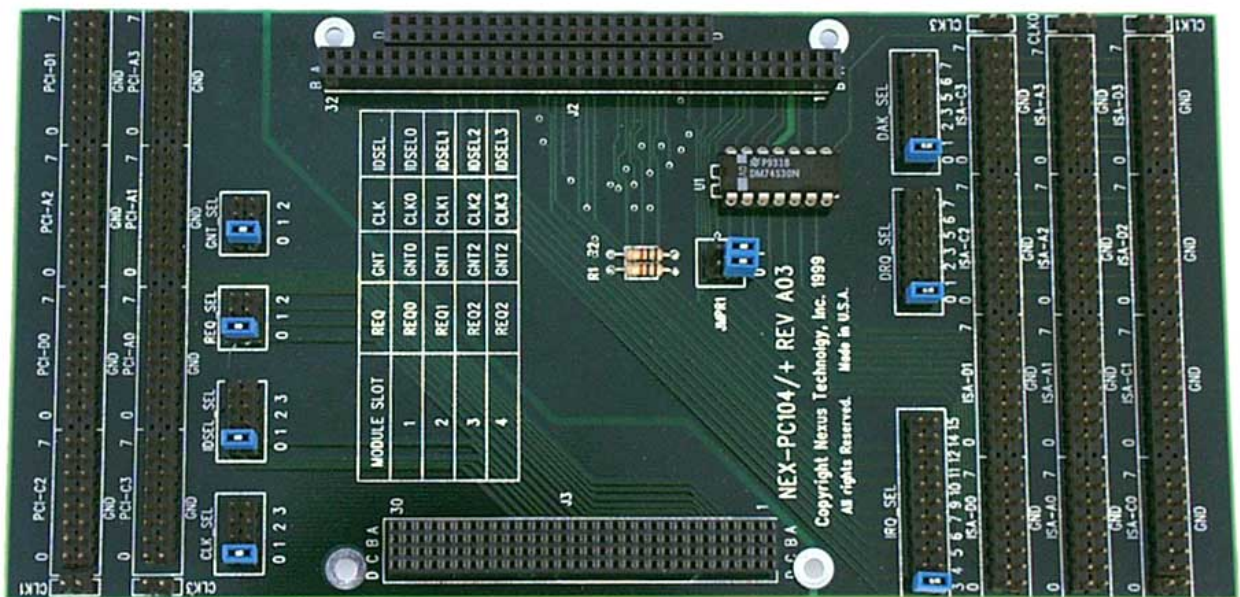


NEX-PC104, NEX-PC104+



- NEX-PC104: 8 and 16-bit PC104/ISA support
- NEX-PC104+: PC104 support plus PC104+/PCI
- Quick convenient connection to the PC104 or PC104+ bus
- Symbolic Disassembly of the 8 or 16-bit PC104/ISA Bus
- Disassembly of the PC104+/PCI Bus
 - Cycle Identification
 - Config Cycle decoding including register evaluation
 - Ability to selectively ignore Idle and Wait States
- Extender card design
- Timing Analysis to 8GHz (125ps) on each channel
- Logic Analyzer Setup Software gets you up and running fast
- Simultaneous State and Timing acquisition on each channel
- Trigger on setup/hold violations on all channels

General Description

NEX-PC104 and NEX-PC104+ are separate products. Please review the descriptions and select the appropriate product for the application.

NEX-PC104 / PC104+ Adapter Module

The same adapter card is supplied with the NEX-PC104 and NEX-PC104+ product. This adapter provides a quick convenient connection to the Tektronix TLA600 and TLA700 logic analyzers. It requires the use of four (68-channels) or six (102 channels) Tektronix P6417/18 probes for connection to the TLA600/700.

The PC104 / ISA support requires a 68 or 102 channel acquisition module. When used with a 68 channel acquisition module the user must jumper select one channel from each of the following groups: IRQ, DRQ and DAK. For example you could select IRQ3, DRQ3 and DAK3 for acquisition and display. When using a 102 channel acquisition module or greater all of the IRQ, DRQ and DAK signals are acquired and displayed. The adapter plugs into an 8 or 16-bit PC104 backplane.

The PC104+ / PCI support requires 68 channels of acquisition. Jumpers must be selected to determine the monitoring of the appropriate PC104+ module slot.

PC104 / PC104+ Software

PC104 / ISA: The included 68PC104 (68 channel support) and 102PC104 (102 channel support) provides intelligent clocking of the PC104 bus and symbolic translation of the acquired data. For example MEMW, IOR and SMEMR cycles are identified.

PC104+ / PCI: The included PC104PCI disassembly software (included with NEX-PC104+) executes on the Tektronix Logic Analyzer. This software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler. All PC104+ Cycle types are identified and Config cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text (see Fig. 1). Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE disk, Video controller, network interface, etc.) is being accessed (see Fig. 1).

It is also possible to filter the data display to show only those cycle types of interest. The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest. Figure 4 shows the same area of acquired data as that in Figure 1, but with Memory and I/O cycles suppressed

Another feature of the disassembly software is its ability to intelligently acquire PC104+ data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the disassembly software is able to acquire only the PC104+ bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes the user also has the ability to override this function and acquire data on every PC104+ CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Timing Analysis

The TLA600/700 Logic Analyzer can acquire timing data at 8GHz (125ps) on each channel. Fast timing acquisition and low capacitive loading (the passive NEX-PC104 / PC104+ adapter module and the < 2pf/P6434 and 0.7pf/P6860 logic analyzer probe) provide excellent timing analysis on each monitored channel of the PC104 / PC104+ bus.

Timestamp

All acquired data is timestamped on Tektronix logic analyzers; no acquisition memory is used to accomplish this. The timestamp resolution on the TLA600/700 is 125ps.

Correlation

While the NEX-PC104 / PC104+ package is being used with a Tektronix logic analyzer to monitor the PC104+ activity, another acquisition module can be used to monitor activity elsewhere within the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred. For instance, the system microprocessor could be monitored and correlated with bus activity to verify CPU and PC104+ bus communication.

Setup/Hold Triggering

Setup and hold specifications can be verified, and margins tested with 125ps resolution, using the TLA600/700. Each channel group (address, control, etc..) or individual channel can have a different setup time and hold time violation set as a fault trigger. If any individual channel or channel in a group is ever in violation of the specified setup and hold time, the logic analyzer will stop and show the violation.

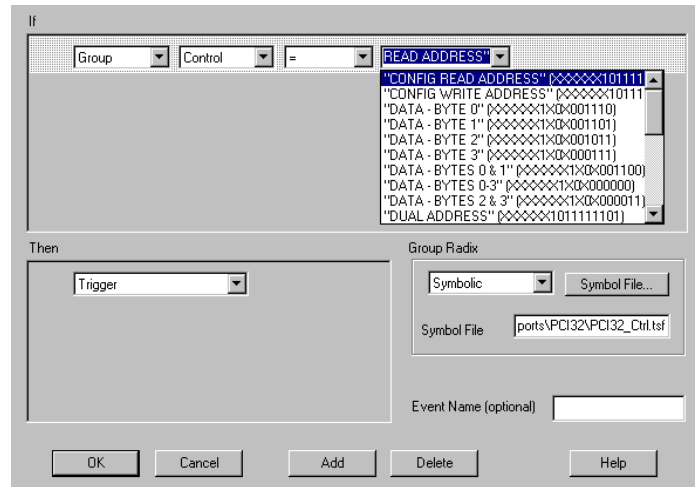
Simultaneous State and Timing Acquisition

The Tektronix TLA600/700 Logic Analyzer offers the unique capability of being able to acquire timing and state data through the same probes at the same time. For example, a user is able to view timing data acquired at 125ps resolution, with state data acquired synchronously (for instance, using NEX-PC104 / PC104+ custom clocking or clocking on every rising edge of CLK). This resolution gives the hardware designer the ability to easily determine edge relationships between any signal without having to deal with the inconvenience and loading problems that are inherent when forced to double-probe with individual state and timing acquisition cards.

Disassembly (State Analysis)

Sample	PCI32X Addr_Dat	PCI32X Mnemonics	Timestamp
	03000043	Class 0x03 - Display controller	
	03000043	Sub-Class 0x00	
	03000043	Prog. I/F 0x00 - VGA compatible	
	03000043	Revision ID 67	
814	00000CF8	I/O WRITE ADDRESS	29.693,500 us
815	80008808	I/O WRITE DATA	90.000 ns
816	10000008	CONFIG READ ADDRESS	2.526,500 us
	10000008	Type 0 Register 2 Function 0	
817	03000043	CONFIG READ DATA	150.500 ns
	03000043	Class 0x03 - Display controller	
	03000043	Sub-Class 0x00	
	03000043	Prog. I/F 0x00 - VGA compatible	
	03000043	Revision ID 67	
818	000C0000	MEMORY READ ADDRESS	23.316,500 us
819	----FFFF	MEMORY READ DATA	2.044,500 us
820	00000CF8	I/O WRITE ADDRESS	14.939,329,500 ns
821	80008804	I/O WRITE DATA	90.500 ns
822	10000004	CONFIG READ ADDRESS	1.684,500 us
	10000004	Type 0 Register 1 Function 0	
823	-----00	CONFIG READ DATA	150.500 ns
	-----00	Wait Cycle disabled	
	-----00	Parity Errors disabled	
	-----00	VGA Palette Snoop disabled	
	-----00	Mem Write & Inv. disabled	
	-----00	Special Cycle Recog. disabled	
	-----00	Master disabled	

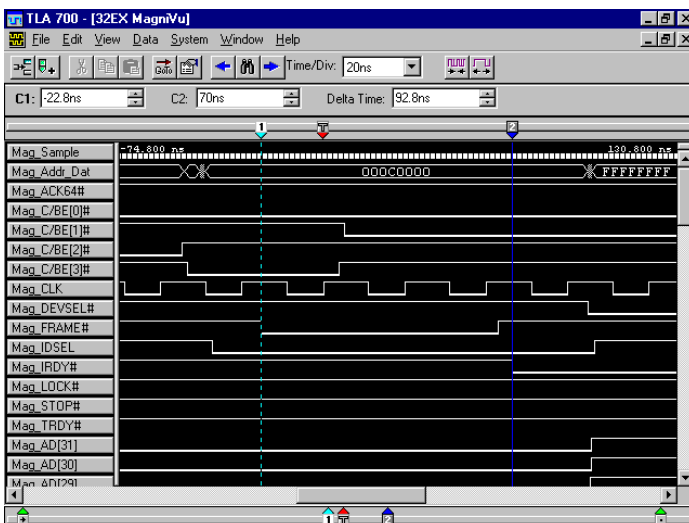
Triggering



PC104+ cycles are identified and Config cycles are decoded. Device information is translated according to Class, sub-Class, and Type.

Trigger on pre-defined PC104+ cycles

Timing Analysis



125ps acquisition on each channel provides excellent timing analysis. Each channel is labeled with the appropriate PC104+ signal name.

Disassembly (with Data Filtering)

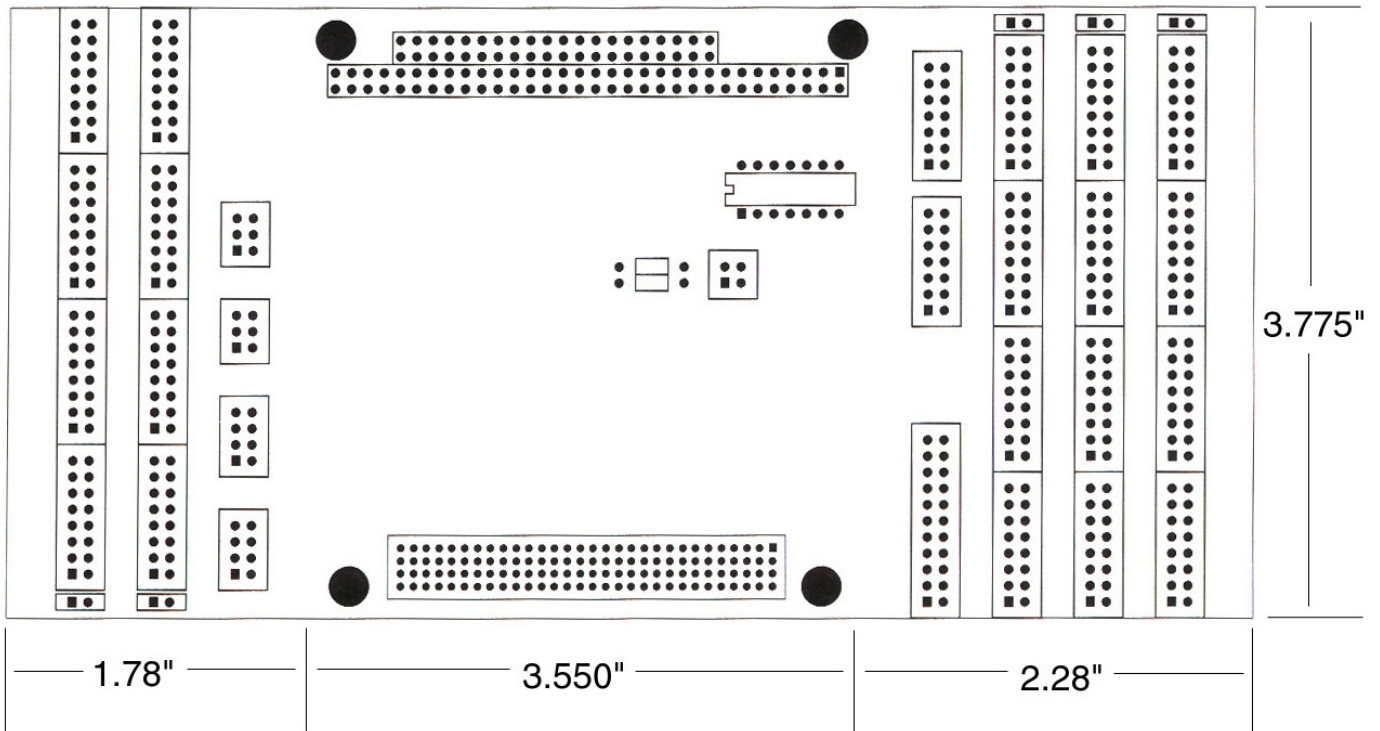
Sample	PCI32X Addr_Dat	PCI32X Mnemonics	Timestamp
812	10000008	CONFIG READ ADDRESS	216.453,000 us
	10000008	Type 0 Register 2 Function 0	
813	03000043	CONFIG READ DATA	150.500 ns
	03000043	Class 0x03 - Display controller	
	03000043	Sub-Class 0x00	
	03000043	Prog. I/F 0x00 - VGA compatible	
	03000043	Revision ID 67	
816	10000008	CONFIG READ ADDRESS	32.310,000 us
	10000008	Type 0 Register 2 Function 0	
817	03000043	CONFIG READ DATA	150.500 ns
	03000043	Class 0x03 - Display controller	
	03000043	Sub-Class 0x00	
	03000043	Prog. I/F 0x00 - VGA compatible	
	03000043	Revision ID 67	
822	10000004	CONFIG READ ADDRESS	14.966,465,500 us
	10000004	Type 0 Register 1 Function 0	
823	-----00	CONFIG READ DATA	150.500 ns
	-----00	Wait Cycle disabled	
	-----00	Parity Errors disabled	
	-----00	VGA Palette Snoop disabled	
	-----00	Mem Write & Inv. disabled	
	-----00	Special Cycle Recog. disabled	
	-----00	Master disabled	
	-----00	Memory Access disabled	
	-----00	I/O Access disabled	
826	10000004	CONFIG WRITE ADDRESS	15.617,000 us

Disassembly display with Memory and I/O cycles suppressed.

Tektronix Logic Analyzers Supported

A TLA600 or TLA700 with a minimum of 68 channel acquisition card. A 102 channel acquisition card is required to acquire all of the PC104 IRQ/DRQ and DAK signals.

Mechanical Outline



Ordering / Contact Information

Part Number NEX-PC104

Includes: NEX-PC104/+ adapter
PC104: 8 & 16-bit PC104 / ISA analysis software (68 and 102 channel versions included)
Manual

Part Number NEX-PC104+

Includes the NEX-PC104 support described above and adds PC104+ / PCI software support for the PC104+ bus.
Manual

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Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

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