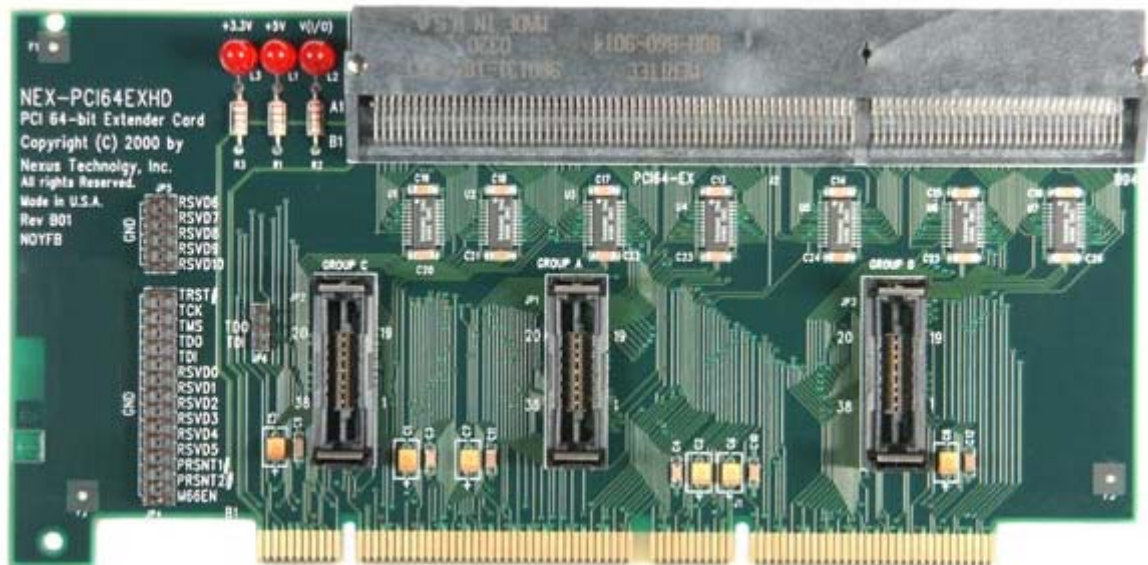

NEX-PCI64EXHD3/5



- High Density connectors provide quick convenient connection to the PCI bus
- Disassembly of the PCI Bus
 - Cycle Identification
 - Config Cycle decoding including register evaluation
 - Ability to selectively ignore Idle and Wait States
- Extender card design
- Logic Analyzer Setup Software gets you up and running fast
- Unique features when using a TLA600 or TLA700
 - Timing Analysis to 8GHz (125ps) on each channel
 - Simultaneous State and Timing acquisition on each channel
 - Trigger on setup/hold violations on all channels

General Description

The included NEX-PCI32X and NEX-PCI64X disassembly software executes on the Tektronix Logic Analyzer. This software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler. All PCI Cycle types are identified and Config cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text (see Fig. 1). Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE disk, Video controller, network interface, etc.) is being accessed (see Fig. 1).

It is also possible to filter the data display to show only those cycle types of interest. The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest. Figure 4 shows the same area of acquired data as that in Figure 1, but with Memory and I/O cycles suppressed. Another feature of the disassembly software is its ability to intelligently acquire PCI data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the disassembly software is able to acquire only the PCI bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes the user also has the ability to override this function and acquire data on every PCI CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Timing Analysis

Timing analysis of the PCI bus can be done at the maximum asynchronous rate of the Tektronix Logic Analyzer. For example the TLA600/700 system with a minimum of 102 channel module can acquire timing data at 8GHz (125ps) on each channel. Fast timing acquisition and low capacitive loading (the passive NEX-PCI64EXHD5/3 adapter module and the < 2pf/P6434 and 0.7pf/P6860) provide excellent timing analysis on each monitored channel of the PCI bus.

NEX-PCI64EXHD5/3 Adapter Module

The NEX-PCI64EXHD5/3 adapter provides a quick convenient connection to standard Tektronix logic analyzers. It requires the use of three Tektronix P6434/P6860 high density probes for connection to the TLA600/700 or a DASMTIF for connection to a DAS/TLA500.

The NEX-PCI64EXHD5/3 extends the PCI bus approximately 3.5 inches in etch length. The Logic Analyzer attaches to the NEX-PCI64EXHD adapter using a high density impedance matched connector. The typical Logic Analyzer loading is < 2pf/P6434 and 0.7pf/P6860. High speed Schottky clamping diodes have been added to prevent the extra etch length from causing unwanted reflections.

The NEX-PCI64EXHD5/3 adapter is available for 5 volt (NEX-PCI64EXHD5) and 3.3 volt (NEX-PCI64EXHD3) applications. Please specify the proper part number when ordering.

Timestamp

All acquired data is timestamped on Tektronix logic analyzers; no acquisition memory is used to accomplish this. The timestamp resolution on the TLA600/700 system is 125ps, and 10ns on the DAS9200 and TLA510/20.

Correlation

While the NEX-PCI64EXHD5/3 package is being used with a Tektronix logic analyzer to monitor the PCI activity, another acquisition module can be used to monitor activity elsewhere within the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred. For instance, the system microprocessor could be monitored and correlated with bus activity to verify CPU and PCI bus communication.

Setup/Hold Triggering

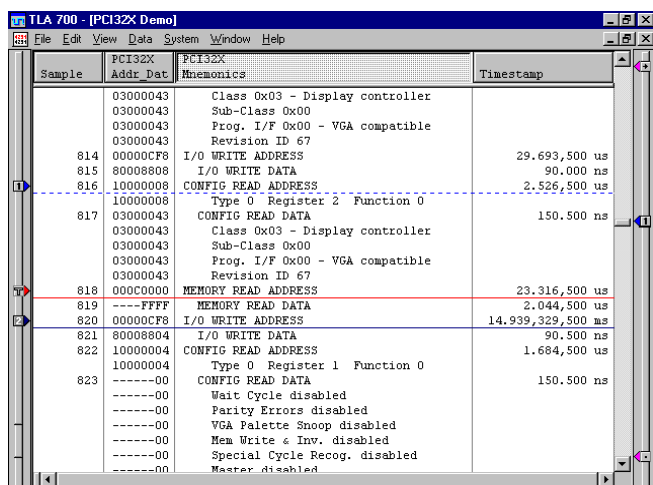
Setup and hold specifications can be verified, and margins tested, using the TLA600/700. Each channel group (address, data, control, etc..) or individual channel can have a different setup time and hold time violation set as a fault trigger. If any individual channel or any channel in a group is ever in violation of the specified setup and hold time, the logic analyzer will stop and show the violation. The timing resolution of the acquired data at the violation point is 8GHz (125ps).

Setup and hold margin testing can be done by altering the setup and hold times set for the violation trigger in 125ps increments. Changing these values until a violation occurs will show the actual setup and hold of the system under test.

Simultaneous State and Timing Acquisition

The Tektronix TLA600/700 Logic Analyzer offers the unique capability of being able to acquire timing and state data through the same probes at the same time. For example, a user is able to view timing data acquired at 125ps resolution, with state data acquired synchronously (for instance, using NEX-PCI64EXHD5/3 custom clocking or clocking on every rising edge of CLK). This resolution gives the hardware designer the ability to easily determine edge relationships between any signal without having to deal with the inconvenience and loading problems that are inherent when forced to double-probe with individual state and timing acquisition cards.

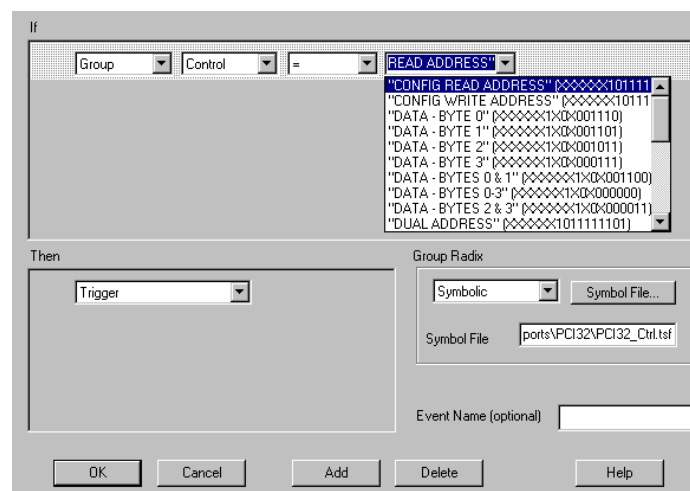
Disassembly (State Analysis) Triggering



Sample	Addr. Dat	Mnemonics	Timestamp
03000043		Class 0x03 - Display controller	
03000043		Sub-Class 0x00	
03000043		Prog. I/F 0x00 - VGA compatible	
03000043		Revision ID 67	
814	00000CF8	I/O WRITE ADDRESS	29.693,500 us
815	80008808	I/O WRITE DATA	90.000 ns
816	10000008	CONFIG READ ADDRESS	2.526,500 us
10000008		Type 0 Register 2 Function 0	
817	03000043	CONFIG READ DATA	150.500 ns
03000043		Class 0x03 - Display controller	
03000043		Sub-Class 0x00	
03000043		Prog. I/F 0x00 - VGA compatible	
03000043		Revision ID 67	
818	000C0000	MEMORY READ ADDRESS	23.316,500 us
819	-----FFFF	MEMORY READ DATA	2.044,500 us
820	00000CF8	I/O WRITE ADDRESS	14.939,329,500 ns
821	80008804	I/O WRITE DATA	90.500 ns
822	10000004	CONFIG READ ADDRESS	1.684,500 us
10000004		Type 0 Register 1 Function 0	
823	-----00	CONFIG READ DATA	150.500 ns
-----00		Wait Cycle disabled	
-----00		Parity Errors disabled	
-----00		VGA Palette Snoop disabled	
-----00		Mem Write & Inv. disabled	
-----00		Special Cycle Recog. disabled	
-----00		Master disabled	

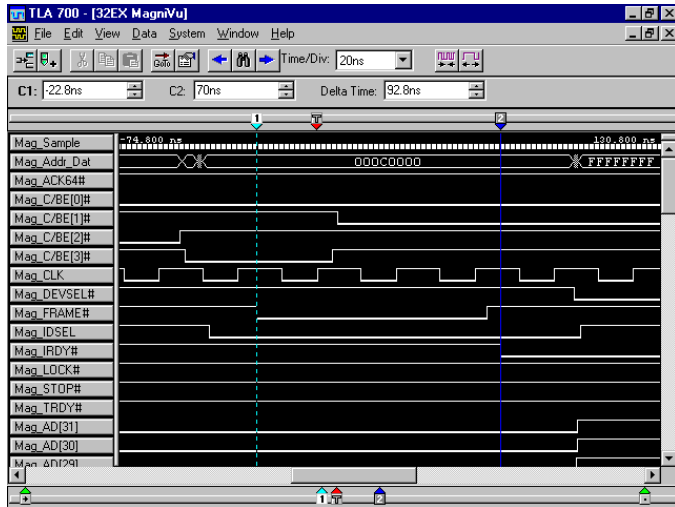
PCI cycles are identified and Config cycles are decoded. Device information is translated according to Class, sub-Class and Type.

Triggering



Trigger on pre-defined PCI cycles

Timing Analysis



125ps acquisition on each channel provides excellent timing analysis. Each channel is labeled with the appropriate PCI signal name. Bus format display of grouped signals shown.

Disassembly (with Data Filtering)

Sample	PCI32X Addr	PCI32X Dat	PCI32X Mnemonics	Timestamp
812	10000008		CONFIG READ ADDRESS	216.453,000 us
	10000008		Type 0 Register 2 Function 0	
813	03000043		CONFIG READ DATA	150.500 ns
	03000043		Class 0x03 - Display controller	
	03000043		Sub-Class 0x00	
	03000043		Prog. I/F 0x00 - VGA compatible	
	03000043		Revision ID 67	
816	10000008		CONFIG READ ADDRESS	32.310,000 us
	10000008		Type 0 Register 2 Function 0	
817	03000043		CONFIG READ DATA	150.500 ns
	03000043		Class 0x03 - Display controller	
	03000043		Sub-Class 0x00	
	03000043		Prog. I/F 0x00 - VGA compatible	
	03000043		Revision ID 67	
822	10000004		CONFIG READ ADDRESS	14.966,465,500 ms
	10000004		Type 0 Register 1 Function 0	
823	-----00		CONFIG READ DATA	150.500 ns
	-----00		Wait Cycle disabled	
	-----00		Parity Errors disabled	
	-----00		VGA Palette Snoop disabled	
	-----00		Mem Write & Inv. disabled	
	-----00		Special Cycle Recog. disabled	
	-----00		Master disabled	
	-----00		Memory Access disabled	
	-----00		I/O Access disabled	
826	10000004		CONFIG WRITE ADDRESS	15.617,000 us

Same disassembly display with Memory and I/O cycles suppressed.

Tektronix Logic Analyzers Supported

TLA600 or TLA700 with a minimum of 102 channel acquisition module (requires 3-P6434/P6860 probes from Tektronix)

TLA510 or TLA520 (1 acquisition module used: requires one DASMTIF probe adapter from Tektronix)

DAS9200 with a 92A96 or 92C96 (any memory depth: requires 1 DASMTIF Tektronix probe adapter)

Mechanical Outline



Ordering / Contact Information

Part Number NEX-PCI64EXHD3 3.3 Volt 32-bit PCI Bus Support & Analysis Software

Part Number NEX-PCI64EXHD5 5 Volt 32-bit PCI Bus Adapter & Analysis Software

Both include: NEX-PCI64EXHD 32-bit Adapter Board (3.3 or 5 volt version)
NEX-PCI32X and NEX-PCI64X Software for: DAS9200, TLA510/520 3 1/2" floppy,
TLA704/711 3 1/2" floppy
Support for DAS9200 5 1/4" drive available upon request

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techsupport@nexustechnology.com

Website: www.nexustechnology.com

Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

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