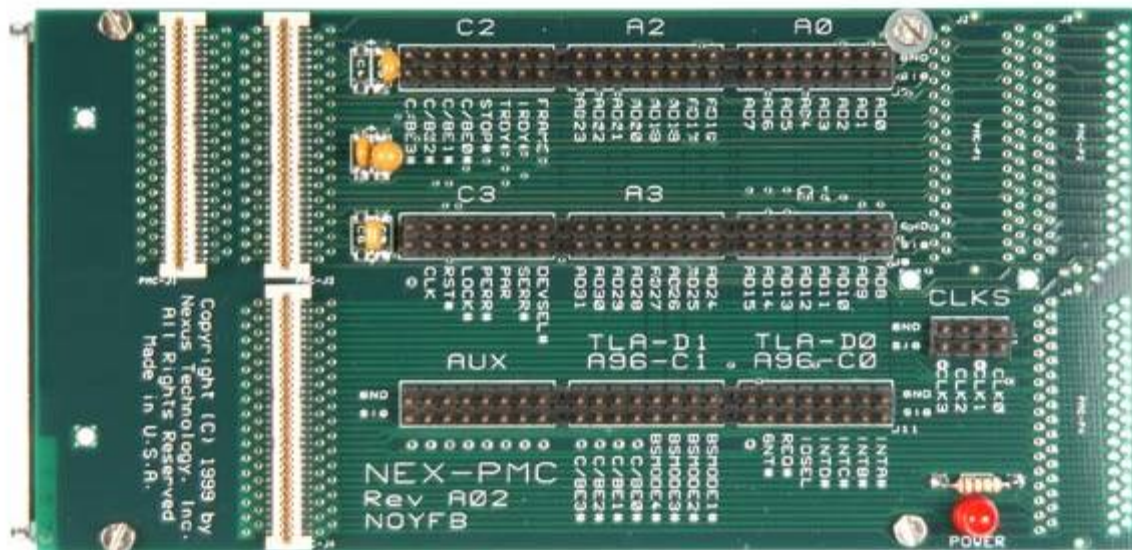


NEX-PMC



- Quick Convenient Connection to the PMC bus
- Disassembly of the PMC Bus
 - Cycle Identification
 - Config Cycle decoding including register evaluation
 - Ability to selectively ignore Idle and Wait States
- Extender Card Design
- Logic Analyzer Setup S/W gets you up and running fast
- Unique features available when using the TLA600 or TLA700
 - Timing Analysis to 8GHz (125ps) on each Channel
 - Simultaneous State and Timing Acquisition on each Channel
 - Trigger on setup/hold violations on all Channels

General Description

PMC Disassembly Software

The included NEX-PMC disassembly software executes on the Tektronix Logic Analyzer. This software decodes bus transactions and displays information in easily understood text form, just like a typical Tektronix microprocessor disassembler. All PMC Cycle types are identified and Config cycles are decoded to reflect the meaning of the registers. For instance, Command and Status registers are completely evaluated, with each bit's state being presented in easy-to-read text (see Fig. 1). Device information is translated according to Class, sub-Class, and Type to inform the user as to what device (IDE disk, Video controller, network interface, etc.) is being accessed (see Fig. 1).

It is also possible to filter the data display to show only those cycle types of interest. The user can choose to display or suppress Memory, I/O, or Config cycles to permit easy and quick analysis of only those cycles of interest. Figure 4 shows the same area of acquired data as that in Figure 1, but with Memory and I/O cycles suppressed

Another feature of the disassembly software is its ability to intelligently acquire PMC data. By taking advantage of the data clocking power built in to the Tektronix Logic Analyzers the disassembly software is able to acquire only the PMC bus cycles and ignore Idle and Wait states. This means that the user is able to make optimum use of the acquisition card's memory and see more bus transactions. For debug purposes the user also has the ability to override this function and acquire data on every PMC CLK rising edge to permit the user to see all of the bus traffic including the Idle and Wait states.

Timing Analysis

Timing analysis of the PMC bus can be done at the maximum asynchronous rate of the Tektronix Logic Analyzer. For example the TLA600 or TLA700 system with a minimum of 68 channels can acquire timing data at 8GHz (125ps) on each channel. Fast timing acquisition and low capacitive loading (the passive NEX-PMC adapter module and the < 2pf/P6434 and 0.7pf/P6860 logic analyzer probe) provide excellent timing analysis on each monitored channel of the PMC bus.

NEX-PMC Adapter Module

The NEX-PMC adapter provides a quick convenient connection to standard Tektronix logic analyzers. The NEX-PMC adapter is an extender card. It occupies the same slot as the PMC module under test.

Timestamp

All acquired data is timestamped on Tektronix logic analyzers; no acquisition memory is used to accomplish this. The timestamp resolution on the TLA600/700 system is 125ps, and 10ns on the DAS9200 and TLA510/20.

Correlation

While the NEX-PMC package is being used with a Tektronix logic analyzer to monitor the PMC activity, another acquisition module can be used to monitor activity elsewhere within the system. The results of the two acquisitions can be correlated in time to determine the sequence of actions that occurred. For instance, the system microprocessor could be monitored and correlated with bus activity to verify CPU and PMC bus communication.

Setup/Hold Triggering

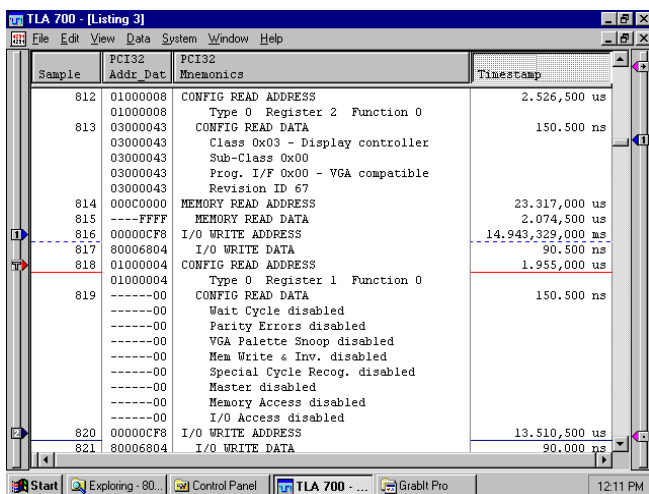
Setup and hold specifications can be verified, and margins tested, using the TLA600/TLA700 system. Each channel group (address, data, control, etc..) or individual channel can have a different setup time and hold time violation set as a fault trigger. If any individual channel or any channel in a group is ever in violation of the specified setup and hold time, the logic analyzer will stop and show the violation. The timing resolution of the acquired data at the violation point is 8GHz (125ps).

Setup and hold margin testing can be done by altering the setup and hold times set for the violation trigger in 500ps increments. Changing these values until a violation occurs will show the actual setup and hold of the system under test.

Simultaneous State and Timing Acquisition

The Tektronix TLA600/700 Logic Analyzer offers the unique capability of being able to acquire timing and state data through the same probes at the same time. For example, a user is able to view timing data acquired at 125ps resolution, with state data acquired synchronously (for instance, using NEX-PMC custom clocking or clocking on every rising edge of CLK). This resolution gives the hardware designer the ability to easily determine edge relationships between any signal without having to deal with the inconvenience and loading problems that are inherent when forced to double-probe with individual state and timing acquisition cards.

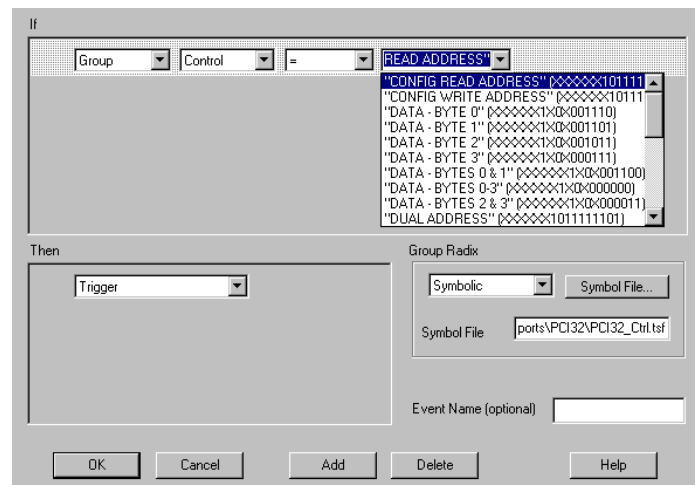
Disassembly (State Analysis)



Sample	PCI32 Addr_Dat	PCI32 Mnemonics	Timestamp
812	01000008	CONFIG READ ADDRESS	2.526,500 us
01000008		Type 0 Register 2 Function 0	
813	03000043	CONFIG READ DATA	150.500 ns
03000043		Class 0x03 - Display controller	
03000043		Sub-Class 0x00	
03000043		Prog. I/F 0x00 - VGA compatible	
03000043		Revision ID 67	
814	000C0000	MEMORY READ ADDRESS	23.317,000 us
815	-----FFFF	MEMORY READ DATA	2.074,500 us
816	00000CF8	I/O WRITE ADDRESS	14.943,329,000 ns
817	80006804	I/O WRITE DATA	90.500 ns
818	01000004	CONFIG READ ADDRESS	1.955,000 us
01000004		Type 0 Register 1 Function 0	
819	-----00	CONFIG READ DATA	150.500 ns
-----00		Wait Cycle disabled	
-----00		Parity Errors disabled	
-----00		VGA Palette Snoop disabled	
-----00		Mem Write & Inv. disabled	
-----00		Special Cycle Recog. disabled	
-----00		Master disabled	
-----00		Memory Access disabled	
-----00		I/O Access disabled	
820	00000CF8	I/O WRITE ADDRESS	13.510,500 us
821	80006804	I/O WRITE DATA	90.000 ns

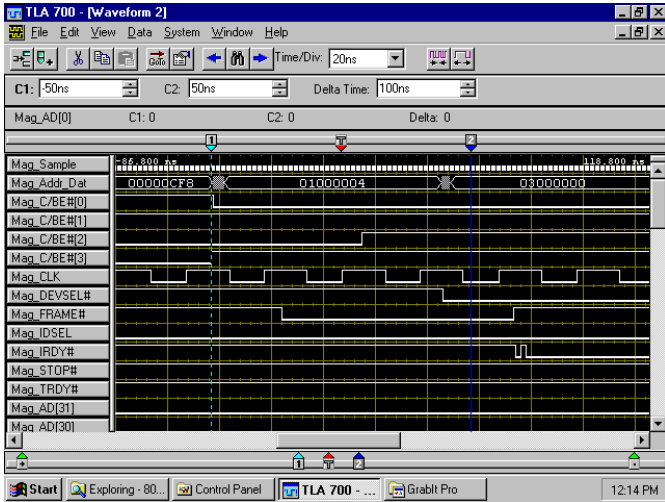
PMC cycles are identified and Config cycles are decoded. Device information is translated according to Class, sub-Class, and Type

Triggering



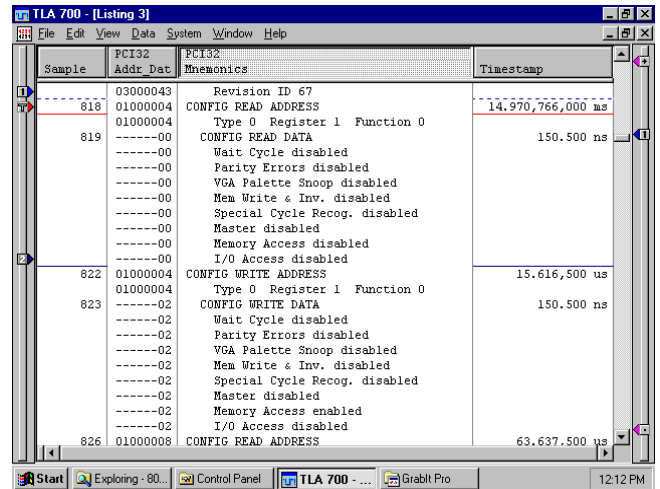
Trigger on pre-defined PMC cycles

Timing Analysis



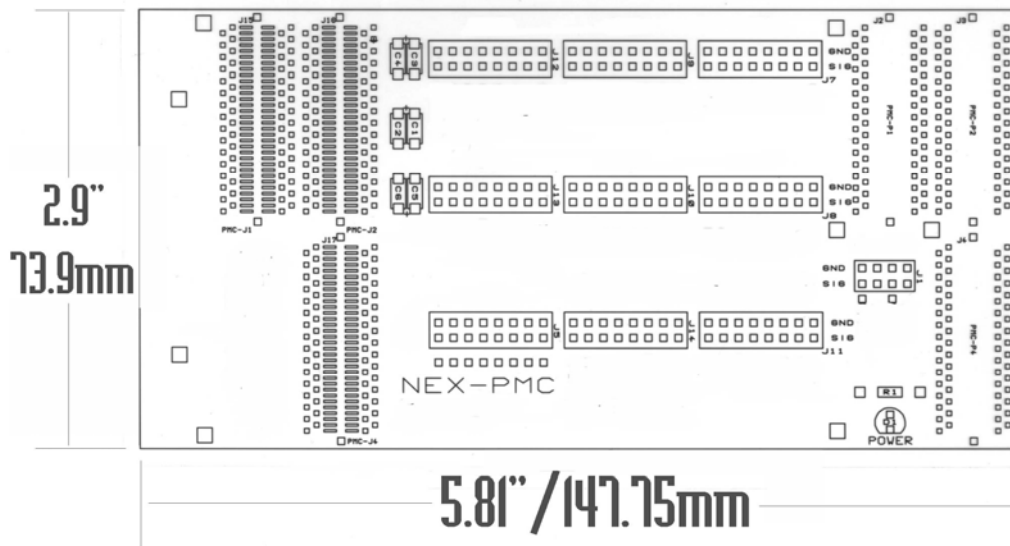
125ps acquisition on each channel provides excellent timing analysis. Each channel is labeled with the appropriate PMC signal name. Bus format display of grouped signals shown.

Disassembly (with Data Filtering)



Same disassembly display as Figure 1 with Memory and I/O cycles suppressed.

Mechanical Outline



Tektronix Logic Analyzers Supported

- TLA600 or TLA700 with a minimum of 68 channel acquisition module
- TLA510 or TLA520 (one acquisition module used)
- DAS9200 with a 92A96 or 92C96 (any memory depth)
- Prism 3000 with a 32GPX or 32GPD

Ordering / Contact Information

Part Number NEX-PMC

Includes: NEX-PMC 32-bit Adapter Board
Software for: DAS9200, TLA510/520 3 ½" floppy TLA600/TLA700 3 ½" floppy
Support for DAS9200 5 1/4" drive or Prism 3000 available upon request
Manual

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Website: www.nexustechnology.com

Placing an Order

Credit Card orders can be placed directly at 877-595-8116.
Purchase orders can be faxed to 877-595-8118.

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