DDR3 SODIMM Slot Protocol Interposer

Flexible Protocol Validation

- Low cost visibility
- High speed DDR3 protocol validation and analysis
- Passive 204-pin SODIMM slot interposer
- Designed for DDR3-2133+
- Automated logic analyzer setup
- Full DDR3 Compliance Analysis
- Compatible with Nexus Real-time MCA Memory Compliance
 Analyzer

Overview

This interposer provides low cost monitoring of a DDR3 SODIMM slot.

Command, address and control information is shown in a display window for easy viewing. Protocol violation analysis software is included.

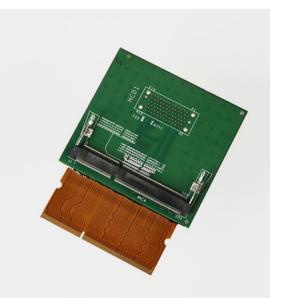
Performance You Can See™

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|--|---|--|---|--|--|----------|
| St - Cursor 1 | 🔻 to 🛛 Cursor | 2▼ = 5.996ns | ; | | | |
| Sample | Timestamp | ♥NewFilter NEX_COMM. | ₽_NewF | ■NewFilt NEX_CO | ₩ ^{NewFi} | ^ |
| 3545) 3581 3584 3593 3597 3599 3609 3634 3643 3643 3643 3643 3643 3643 364 | 9.004 ns 54.024 ns 13.536 c015 ns 2.969 ns 15.000 ns 37.500 ns 3.008 ns 3.008 ns 3.008 ns 3.008 ns 13.535 ns 55.6992 ns 10.488 ns 3.008 ns 3.008 ns 5.508 ns 3.008 ns 5.508 ns 3.008 ns 5.508 ns 3.008 ns 5.5992 ns 10.488 ns 5.5993 ns 5.5993 ns 5.5993 ns 5.5993 ns | RANKK 1 RANKK 1 RRANKK 1 | RD PRE ACT MR PREFA REF ACT PRE RD PRE ACT PRE RD PRE RD PRE ACT PRE RD PRE RD PRE RD PRE RD PRE PRE PRE RD PRE PRE RD PRE RD PRE RE RC RC RC RC RC RC RC RC RC RC RC RC RC | 5 5 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 | 03C0 0000 3010 0388 03C0 0400 0400 0000 03C8 03D0 03D0 03C8 03D0 03C8 03D0 03D0 03D0 03C8 03D0 | |
| 3853 3859 3896 | 3.027 ns 8.985 ns 55.488 ns | RANK 1 RANK 1 RANK 1 | RD RD PRE | Bank 5 Bank 5 Bank 5 | 03E8 03F0 0000 | ~ |

Figure 1 State Display of Command, Address, & Control

| Sample C | ommand | Rank | Bank | Row/Col Addr. | Error |
|--|----------------------------|---|------------------------------------|--|--|
| 1658 R | D | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1676 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1694 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1712 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1716 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1720 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1724 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1742 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1760 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| 1778 R | | 0 | NA | NA | RD command to rank with I/O gating overdriving sense a |
| equires tNWR(1 | | | | | BD command to end with U/O antine suscritiving anose a |
| RD command to equires tNWR(1 ummary | 10007cks). | Rank re | ceived o | | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109:38 r |
| RD command to equires tNWR(1 ummary Name | 10007cks). | Rank re | ceived o | nly 392cks. Commands In Tim | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109:38 r |
| RD command to equires tNWR(1 UMMARY Name Total Samples | 10007cks). | Rank re Value 8194 | ceived o | nly 392cks. Commands In Tim Protocol Err. | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109:38 r |
| RD command to equires tNWR(1 UMMARY Name Total Samples Total Command | 10007cks). | Rank re Value 8194 1557 | ceived o | nly 392cks. Commands In Tim | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109.38 r |
| RD command to equires tNWR(1 UMMARY Name Total Samples | 10007cks). | Rank re Value 8194 | ceived o | nly 392cks. Commands In Tim Protocol Err. | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109:38 r |
| RD command to equires tNWR(1 UMMARY Name Total Samples Total Command | 10007cks). 1 1s 2 | Rank re Value 8194 1557 | Ceived of F F | nly 392cks. Commands In Tim Protocol Err. Precharge | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109:38 r |
| RD command to equires tNWR(1 UMMARY Name Total Samples Total Command Errors Found | 10007cks). | Rank re Value 8194 1557 22 | Ceived of F F F | nly 392cks. Commands In Tim Protocol Err. Precharge Activate Read | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109:38 r |
| RD command to equires tNWR(1 UMMAIY Name Total Samples Total Command Errors Found Command Activ | 10007cks). | Rank re Value 8194 1557 22 19.00% | Ceived of F F F | nly 392cks. Commands In Tim Protocol Err. Precharge Activate | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109.36 r |
| RD command to equires tNWR(1 UMMARY Name Total Samples Total Command Errors Found Command Activ Read Activity | 10007cks). | Rank re Value 8194 1557 22 19.00% 11.86% | Ceived or F F A F V | nly 392cks. Commands In Time Protocol Err. Precharge Activate Read Vrite | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109.38 r |
| RD command to equires tNWR(1 UMMAIY Name Total Samples Total Command Errors Found Command Activity Read Activity Refresh Comma Precharge Com | 10007cks). | Rank re Value 8194 1557 22 19.00% 11.86% 0.01% 2 290 | Ceived or F F A F V | nly 392cks. | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109.38 r e |
| RD command to equires tNWR(1 UMMATY Name Total Samples Total Command Errors Found Command Activ Read Activity Write Activity Refresh Comma | 10007cks). | Rank re Value 8194 1557 22 19.00% 11.86% 0.01% 2 | Ceived or F F A F V | nly 392cks. Commands In Time Protocol Err. Precharge Activate Read Vrite ~1.5 | ers because of a previous write (WR or WRA) command. Rank Analysis completed in 109.36 r |

Figure 2 Protocol Violation Analysis



Software

This DDR3 SODIMM slot protocol interposer comes with logic analyzer setup software that acquires and displays command, address, and control information from a SODIMM slot. Protocol violation analysis software is also included.

Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides protocol decoding of the DDR3 transactions (Command, Address and Control only) for easy display and logic analyzer triggering/filtering.

Compliance Analysis Software

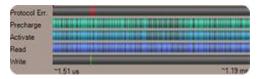


There's a BIG difference between protocol decode and protocol violation analysis. Protocol decoding provides a static tabulation of command and address bus activity. This functionality is made available through the logic analyzer listing window using a Nexus Technology DDR3 support package/setup software. Performing a very different and powerful set of tasks, protocol violation analysis analyzes the entire logic analyzer memory, compiling statistical information and error reporting based on every

command acquired. This provides a global picture of the activity on the bus and - more importantly - analyzes every command to see that the protocol adheres to the JEDEC specification. Please see the NEX-MCATLA-DDR3-SWL product webpage for more information.

Digital Validation

Logic analyzer setup software (TLA support package) is included with this product.



The Optional Memory Compliance Analysis software provides statistical information and global bus activity to quickly give the user an overview of the DDR3 bus activity without having to revert to a listing or waveform window. The software also performs basic protocol violation checking. Advanced

protocol violation checking is available for purchase separately. Please see the NEX-MCATLA-DDR3-SWL product webpage for more information.

DDR3 SODIMM Slot Protocol Interposer

NEX-SODDR3INTR-P Technical Specification

General

| Specification | Detail |
|----------------------------------|---|
| Interface Type | Passive Interposer |
| LA Interface | NEX-PRB1-XL |
| JEDEC Module Type | DDR3 SDRAM Unbuffered SODIMM (reversed or standard connectors) |
| DDR3 Data Rates Supported (MT/s) | DDR3-2133+ |
| Min. Voltage Swing | 200mv |
| Min. Eye Width | 200ps |

Tektronix Hardware

| Specification | Detail | Quantity |
|--------------------------|--|----------|
| Logic Analyzer Mainframe | TLA7000 | 1 |
| Logic Analyzer Module(s) | TLA7BB2/3/4 (1.4GHz Opt. Required for DDR3- >1333) | 1 |
| Logic Analyzer Probes | NEX-PRB1-XL | 1 |

DDR3 Signals Probed

| Specification | Detail |
|---------------|---|
| Command | RAS#, CAS#, WE#, CKE0, CKE1, RESET#, ODT0, ODT1 |
| Addressing | CS0#, CS1#, A00-A15, BA0-BA2 |

Product Configurations

| Nomenclature | LA Probes Included | Nexus Hardware Included | Nexus Software Included |
|---------------------|--------------------|---|--|
| NEX-SODDR3INTR-P | No | 1- DDR3 SODIMM Slot Protocol Interposer | TLA Setup, Protocol Decode, and Full Protocol Violation Analysis |
| NEX-SODDR3INTR-P-PR | Yes | 1- DDR3 SODIMM Slot Protocol Interposer 1- NEX-PRB1-XL | TLA Setup, Protocol Decode, and Full Protocol Violation Analysis |

Further Information

Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

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